

# BLF8G10LS-270V; BLF8G10LS-270GV

Power LDMOS transistor

Rev. 2 — 1 September 2015

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

270 W LDMOS power transistor with improved video bandwidth for base station applications at frequencies from 790 MHz to 960 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ }^{\circ}\text{C}$  in a common source class-AB production test circuit, tested on straight lead device.

Test signal	f (MHz)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)	ACPR <sub>5M</sub> (dBc)
2-carrier W-CDMA	869 to 894	28	67	19.5	31	-37 <sup>[1]</sup>

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 10 MHz.

### 1.2 Features and benefits

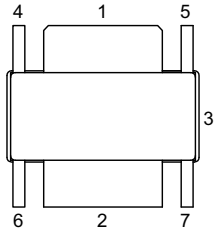
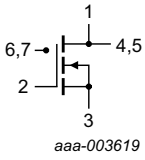
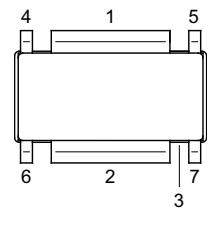
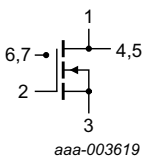
- Excellent ruggedness
- High efficiency
- Low  $R_{th}$  providing excellent thermal stability
- Designed for broadband operation (790 MHz to 960 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Decoupling leads to enable improved video bandwidth (55 MHz typical)
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Design optimized for gull-wing and straight lead versions
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 790 MHz to 960 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF8G10LS-270V (SOT1244B)</b>			
1	drain		 <p>aaa-003619</p>
2	gate		
3	source		
4	decoupling lead		
5	decoupling lead		
6	n.c.		
7	n.c.		
<b>BLF8G10LS-270GV (SOT1244C)</b>			
1	drain		 <p>aaa-003619</p>
2	gate		
3	source		
4	decoupling lead		
5	decoupling lead		
6	n.c.		
7	n.c.		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BLF8G10LS-270V	-	earless flanged ceramic package; 6 leads	SOT1244B
BLF8G10LS-270GV	-	earless flanged ceramic package; 6 leads	SOT1244C

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	225	°C

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 67\text{ W}$	0.257	K/W

## 6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 4.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 450\text{ mA}$	1.5	1.8	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	4.2	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	82	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	420	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 450\text{ mA}$	-	3.92	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 15.75\text{ A}$	-	0.04	-	$\Omega$

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1-64 DPCH;  $f_1 = 871.5\text{ MHz}; f_2 = 881.5\text{ MHz}; f_3 = 881.5\text{ MHz}; f_4 = 891.5\text{ MHz}; f_5 = 881.5\text{ MHz}; f_6 = 891.5\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 2000\text{ mA}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in a class-AB production test circuit, tested on straight lead device.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 67\text{ W}$	17.3	19.5	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 67\text{ W}$	-	-16	-12	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 67\text{ W}$	26	31	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)} = 67\text{ W}$	-	-37	-33	dBc

## 7. Test information

### 7.1 Ruggedness in class-AB operation

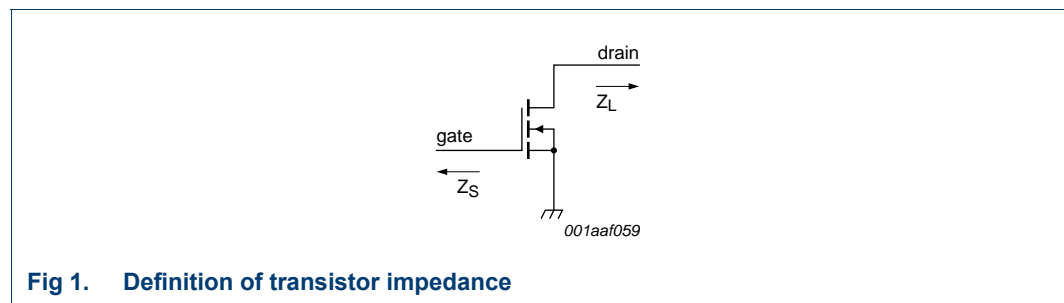
The BLF8G10LS-270V and BLF8G10LS-270GV are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 28\text{ V}; I_{Dq} = 2000\text{ mA}; P_L = 270\text{ W}; f = 820\text{ MHz}; f = 869\text{ MHz}; f = 920\text{ MHz}; f = 960\text{ MHz}$  and a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions:  $V_{DS} = 28\text{ V}; I_{Dq} = 2000\text{ mA}; P_L = 270\text{ W}; f = 790\text{ MHz}$ .

### 7.2 Impedance information

**Table 8. Typical impedance**  
*I<sub>Dq</sub> = 2700 mA; main transistor V<sub>DS</sub> = 28 V.*

f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)
790	1.4 – j1.84	1.22 – j2.07
820	1.58 – j1.96	1.29 – j1.95
869	1.84 – j2.70	1.12 – j1.83
881	1.78 – j2.94	1.12 – j1.84
894	1.90 – j3.08	1.12 – j1.84
920	2.06 – j2.50	1.04 – j1.13
940	2.10 – j2.90	1.04 – j1.13
960	2.56 – j2.65	1.00 – j1.22

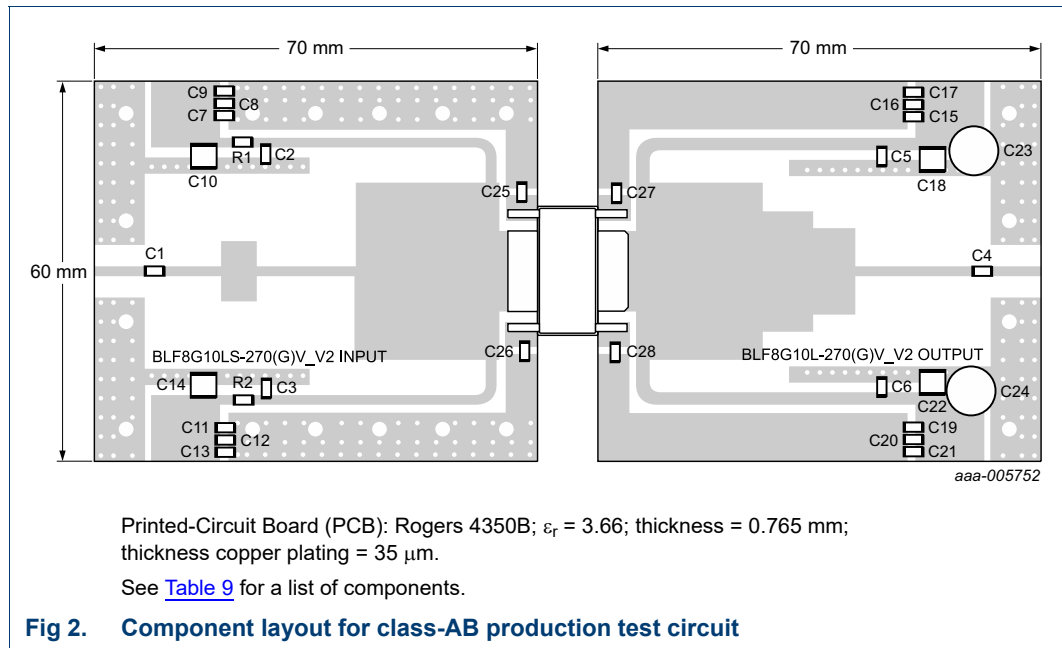
[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).



### 7.3 VBW in class-AB operation

The BLF8G10LS-270V and BLF8G10LS-270GV show 55 MHz (typical) video bandwidth in class-AB test circuit in 800 MHz band at V<sub>DS</sub> = 28 V and I<sub>Dq</sub> = 2 A.

7.4 Test circuit



**Table 9. List of components**

For test circuit see [Figure 2](#).

Component	Description	Value	Remarks
C1, C4	multilayer ceramic chip capacitor	47 pF	[1] ATC100B
C2, C3, C5, C6	multilayer ceramic chip capacitor	45 pF	[1] ATC100B
C7, C11, C15, C19	multilayer ceramic chip capacitor	0.01 $\mu\text{F}$	[2] Murata
C8, C12, C16, C20	multilayer ceramic chip capacitor	0.1 $\mu\text{F}$	[2] Murata
C9, C13, C17, C21	multilayer ceramic chip capacitor	1 $\mu\text{F}$	[2] Murata
C10, C14, C18, C22	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$	[2] Murata
C23, C24	electrolytic capacitor	470 $\mu\text{F}$ , 63 V	
C25, C26, C27, C28	multilayer ceramic chip capacitor	10 $\mu\text{F}$	[2] Murata
R1, R2	chip resistor	9.1 $\Omega$	[3] Vishay Dale 0805

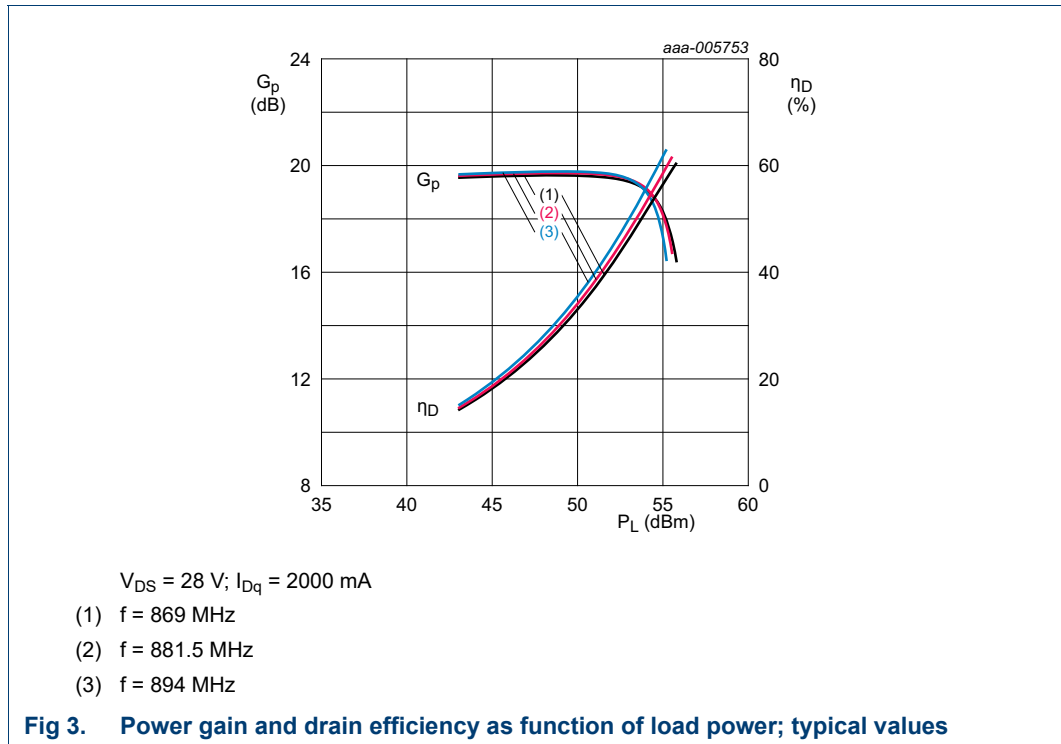
[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] Murata or capacitor of same quality.

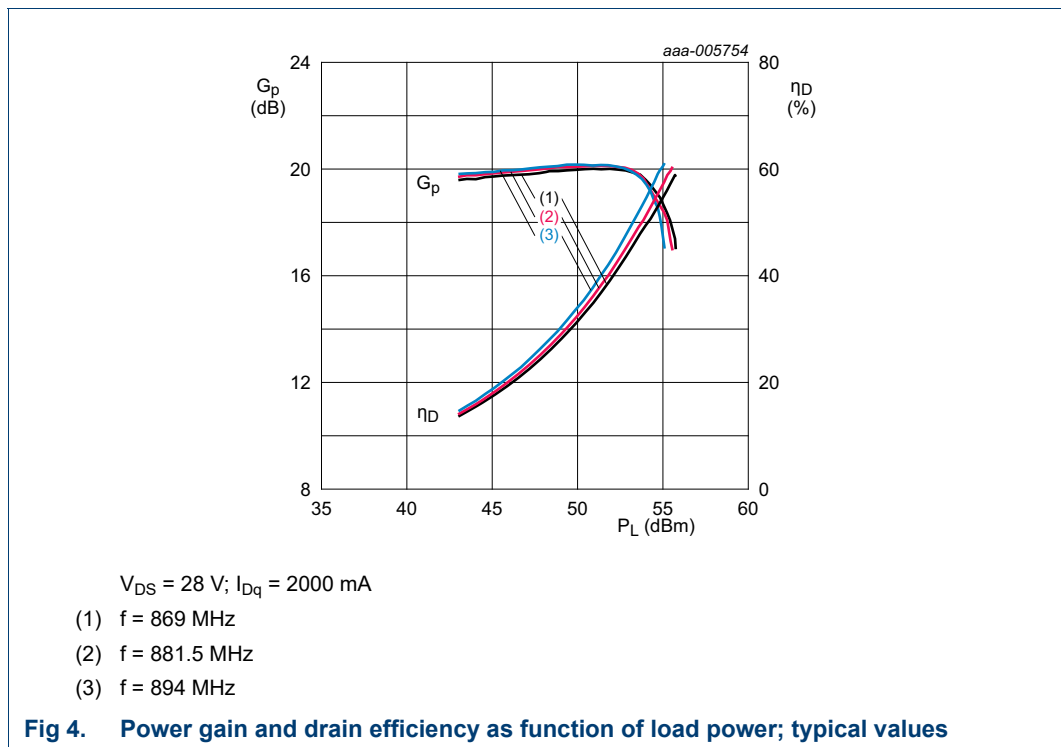
[3] Vishay Dale resistor of same quality.

7.5 Graphical data

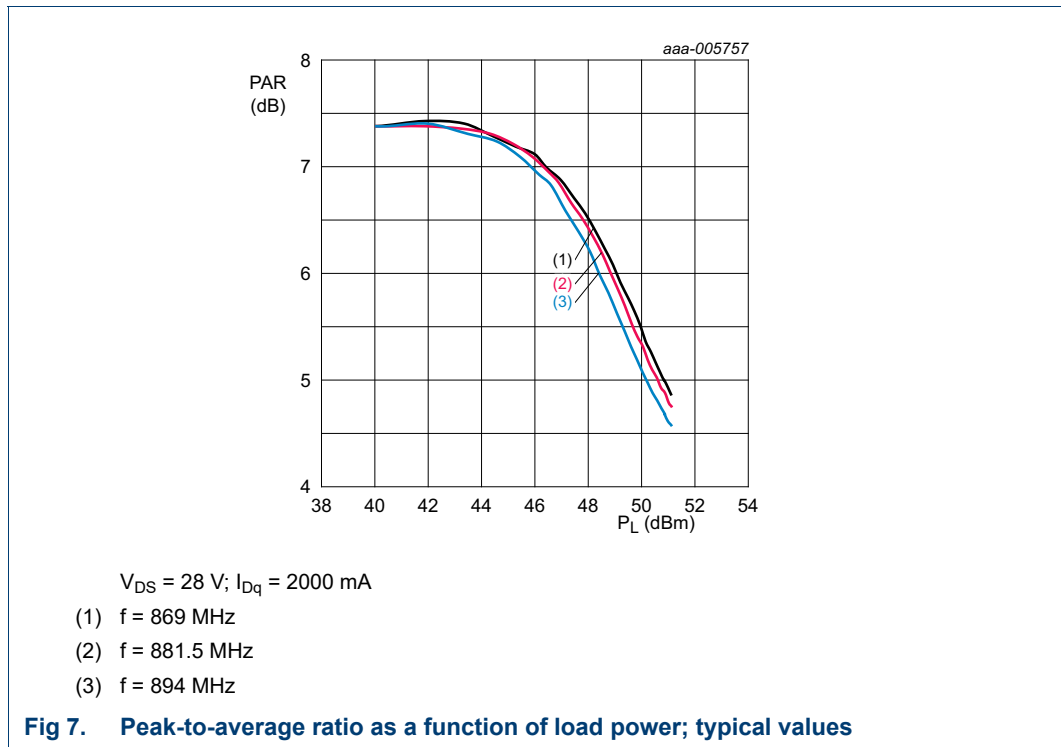
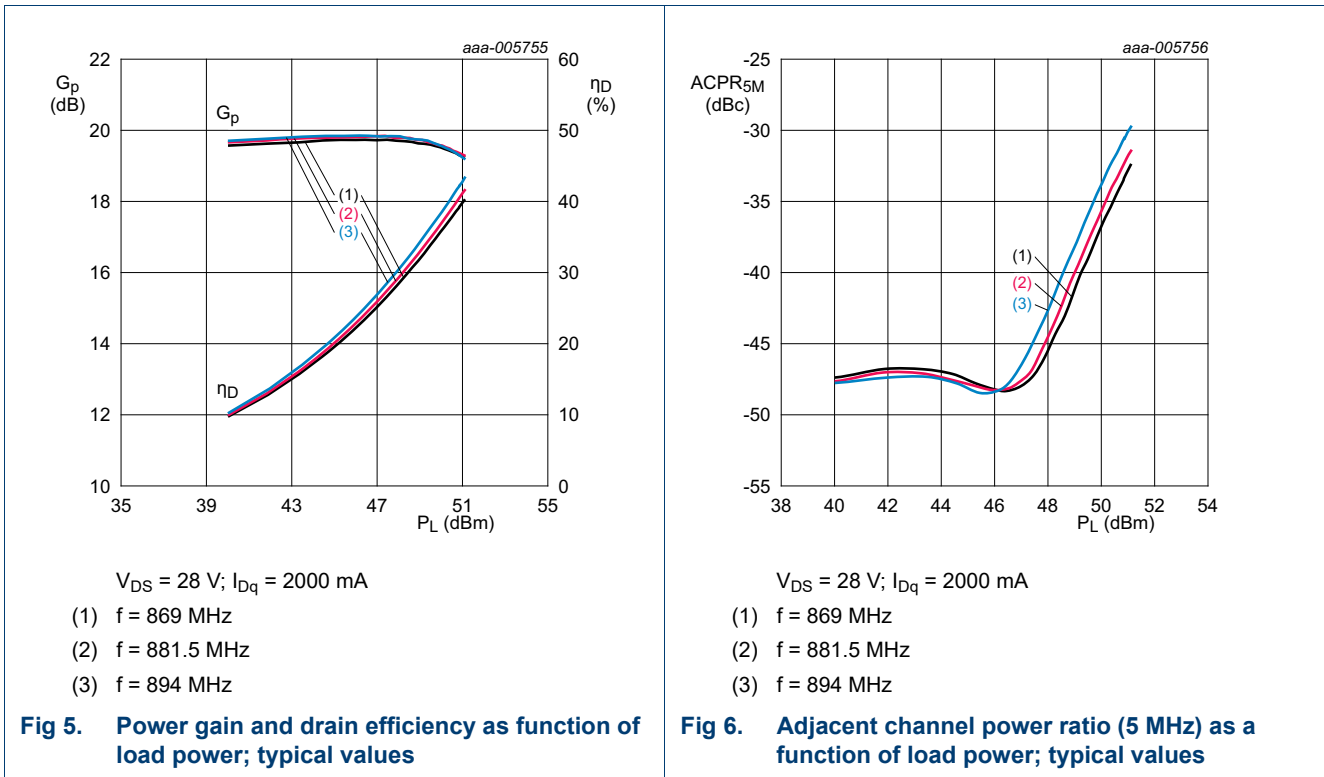
7.5.1 Straight lead sample CW



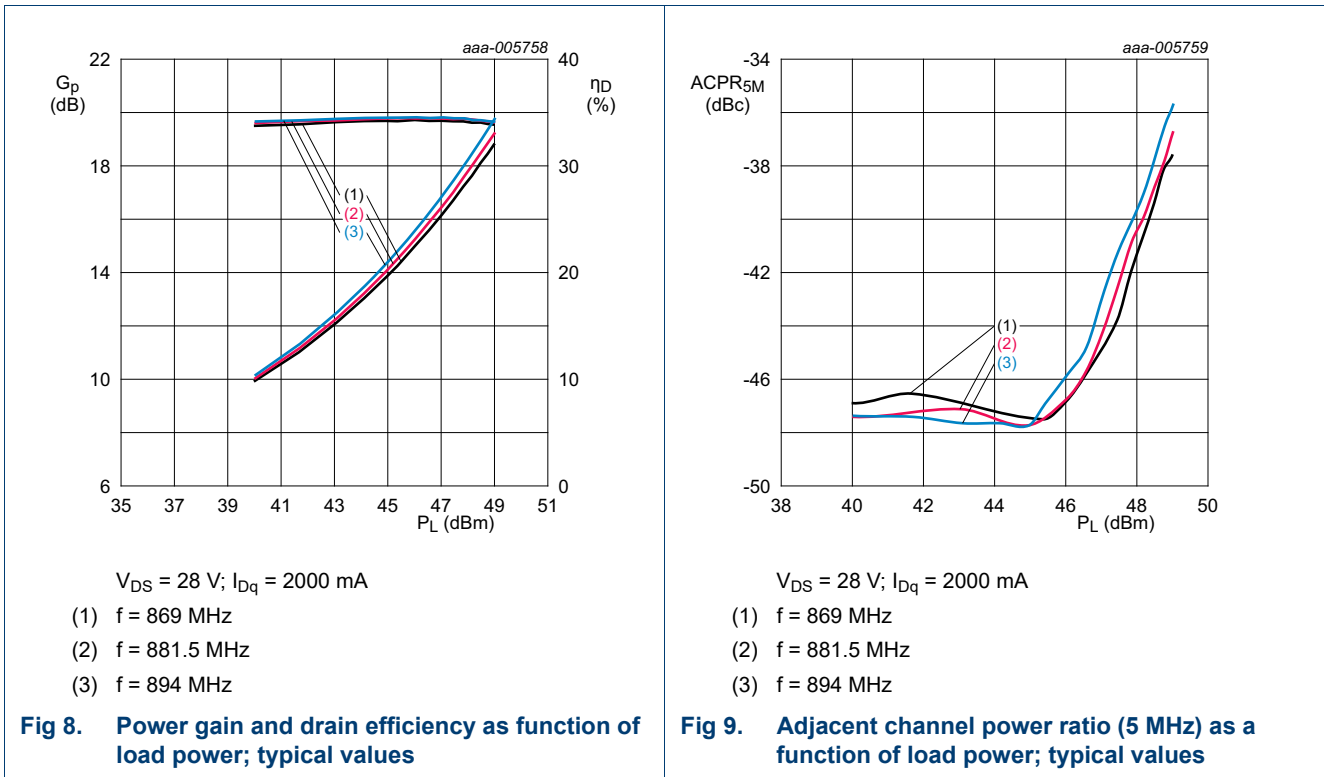
7.5.2 Straight lead sample CW pulsed



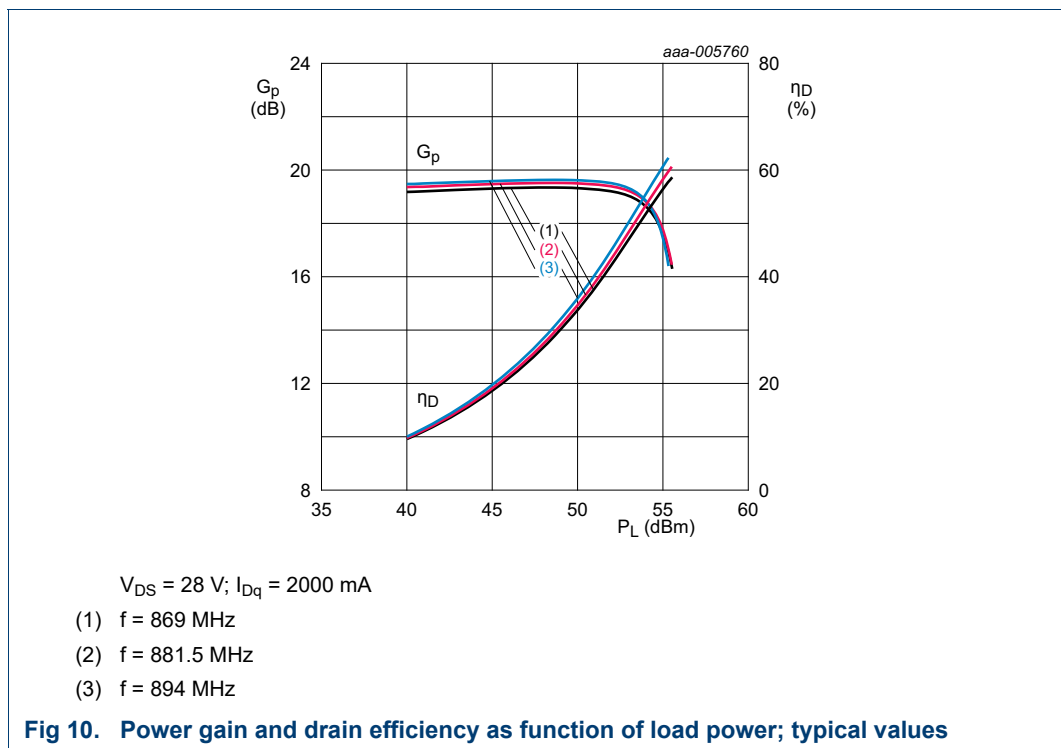
7.5.3 Straight lead sample 1-carrier W-CDMA



7.5.4 Straight lead sample 2-carrier W-CDMA

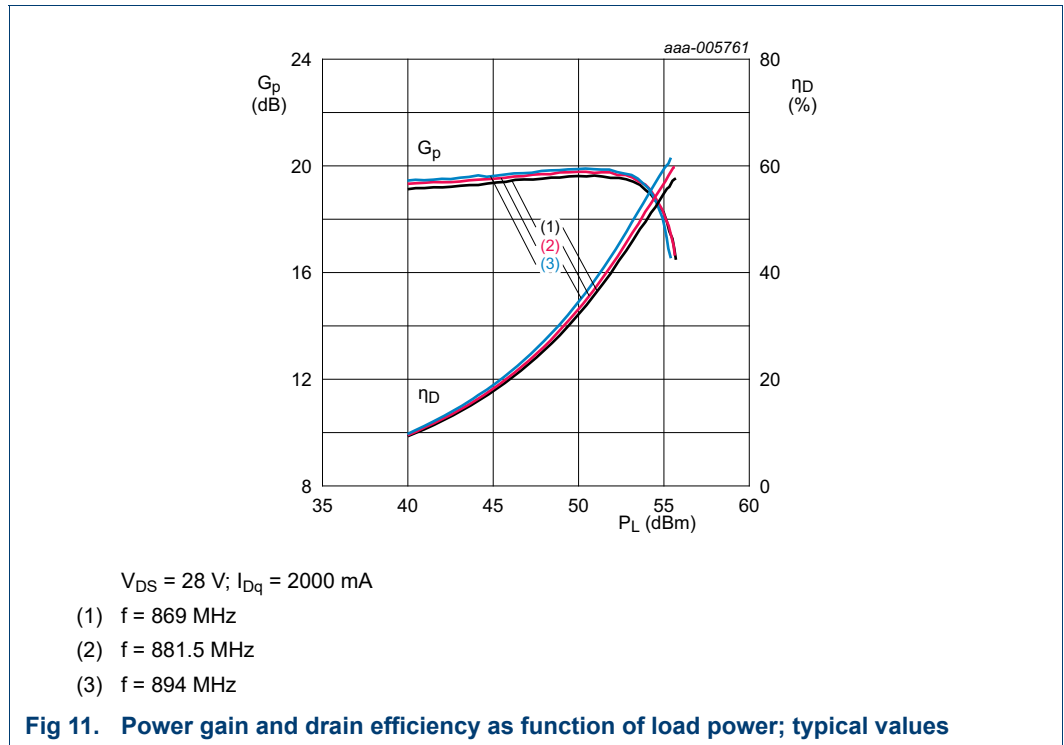


7.5.5 Gull-wing sample CW

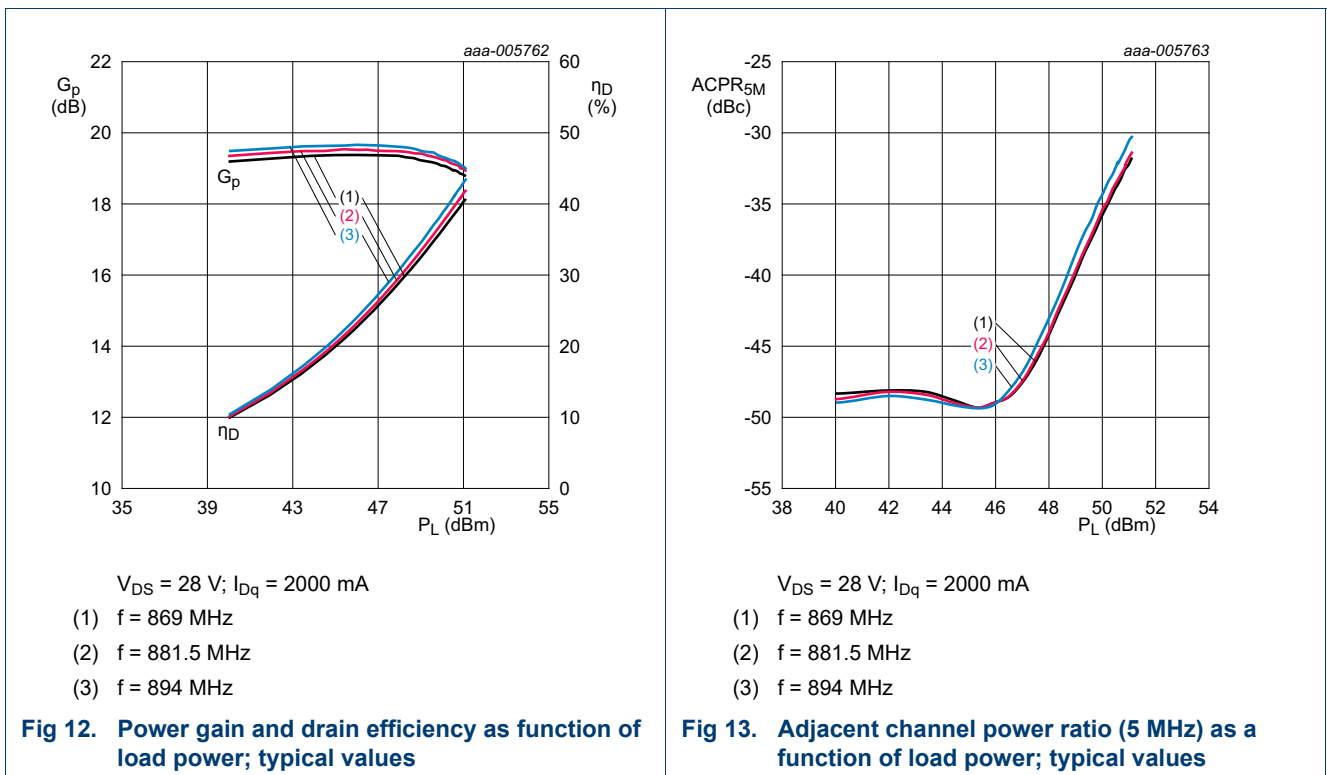


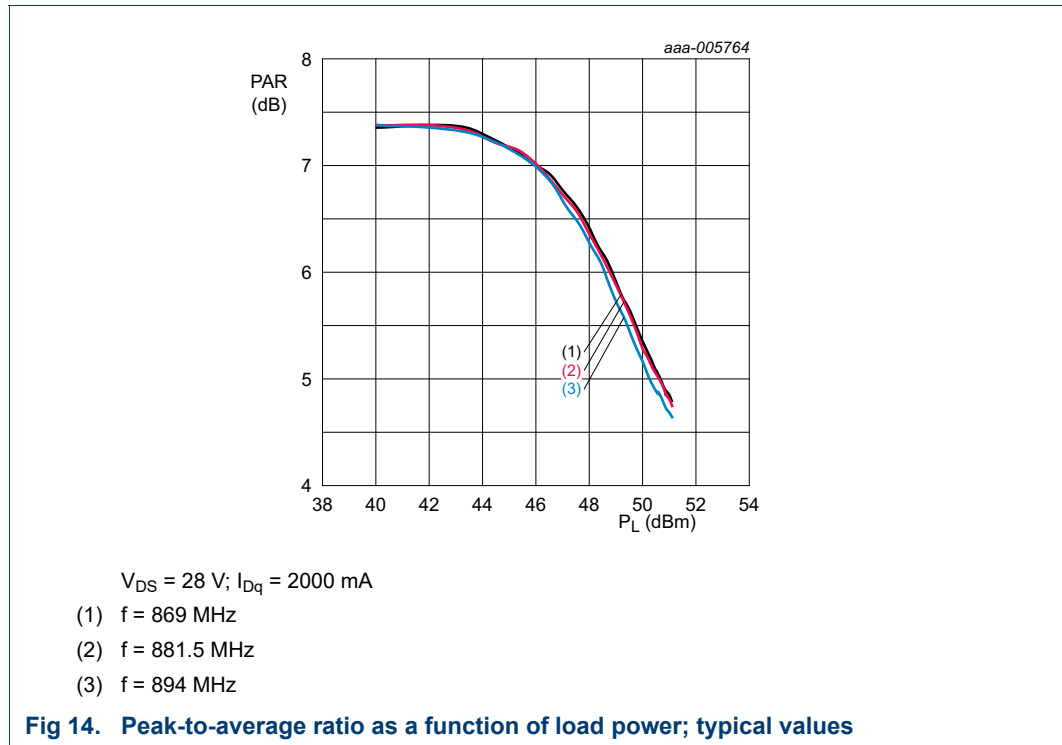


7.5.6 Gull-wing sample CW pulsed

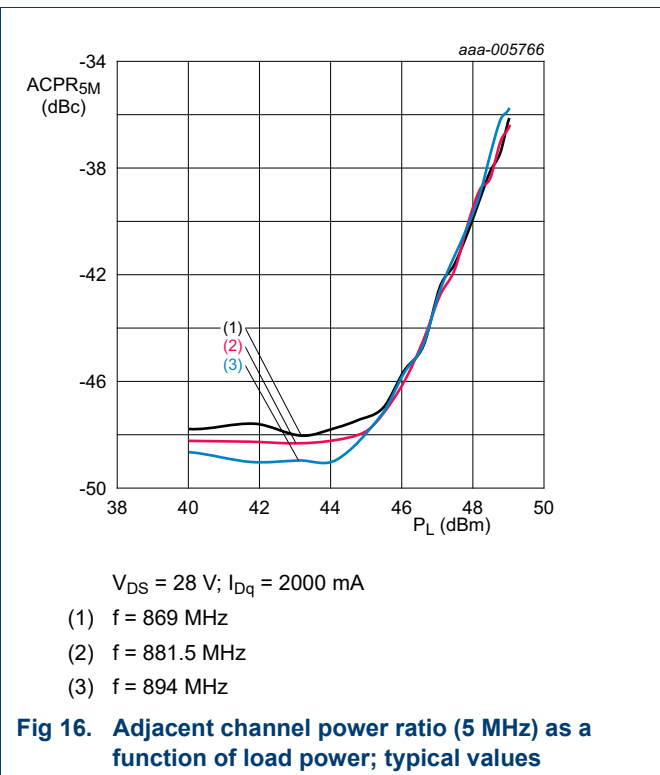
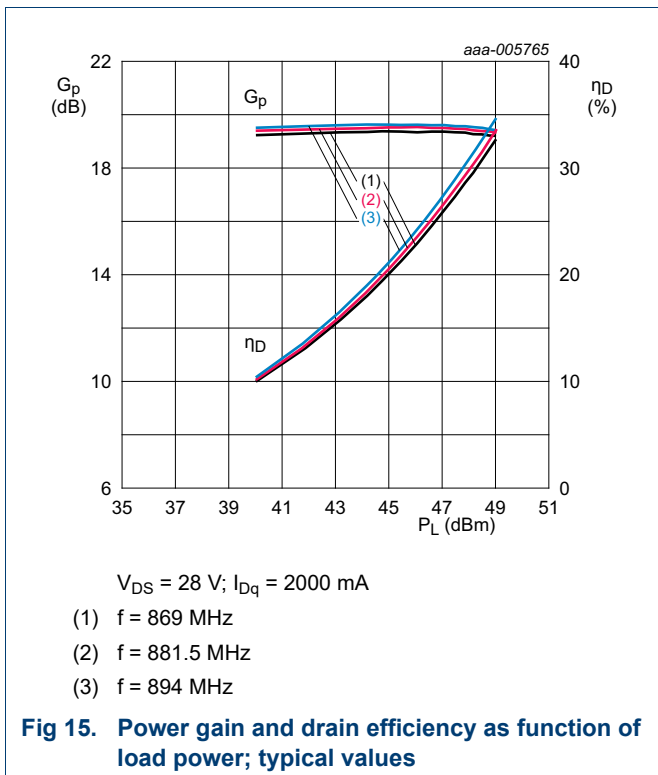


7.5.7 Gull-wing sample 1-carrier W-CDMA

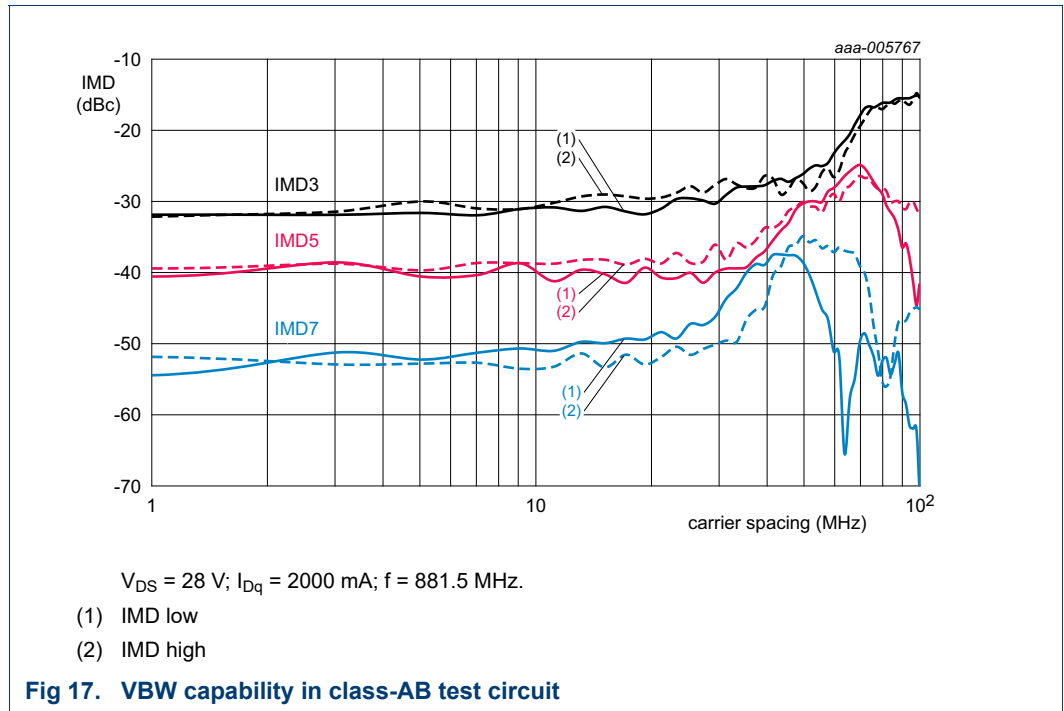




7.5.8 Gull-wing sample 2-carrier W-CDMA



7.5.9 2-Tone VBW



8. Package outline

Earless flanged ceramic package; 6 leads

SOT1244B

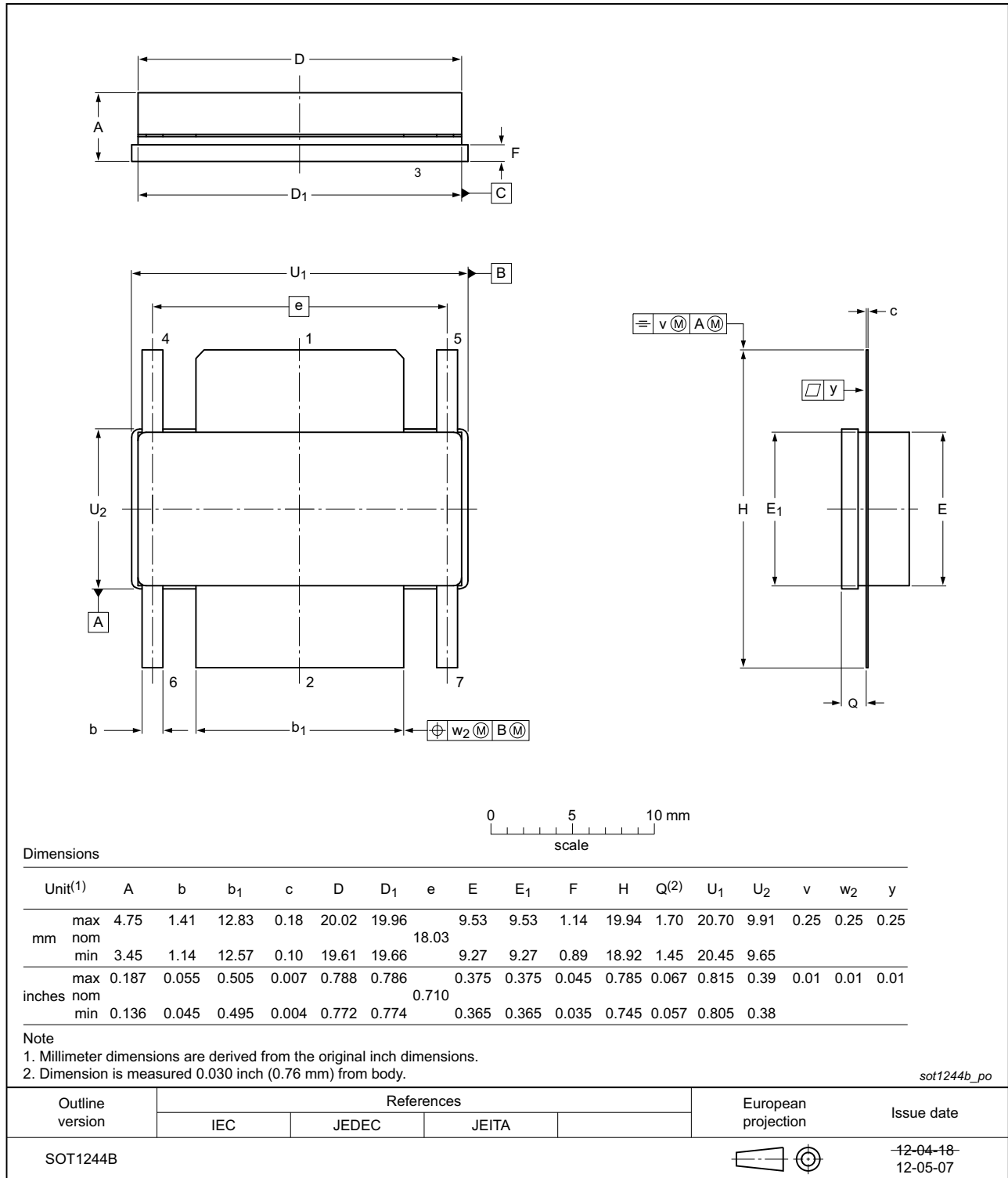


Fig 18. Package outline SOT1244B

Earless flanged ceramic package; 6 leads

SOT1244C

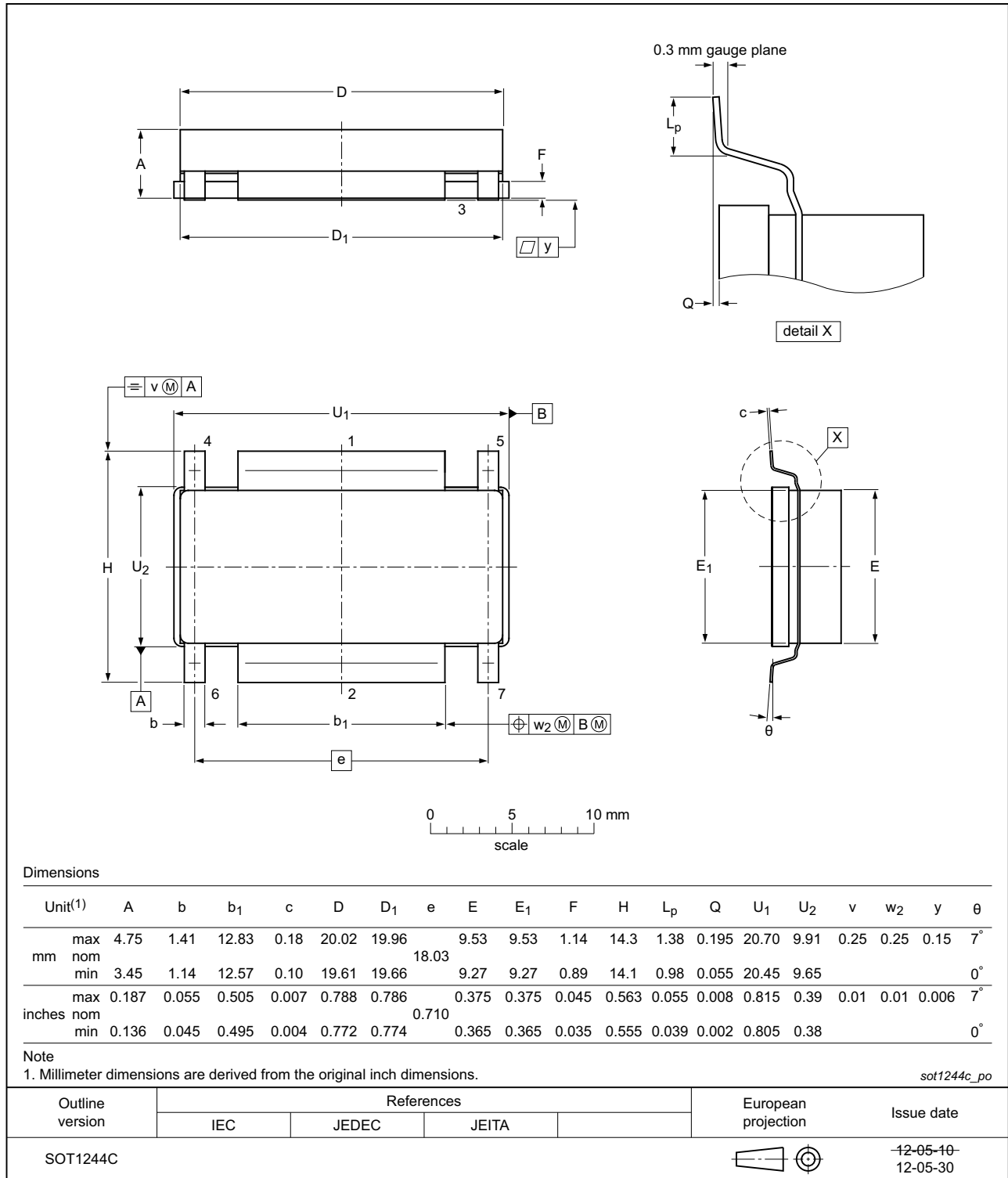


Fig 19. Package outline SOT1244C

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical Channel
ESD	ElectroStatic Discharge
IMD	InterModulation Distortion
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average Ratio
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G10LS-270V_8G10LS-270GV#2	20150901	Product data sheet	-	BLF8G10LS-270V_8G10LS-270GV v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
BLF8G10LS-270V_8G10LS-270GV v.1	20121203	Product data sheet	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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