BLF9G38-10G

Power LDMOS transistor

Rev. 1 — 19 October 2017

AMPLEON

Product data sheet

1. Product profile

1.1 General description

10 W LDMOS power transistor for base station applications at frequencies from 3400 MHz to 3600 MHz.

Table 1. Typical performance

RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	3400 to 3600	70	28	2	17.7	26	–30 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF per carrier; 5 MHz carrier spacing.

1.2 Features and benefits

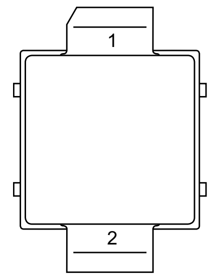
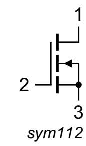
- High efficiency
- Integrated ESD protection
- Excellent ruggedness
- Excellent thermal stability
- Designed for broadband operation
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 3400 MHz to 3600 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF9G38-10G	-	earless flanged ceramic package; 2 leads	SOT975C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−0.5	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 2 W (CW)	4.5	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.11 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 10.5 mA	1.5	2	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	2.2	-	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 0.53 A	0.91	-	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 368 mA	561	-	2153	mΩ

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; 3GPP test model 1 with 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; f_1 = 3402.5 MHz; f_2 = 3407.5 MHz; f_3 = 3592.5 MHz; f_4 = 3597.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 70 mA; T_{case} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 2 W	16.5	17.7	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 2 W	-	−10	−6	dB
η_D	drain efficiency	$P_{L(AV)}$ = 2 W	21	26	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 2 W	-	−30	−25	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF9G38-10G is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 70 mA; P_L = 10 W (CW); f = 3400 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data of device; I_{Dq} = 70 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs: δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
3300	11.1 – j22.0	9.9 – j6.7	14.8	56.8	15.4
3400	15.0 – j19.0	8.7 – j8.4	14.6	57.1	15.6
3500	15.2 – j13.0	7.9 – j8.8	15.0	60.4	15.9
3600	11.8 – j11.0	7.8 – j10.4	15.0	59.3	15.4
3700	7.0 – j9.7	9.0 – j10.7	14.9	57.7	14.7
3800	4.2 – j11.4	9.1 – j11.5	14.6	57.9	15.0
Maximum drain efficiency load					
3300	11.1 – j22.0	4.8 – j5.6	11.3	62.8	17.7
3400	15.0 – j19.0	3.8 – j6.9	11.1	66.5	18.3
3500	15.2 – j13.0	3.1 – j8.2	10.1	68.4	18.9
3600	11.8 – j11.0	3.9 – j8.6	10.8	68.1	18.2
3700	7.0 – j9.7	4.0 – j9.8	10.6	66.1	17.2
3800	4.2 – j11.4	4.0 – j11.4	10.4	64.8	17.9

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

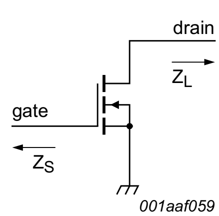
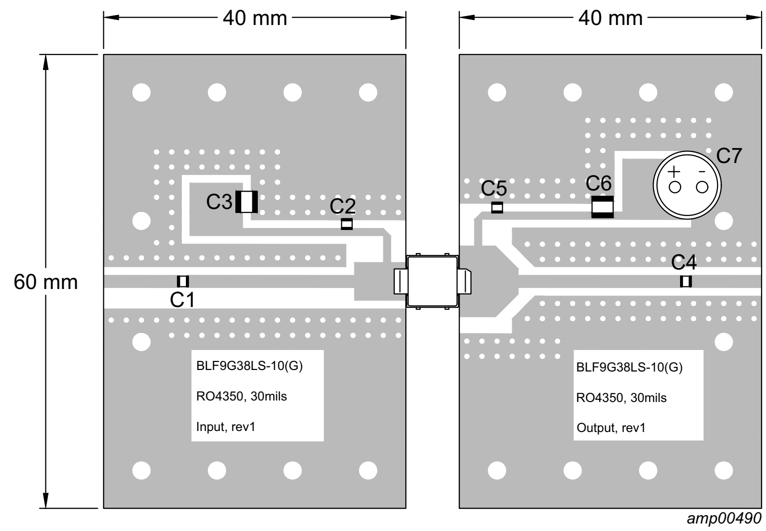


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.76 mm.

See Table 9 for a list of components.

Fig 2. Component layout for test circuit

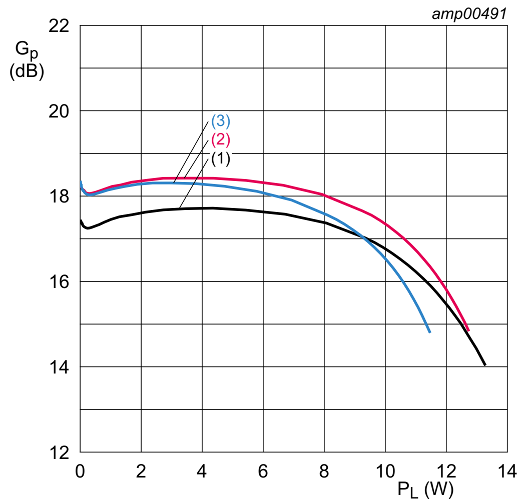
Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	8.2 pF	ATC 100A
C2	multilayer ceramic chip capacitor	8.2 pF	ATC 100A
C3	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata
C4	multilayer ceramic chip capacitor	7.5 pF	ATC 100A
C5	multilayer ceramic chip capacitor	8.2 pF	ATC 100A
C6	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata
C7	electrolytic capacitor	220 μF	

7.4 Graphical data

7.4.1 Pulsed CW



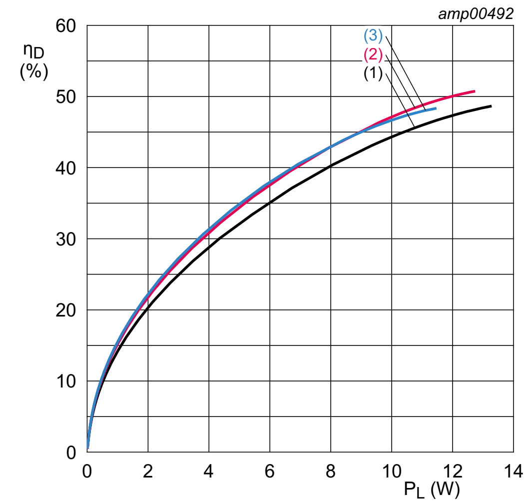
V_{DS} = 28 V; I_{Dq} = 70 mA; t_p = 100 μs; δ = 10 %.

(1) f = 3405 MHz

(2) f = 3500 MHz

(3) f = 3595 MHz

Fig 3. Power gain as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 70 mA; t_p = 100 μs; δ = 10 %.

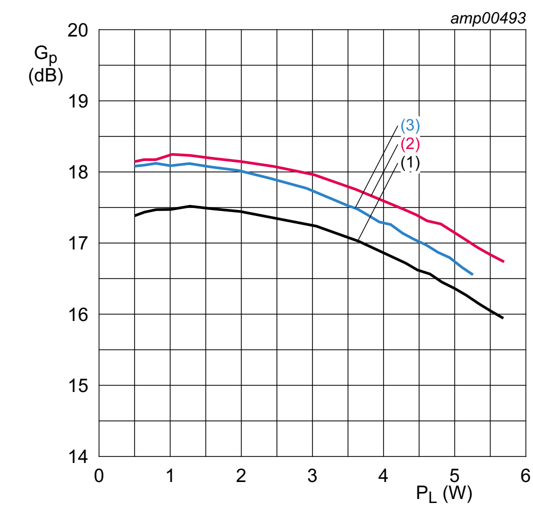
(1) f = 3405 MHz

(2) f = 3500 MHz

(3) f = 3595 MHz

Fig 4. Drain efficiency as a function of output power; typical values

7.4.2 1-Carrier W-CDMA



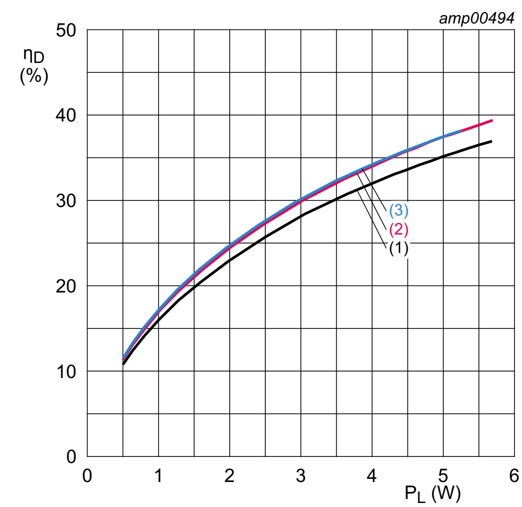
V_{DS} = 28 V; I_{Dq} = 70 mA.

(1) f = 3405 MHz

(2) f = 3500 MHz

(3) f = 3595 MHz

Fig 5. Power gain as a function of output power; typical values



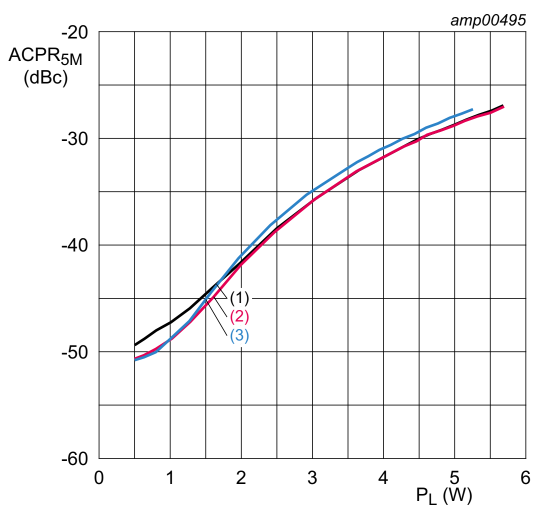
V_{DS} = 28 V; I_{Dq} = 70 mA.

(1) f = 3405 MHz

(2) f = 3500 MHz

(3) f = 3595 MHz

Fig 6. Drain efficiency as a function of output power; typical values



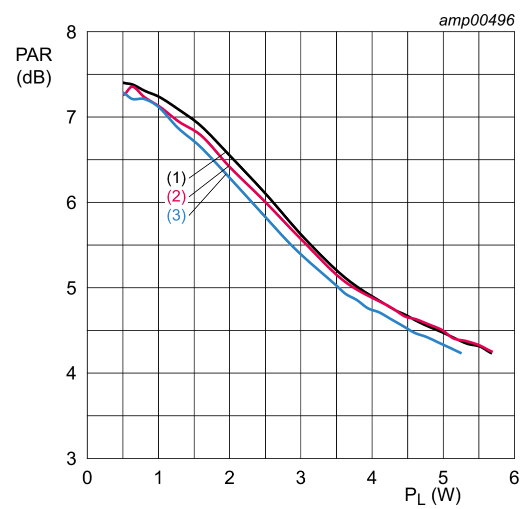
V_{DS} = 28 V; I_{Dq} = 70 mA.

(1) f = 3405 MHz

(2) f = 3500 MHz

(3) f = 3595 MHz

Fig 7. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 70 mA.

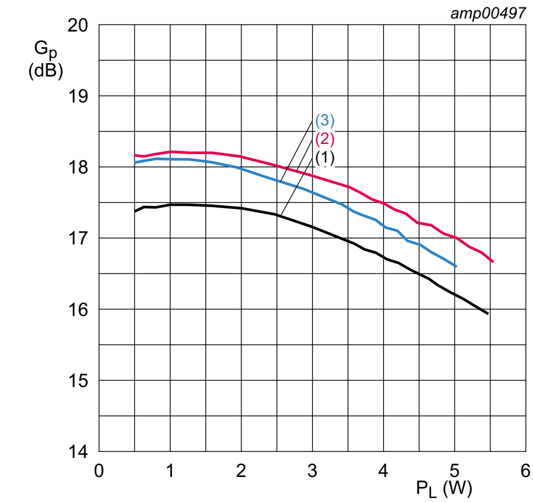
(1) f = 3405 MHz

(2) f = 3500 MHz

(3) f = 3595 MHz

Fig 8. Peak-to-average ratio as a function of output power; typical values

7.4.3 2-Carrier W-CDMA



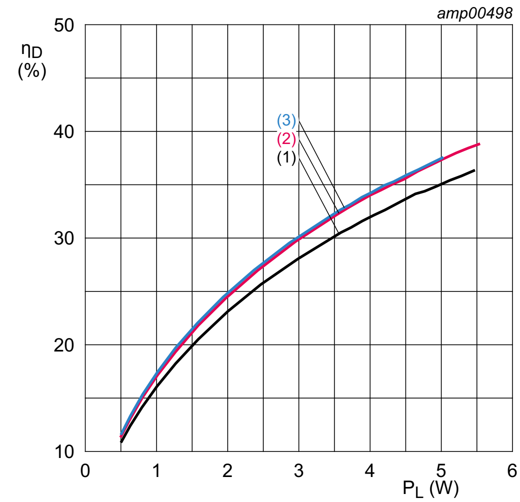
V_{DS} = 28 V; I_{Dq} = 70 mA; 5 MHz spacing.

(1) f = 3405 MHz

(2) f = 3500 MHz

(3) f = 3595 MHz

Fig 9. Power gain as a function of output power; typical values



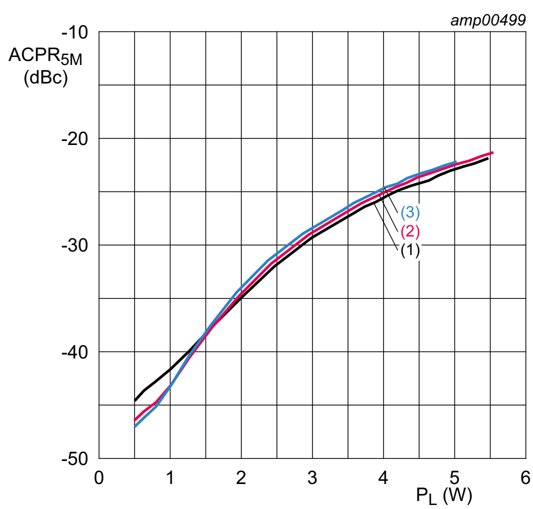
V_{DS} = 28 V; I_{Dq} = 70 mA; 5 MHz spacing.

(1) f = 3405 MHz

(2) f = 3500 MHz

(3) f = 3595 MHz

Fig 10. Drain efficiency as a function of output power; typical values



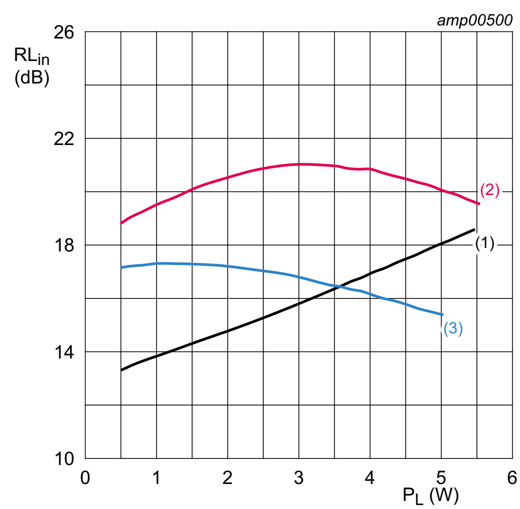
V_{DS} = 28 V; I_{Dq} = 70 mA; 5 MHz spacing.

(1) f = 3405 MHz

(2) f = 3500 MHz

(3) f = 3595 MHz

Fig 11. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 70 mA; 5 MHz spacing.

(1) f = 3405 MHz

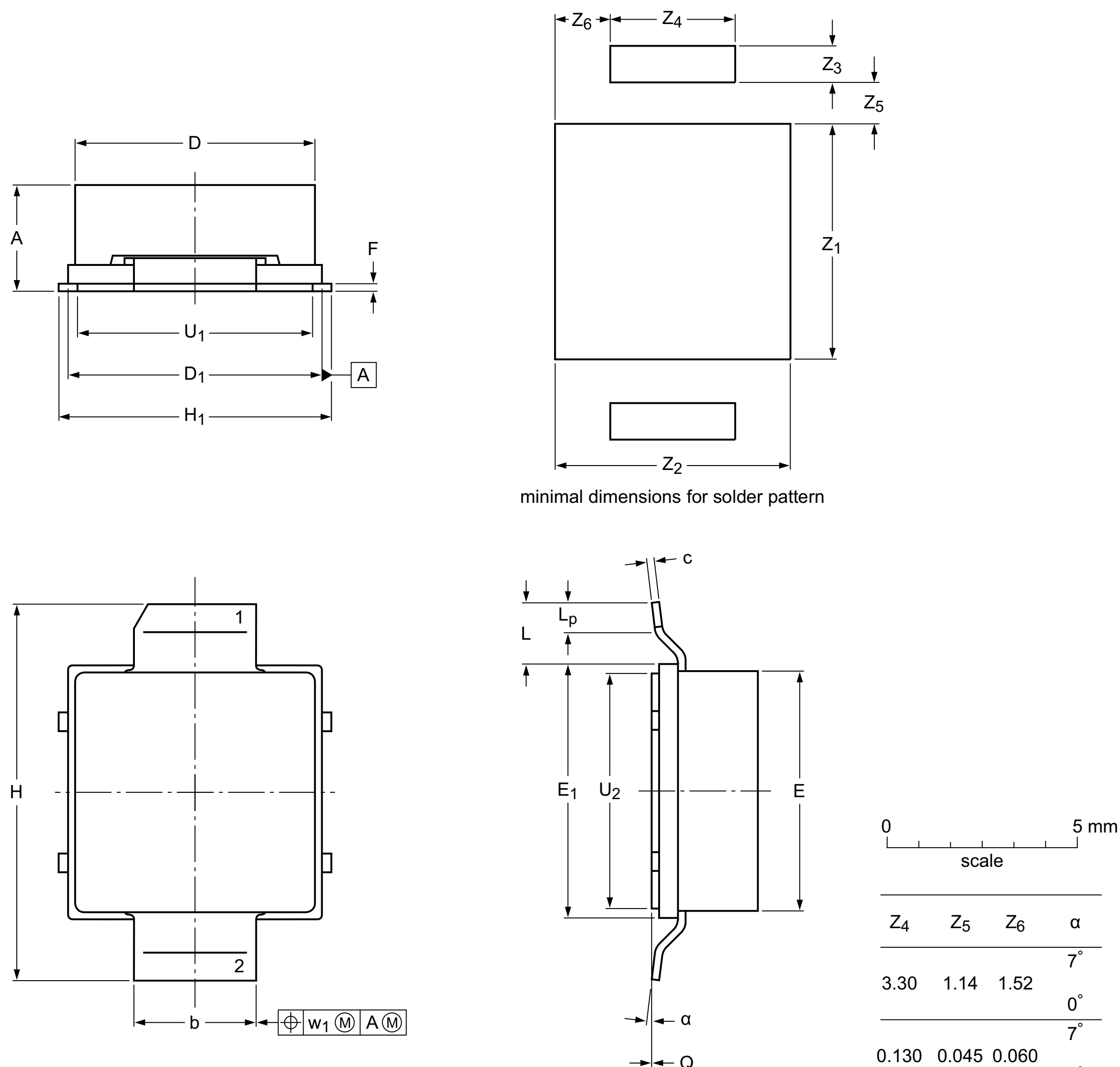
(2) f = 3500 MHz

(3) f = 3595 MHz

Fig 12. Input return loss as a function of output power; typical values

8. Package outline

Earless flanged ceramic package; 2 leads **SOT975C**



Z_4	Z_5	Z_6	α
3.30	1.14	1.52	7° 0°
0.130	0.045	0.060	7° 0°

Dimensions (mm dimensions are derived from the original inch dimensions)

Unit		A	b	c	D	D_1	E	E_1	F	H	H_1	L	L_p	Q	U_1	U_2	w_1	Z_1	Z_2	Z_3
mm	max	3.15	3.38	0.23	6.55	6.93	6.55	6.93	0.23	10.29	7.49		1.02	+0.05	6.43	6.43				
	nom											1.65					0.51	6.35	6.35	1.02
	min	2.59	3.23	0.18	6.40	6.78	6.40	6.78	0.18	10.03	6.73		0.51	-0.05	6.27	6.27				
inches	max	0.124	0.133	0.009	0.258	0.273	0.258	0.273	0.009	0.405	0.295		0.040	+0.002	0.253	0.253				
	nom											0.065					0.020	0.250	0.250	0.040
	min	0.102	0.127	0.007	0.252	0.267	0.252	0.267	0.007	0.395	0.265		0.020	-0.002	0.247	0.247				

sot975c_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT975C						~~08-07-10~~ 14-10-13

Fig 13. Package outline SOT975C

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average power Ratio
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF9G38-10G v.1	20171019	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

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13. Contact information

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For sales office addresses, please visit: **http://www.ampleon.com/sales**

14. Contents

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