BLF9G38LS-90P

Power LDMOS transistor

Rev. 2 — 3 July 2015 Product data sheet

1. Product profile

1.1 General description

90 W LDMOS power transistor for base station applications at frequencies from 3400 MHz to 3600 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in the Doherty application demo circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
IS-95	3400 to 3600	28	15.1	12.7	37.0	–37 [1]

[1] Test signal: IS-95; pilot, paging, sync, 6 traffic channels with Walsh codes 8 – 13; PAR = 9.7 dB at 0.01 % probability.

1.2 Features and benefits

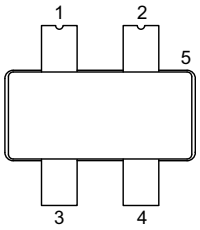
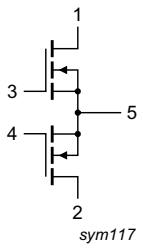
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifier for LTE base stations and multi carrier applications in the 3400 MHz to 3600 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF9G38LS-90P	-	earless flanged ceramic package; 4 leads	SOT1121B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 80 °C; V_{DS} = 28 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.0 V [1]		
		P_L = 18 W (CW)	0.37	K/W
		P_L = 56 W (CW)	0.22	K/W

[1] Measured in Doherty development circuit for thermal measurement

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.513 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 51.3mA	1.5	2.1	3.1	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 307.8 mA	1.7	2.3	3.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	11	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 51.3 mA	-	0.45	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1.8 A	-	236	449	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 3400 MHz; f_2 = 3500 MHz; f_3 = 3600 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 600 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit at frequencies from 3400 MHz to 3600 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 20 W	13.8	15.0	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 20 W	-	–10	–6	dB
η_D	drain efficiency	$P_{L(AV)}$ = 20 W	23	28	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 20 W	-	–26	–21	dBc

7. Test information

7.1 Ruggedness in Doherty operation

The BLF9G38LS-90P is capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 0.7 V; P_L = 56 W (CW); f = 3400 MHz; tested on the Doherty development test circuit.

7.2 Impedance information

Table 8. Typical impedance of maximum power and drain efficiency

Measured load-pull data (half device); I_{Dq} = 300 mA; V_{DS} = 28 V; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
3400	7.0 – j20.0	6.5 – j14.1	64	52.8	12.2
3600	18.1 – j29.7	7.9 – j15.2	61	50.9	12.5
3800	47.2 – j5.9	6.7 – j16.7	60	47.4	11.7
Maximum drain efficiency load					
3400	7.0 – j20.0	9.3 – j9.1	50	58.8	14.1
3600	18.1 – j29.7	7.5 – j10.3	50	55.6	14.1
3800	47.2 – j5.9	7.0 – j11.7	49	53.4	14.1

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

Table 9. Typical trade off impedance at 1 : 1 load

Measured load-pull data (half device); I_{Dq} = 300 mA; V_{DS} = 28 V; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(dBm)	(%)	(dB)
3400	7.0 – j20.0	8.5 – j12.3	60	57.9	13.3
3600	18.1 – j29.7	7.3 – j12.7	59	54.7	13.2
3800	47.2 – j5.9	7.7 – j13.9	56	52.3	13.1

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

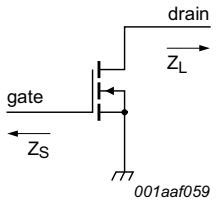
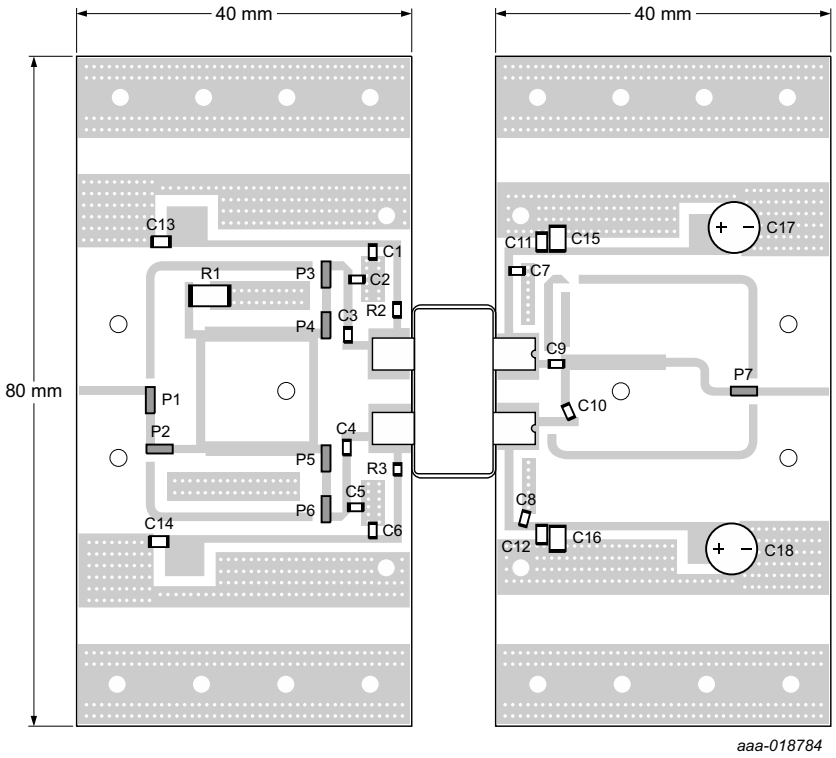


Fig 1. Definition of transistor impedance

7.3 VBW in Doherty operation

The BLF9G38LS-90P shows 100 MHz (typical) video bandwidth in Doherty development test circuit in 3500 MHz at V_{DS} = 28 V; I_{Dq} = 300 mA and $V_{GS(amp)peak}$ = 0.6 V.

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.5; thickness = 0.508 mm; thickness copper plating = 35 μm.

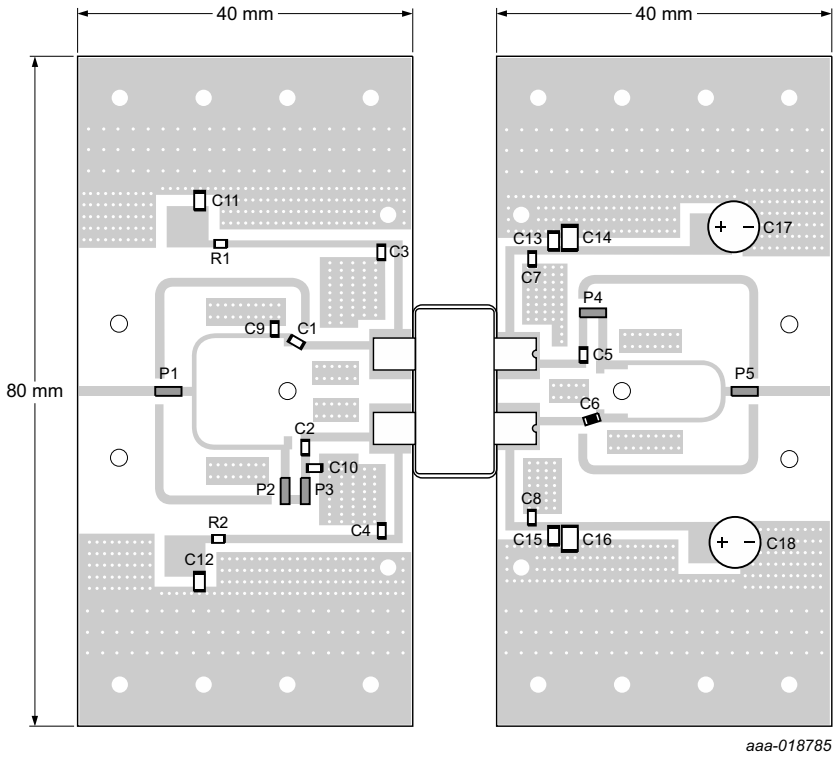
See Table 10 for a list of components.

Fig 2. Component layout for Doherty development test circuit

Table 10. List of components

See Figure 3 for component layout.

Component	Description	Value	Remarks
C1, C3, C4, C6, C7, C8, C10	multilayer ceramic chip capacitor	9.1 pF	ATC 600F
C2, C5	multilayer ceramic chip capacitor	0.9 pF	ATC 600F
C9	multilayer ceramic chip capacitor	1.3 pF	ATC 600F
C11, C12, C13, C14	multilayer ceramic chip capacitor	1 μF, 50 V	Murata
C15, C16	multilayer ceramic chip capacitor	10 μF, 50 V	Murata
C17, C18	electrolytic capacitor	2200 μF, 63 V	
P1, P2, P3, P4, P5, P6, P7	copper foil strip	-	needed for tuning
R1	SMD resistor	50 Ω	SMD 2512
R2, R3	SMD resistor	5.1 Ω	SMD 0805



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.5; thickness = 0.508 mm; thickness copper plating = 35 μm.

See Table 11 for a list of components.

Fig 3. Component layout for class-AB production test circuit

Table 11. List of components

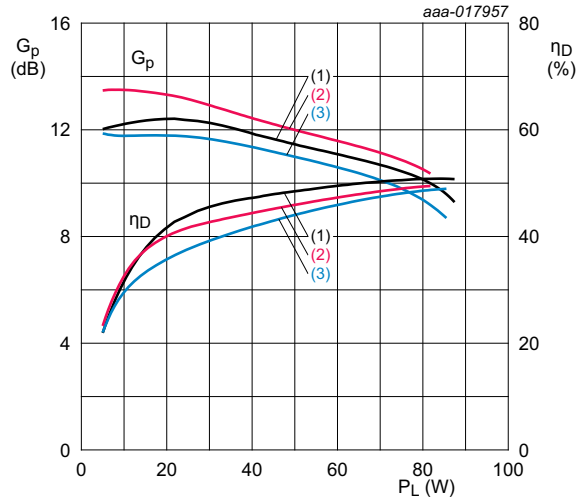
See Figure 3 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4, C5, C6, C7, C8	multilayer ceramic chip capacitor	9.1 pF	ATC 600F
C9, C10	multilayer ceramic chip capacitor	0.6 pF	ATC 600F
C11, C12, C13, C15	multilayer ceramic chip capacitor	1 μF, 50 V	Murata
C14, C16	multilayer ceramic chip capacitor	10 μF, 50 V	Murata
C17, C18	electrolytic capacitor	1000 μF, 63 V	
P1, P2, P3, P4, P5	copper foil strip	-	needed for tuning
R1, R2	SMD resistor	5.1 Ω	SMD 0805

7.5 Graphical data

All data are measured on the Doherty development test circuit.

7.5.1 CW



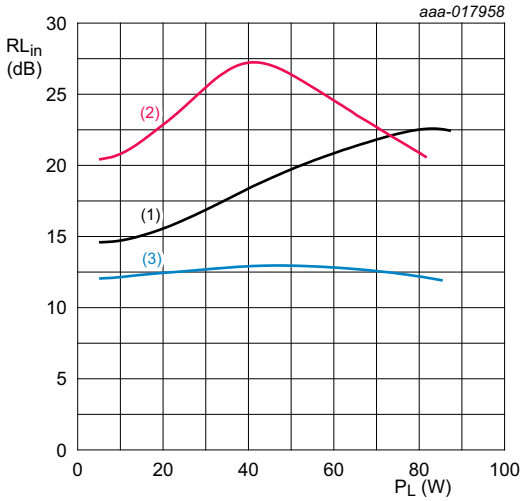
V_{DS} = 28 V; I_{Dq} = 300 mA (main device);
$V_{GS(amp)peak}$ = 0.7 V.

(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 300 mA (main device);
$V_{GS(amp)peak}$ = 0.7 V.

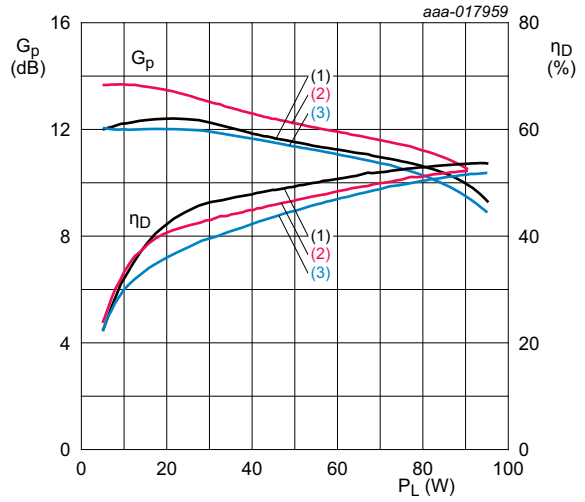
(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 5. Input return loss as a function of output power; typical values

7.5.2 Pulsed CW



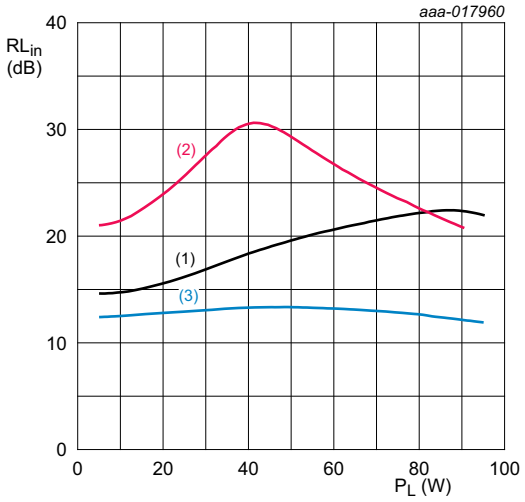
V_{DS} = 28 V; I_{Dq} = 300 mA (main device);
$V_{GS(amp)peak}$ = 0.7 V; t_p = 100 µs; δ = 10 %.

(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 6. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 300 mA (main device);
$V_{GS(amp)peak}$ = 0.7 V; t_p = 100 µs; δ = 10 %.

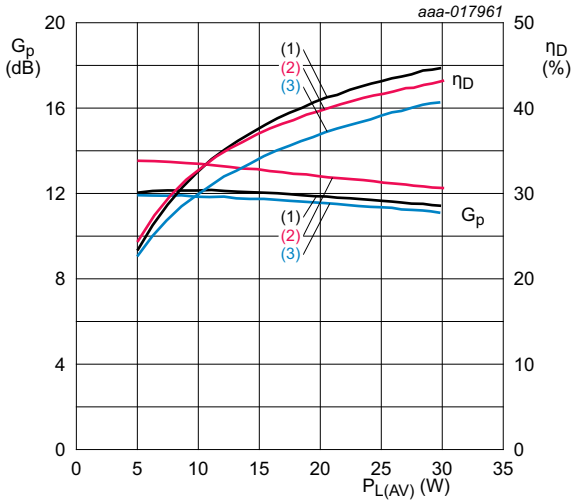
(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 7. Input return loss as a function of output power; typical values

7.5.3 1-Carrier W-CDMA



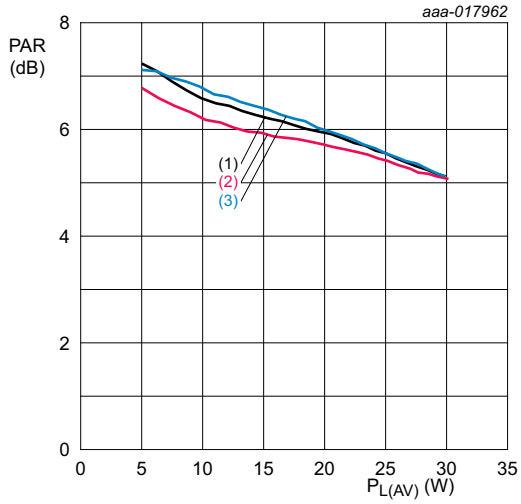
V_{DS} = 28 V; I_{Dq} = 300 mA (main device); $V_{GS(amp)peak}$ = 0.7 V.

(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 8. Power gain and drain efficiency as function of average output power; typical values



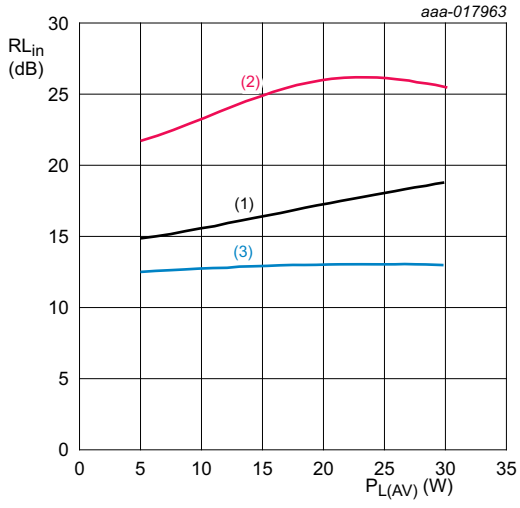
V_{DS} = 28 V; I_{Dq} = 300 mA (main device); $V_{GS(amp)peak}$ = 0.7 V.

(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 9. Peak-to-average power ratio as a function of average output power; typical values



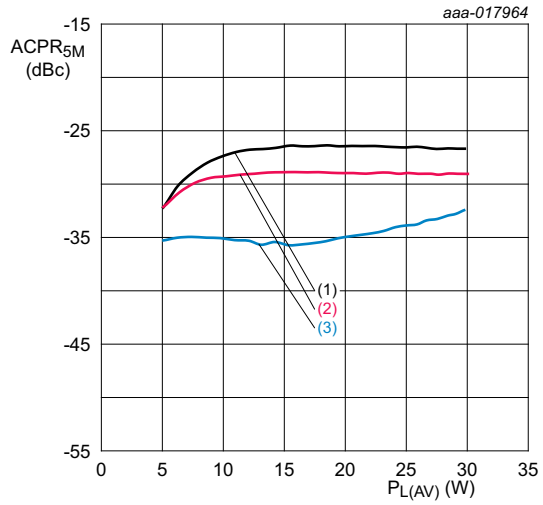
V_{DS} = 28 V; I_{Dq} = 300 mA (main device); $V_{GS(amp)peak}$ = 0.7 V.

(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 10. Input return loss as a function of average output power; typical values



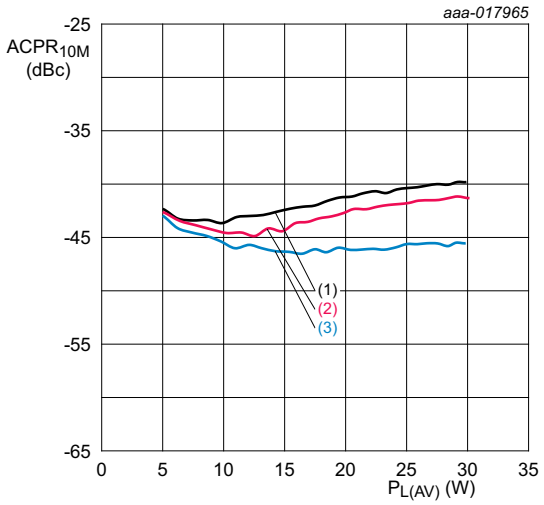
V_{DS} = 28 V; I_{Dq} = 300 mA (main device); $V_{GS(amp)peak}$ = 0.7 V.

(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 11. Adjacent channel power ratio (5 MHz) as a function of average output power; typical values



V_{DS} = 28 V; I_{Dq} = 300 mA (main device); $V_{GS(amp)peak}$ = 0.7 V.

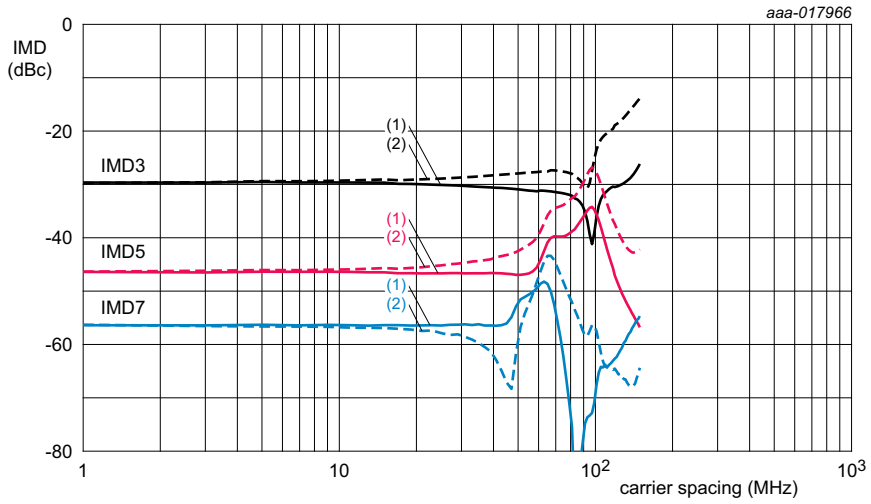
(1) f = 3400 MHz

(2) f = 3500 MHz

(3) f = 3600 MHz

Fig 12. Adjacent channel power ratio (10 MHz) as a function of average output power; typical values

7.5.4 2-Tone VBW



V_{DS} = 28 V; I_{Dq} = 300 mA; f_c = 3500 MHz.

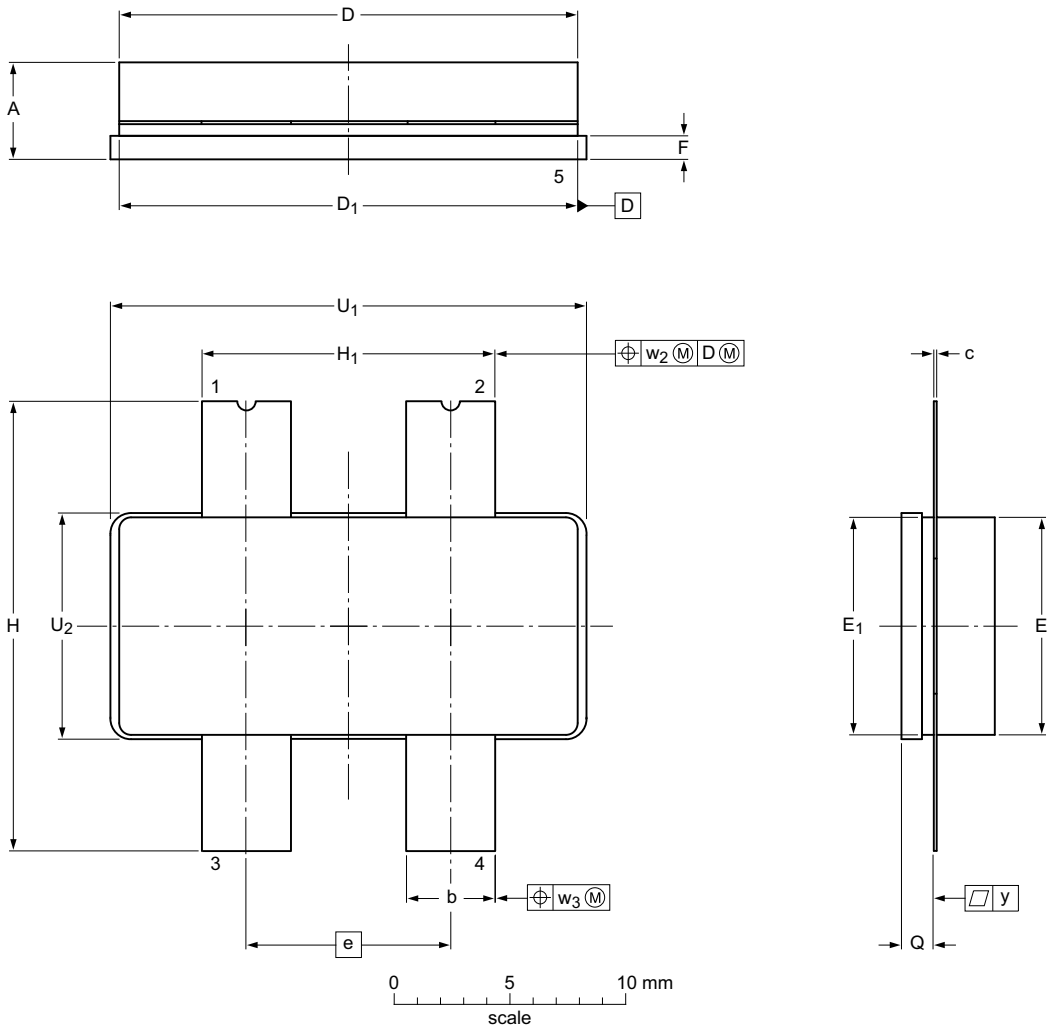
(1) IMD low

(2) IMD high

Fig 13. VBW capability on Doherty development test circuit

8. Package outline

Earless flanged ceramic package; 4 leads **SOT1121B**



Dimensions

Unit[1]		A	b	c	D	D_1	e	E	E_1	F	H	H_1	Q	U_1	U_2	w_2	w_3	y
mm	max	4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	1.70	20.70	9.91	0.51	0.25	0.25
	nom						8.89											
	min	3.45	3.68	0.08	19.61	19.66		9.27	9.27	0.89	18.92	12.57	1.45	20.45	9.65			
inches	max	0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.067	0.815	0.39	0.02	0.01	0.01
	nom						0.35											
	min	0.136	0.145	0.003	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.057	0.805	0.38			

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1121B						~~09-12-14~~ 12-06-07

Fig 14. Package outline SOT1121B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LTE	Long Term Evolution
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF9G38LS-90P v.2	20150703	Product data sheet	-	BLF9G38LS-90P v.1
Modifications:	• Table 1 on page 1; table updated • Table 5 on page 2; table updated • Section 6 on page 3; tables added • Section 7 on page 3; section added			
BLF9G38LS-90P v.1	20141215	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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