Ver 1.1

1.6-Gbps to 2.5-Gbps Radiation-Hardened Transceive

Datasheet

Part Number：BLK2711MQRH

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Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2017.11		Initial release.	
1.1	2018.3		Update format	

TABLE OF CONTENTS

1. Features

- 1.6- to 2.5-Gbps (Gigabits Per Second) Serializer/De-serializer
- Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link
- Interfaces to Backplane, Copper Cables, or Optical Converters
- 16-Bit Parallel LVTTL-Compatible Data Interface
- 3-V Tolerance on Parallel Data Input Signals
- On-Chip PLL Provides Clock Synthesis From Low-Speed Reference
- On-Chip 8-Bit/10-Bit Encoding/Decoding, Comma Detect
- Programmable Pre-emphasis Levels on Serial Output
- Integrated 50-Ω Termination Resistors on RX
- Loss of Signal (LOS) Detection
- Hot-Plug Protection
- Low-Power Operation: <600mW(Frequency = 2.5Gbps, using internal PRBS Generator)
- Military Temperature Range (–55°C to 125°C Tcase)
- Bit Error Rate (BER) <1E-12
- Guaranteed Total Ionizing Dose to 100Krad(Si)
- Latch-up Immune to LET > 75 MeV-cm^2/mg
- High-Performance 68-Pin Ceramic Quad Flat Pack Package (HFG)

2. Applications

- Point-to-Point High Speed I/O
- Data Acquisition
- Data Processing

3. Description

The BLK2711MQRH is a multi-gigabit transceiver, intended for use in ultra-high-speed bidirectional point-to-point data transmission systems. The BLK2711MQRH supports an effective serial interface speed of 1.6Gbps to 2.5Gbps, providing up to 2.0Gbps of data bandwidth.

The primary application of the BLK2711MQRH is to provide high-speed I/O data channels for point-to-point baseband data transmission over controlled impedance media of approximately 50Ω. The transmission media can be printed

circuit board, copper cables, or fiber-optic cable. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector pins, and transmit/receive pins. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel, which can be a coaxial copper cable, a controlled impedance backplane, or an optical link. It is then reconstructed into its original parallel format. It offers significant power and cost savings over parallel solutions, as well as scalability for higher data rates in the future.

The BLK2711MQRH performs parallel-to-serial and serial-to-parallel data conversion. The clock extraction functions as a physical layer (PHY) interface device. The serial transceiver interface operates at a maximum speed of 2.5Gbps. The transmitter latches 16-bit parallel data at a rate based on the supplied reference clock (GTX_CLK). The 16-bit parallel data is internally encoded into 20 bits using an 8-bit/10-bit (8B/10B) encoding format. The resulting 20-bit word is then transmitted differentially at 20 times the reference clock (GTX_CLK) rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel data to the recovered clock (RX_CLK). It then decodes the 20-bit wide data using the 8-bit/10-bit decoding format resulting in 16 bits of parallel data at the receive data pins (RXD0–RXD15). The outcome is an effective data payload of 1.28Gbps to 2Gbps (16 bits data × the frequency).

The BLK2711MQRH provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the de-serializer, providing the protocol device with a functional self-check of the physical interface.

The BLK2711MQRH has a loss of signal (LOS) detection circuit for conditions where the incoming signal no longer has a sufficient voltage amplitude to keep the clock recovery circuit in lock. The BLK2711MQRH allows users to implement redundant ports by connecting receive data bus pins from two BLK2711MQRH devices together. Asserting the LCKREFN to a low state causes the receive data bus pins (RXD0 -RXD15, RX_CLK, RKLSB, and RKMSB) to go to a high-impedance state if device is enabled (ENABLE = H). This places the device in a transmit-only mode, since the receiver is not tracking the data. **LCKREFN must be de-asserted to a high state during power-on reset.** See **Power-On Reset**. If device is disabled (ENABLE = L), then RKMSB will output the status of the LOS detector (active low =

LOS). All other receive outputs will remain high-impedance.

The BLK2711MQRH I/Os are 3-V compatible. The BLK2711MQRH is characterized for operation from –55°C to 125°C Tcase.

The BLK2711MQRH is designed to be hot-plug capable. An on-chip power-on reset circuit holds the RX_CLK low, and goes to high impedance on the parallel-side output signal pins, as well as DOUTTXP and DOUTTXN during power up.

The BLK2711MQRH is available in a 68-pin ceramic nonconductive tie-bar package (HFG).

4. Pin Configuration and Functions

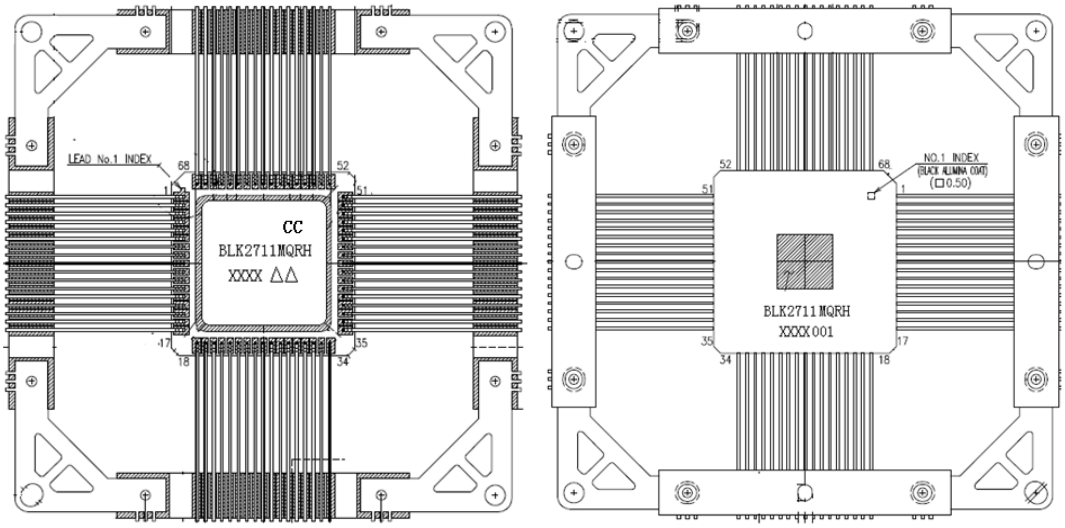


Figure 1 HFG PACKAGE Top View& Bottom View

Table 1 Pin Functions

PIN NAME	NO	I/O	DESCRIPTION
VDD	1, 9, 24, 40,50	POWER	Digital logic power. Provides power for all digital circuitry and digital I/O buffers.
VDDA	59, 61	POWER	Analog power. VDDA provides a supply reference for the high-speed analog circuits, receiver and transmitter.
GND	5, 13, 17, 19, 24,59, 35,14, 35,55, 58, 62, 65	GND	Analog and digital logic ground. Provides a ground for the logic circuits, digital I/O buffers, and the high-speed analog circuits.
TXD0~TXD15	66,67,68, 2,3,4,6,7, 10,11,12,14, 15,16,18,20	I	Transmit data bus. These inputs carry the 16-bit parallel data output from a protocol device to the transceiver for encoding, serialization, and transmission. This 16-bit parallel data is clocked into the transceiver on the rising edge of GTX_CLK as shown in Figure 3.

TKLSB	23	I	K-code generator (LSB). When TKLSB is high, an 8-bit/10-bit K code is transmitted as controlled by data bits TXD0–TXD7. When TKLSB is low, an 8-bit/10-bit D code is transmitted as controlled by data bits TXD0–TXD7.
TKMSB	21	I	K-code generator (MSB). When TKMSB is high, an 8-bit/10-bit K code is transmitted as controlled by data bits TXD8–TXD15. When TKMSB is low, an 8-bit/10-bit D code is transmitted as controlled by data bits TXD8–TXD15.
GTX_CLK	8	I	Reference clock. GTX_CLK is a continuous external input clock that synchronizes the transmitter interface signals TKMSB, TKLSB, and TXD0–TXD15. The frequency range of GTX_CLK is 80 MHz to 125 MHz. The transmitter uses the rising edge of this clock to register the 16-bit input data TXD0–TXD15 for serialization.
RXD0~RXD15	54,53,52 49,48,47,46, 44,42,41,39, 38,37,36,33, 32	O	Receive data bus. These outputs carry 16-bit parallel data output from the transceiver to the protocol device, synchronized to RX_CLK. The data is valid on the rising edge of RX_CLK as shown in Figure 6. These pins are in high-impedance state during power-on reset.
RKLSB	30	O	K-code indicator/PRBS test results. When RKLSB is asserted high, an 8-bit/10-bit K code was received and is indicated by data bits RXD0-RXD7. When RKLSB is asserted low, an 8-bit/10-bit D code is received and is presented on data bits RXD0-RXD7. When PRBSEN is asserted high, this pin is used to indicate status of the PRBS test results (high = pass).

RKMSB	31	O	K-code indicator. When RKMSB is asserted high an 8-bit/10-bit K code was received and is indicated by data bits RXD8–RXD15. When RKMSB is asserted low an 8-bit/10-bit D code was received and is indicated by data bits RXD8-RXD15. If the differential signal on DINRXN and DINRXP drops below 200mV. RXD0-RXD15, RKLSB, and RKMSB are all asserted high. When device is disabled (ENABLE = L), RKMSB will output the status of LOS. Active low =LOS detected.
RX_CLK	43	O	Recovered clock. Output clock that is synchronized to RXD0-RXD15, RKLSB, and RKMSB. RX_CLK is the recovered serial data rate clock divided by 20. RX_CLK is held low during power-on reset.
DOUTTXP DOUTTXN	64 63	O	Serial transmit outputs. DOUTTXP and DOUTTXN are differential serial outputs that interface to copper or an optical I/F module. These pins transmit NRZ data at a rate of 20 times the GTX_CLK value. DOUTTXP and DOUTTXN are put in a high-impedance state when LOOPEN is high and are active when LOOPEN is low. During power-on reset, these pins are high impedance.
DINRXP DINRXN	57 56	I	Serial receive inputs. DINRXP and DINRXN together are the differential serial input interface from a copper or an optical I/F module.

ENABLE	25	I	Device enable. When this pin is held low, the device is placed in power-down mode. Only the signal detect circuit on the serial receive pair is active. When in power down mode, RKMSB will output the status of signal detect circuit (LOS). When asserted high while the device is in power-down mode, the transceiver goes into power-on reset before beginning normal operation.
LCKREFN	26	I	Lock to reference. When LCKREFN is low, the receiver clock is frequency locked to GTX_CLK. This places the device in a transmit-only mode since the receiver is not tracking the data. When LCKREFN is asserted low, the receive data bus pins (RXD0 - RXD15, RX_CLK, RKLSB, and RKMSB) are in high-impedance state if device is enabled (ENABLE = H). If device is disable (ENABLE = L) the RKMSB will output the status of the LOS detector (active low= LOS). All other receive outputs will remain high-impedance. When LCKREFN is de-asserted high, the receiver is locked to the received data stream. LCKREFN must be de-asserted to a high state during power-on reset. See **Power-On Reset**.

LOOPEN	22	I	Loop enable. When LOOPEN is active high, the internal loopback path is activated. The transmitted serial data is directly routed internally to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The DOUTTXP and DOUTTXN outputs are held in a high-impedance state during the loopback test. LOOPEN is held low during standard operational state, with external serial outputs and inputs active.
PRE	60	I	Pre-emphasis control. Selects the amount of pre-emphasis to be added to the high-speed serial output drivers. Left low or unconnected, 5% pre-emphasis is added. Pulled high, 20% pre-emphasis is added.
PRBSEN	27	I	PRBS test enable. When asserted high, results of pseudo-random bit stream (PRBS) tests can be monitored on the RKLSB pin. A high on RKLSB indicates that valid PRBS is being received.
TESTEN	28	I	Test mode enable. This pin should be left unconnected or tied low.

5. Detailed Description

5.1 Overview

The following sections describe block by block features and operation of the BLK2711MQRH transceiver.

5.2 Functional Block Diagram

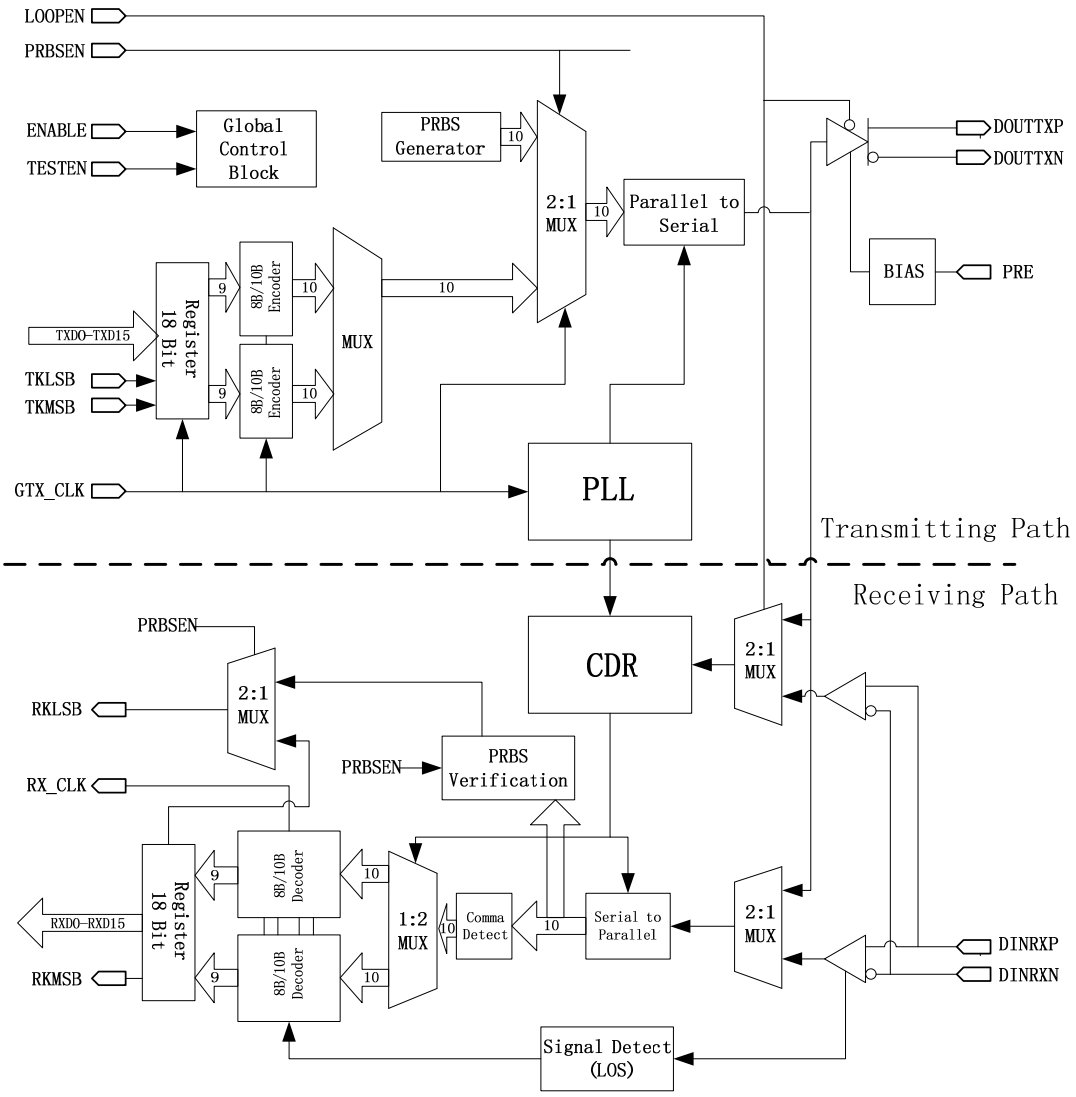


Figure 2 Functional Block Diagram

6. Feature Description

6.1 Transmit Interface

The transmitter interface registers valid incoming 16-bit-wide data (TXD0–TXD15) on the rising edge of the GTX_CLK. The data is then 8-bit/10-bit encoded, serialized, and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the reference clock (GTX_CLK) by a factor of 10 times, creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register, which transmits data on both the rising and falling edges of the bit clock, providing a serial data rate that is 20 times the reference clock. Data is transmitted least significant bit (LSB) (TXD0) first.

6.2 Transmit Data Bus

The transmit data bus interface accepts 16-bit single-ended TTL parallel data at the TXD0–TXD15 pins. Data and K-code control is valid on the rising edge of the GTX_CLK. The GTX_CLK is used as the word clock. The data, K code, and clock signals must be properly aligned as shown in Figure 3. Detailed timing information can be found in the electrical characteristics table.

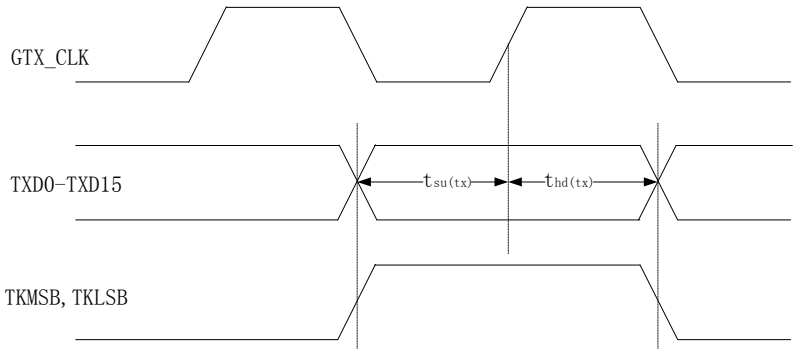


Figure 3 Transmit Timing Waveform

6.3 Data Transmission Latency

The data transmission latency of the BLK2711MQRH is defined as the delay from the initial 16-bit word load to the serial transmission of bit 0. The transmit latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum transmit latency td (Tx latency) is 34 bit times; the maximum is 38 bit times. Figure 4 shows the timing relationship between the transmit data bus, the GTX_CLK, and the serial transmit pins.

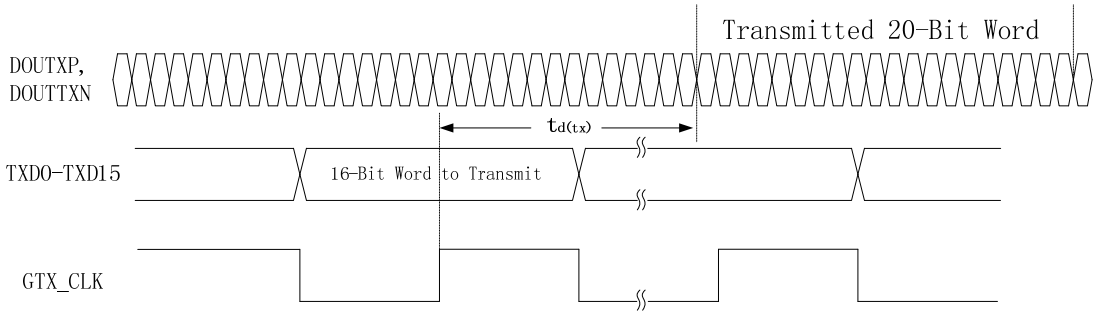


Figure 4 Transmitter Latency

6.4 8-Bit/10-Bit Encoder

All true serial interfaces require a method of encoding to ensure minimum transition density, so that the receiving phase-locked loop (PLL) has a minimal number of transitions to stay locked on. The encoding scheme maintains the signal dc balance by keeping the number of ones and zeros the same. This provides good transition density for clock recovery and improves error checking. The BLK2711MQRH uses the 8-bit/10-bit encoding algorithm that is used by fiber channel and gigabit ethernet. This is transparent to the user, as the BLK2711MQRH internally encodes and decodes the data such that the user reads and writes actual 16-bit data.

The 8-bit/10-bit encoder converts 8-bit-wide data to a 10-bit-wide encoded data character to improve its transmission characteristics. Since the BLK2711MQRH is a 16-bit-wide interface, the data is split into two 8-bit-wide bytes for encoding. Each byte is fed into a separate encoder. The encoding is dependent upon two additional input signals, TKMSB and TKLSB.

Table 2 Transmit Data Controls

TKLSB	TKMSB	16 BIT PARALLEL INPUT
0	0	Valid data on TXD0 to TXD7 Valid data TXD8 to TXD15
0	1	Valid data on TXD0 to TXD7 K code on TXD8 to TXD15
1	0	K code on TXD0 to TXD7 Valid data on TXD8 to TXD15
1	1	K code on TXD0 to TXD7 K code on TXD8 to TXD15

6.5 Pseudo-Random Bit Stream (PRBS) Generator

The BLK2711MQRH has a built-in 2^7–1 PRBS function. When the PRBSEN pin is forced high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel-to-serial converter input register. Data from the normal input source is ignored during the PRBS mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a bit error rate tester (BERT), the receiver of another BLK2711MQRH, or looped back to the receive input. Since the PRBS is not really random but a

predetermined sequence of ones and zeroes, the data can be captured and checked for errors by a BERT.

6.6 Parallel to Serial

The parallel-to-serial shift register takes in the 20-bit-wide data word multiplexed from the two parallel 8-bit/10-bit encoders and converts it to a serial stream. The shift register is clocked on both the rising and falling edge of the internally generated bit clock, which is 10 times the GTX_CLK input frequency. The LSB (TXD0) is transmitted first.

6.7 High-Speed Data Output

The high-speed data output driver consists of a voltage mode logic (VML) differential pair optimized for a 50-Ωimpedance environment. The magnitude of the differential pair signal swing is compatible with pseudo emitter coupled logic (PECL) levels when ac coupled. The line can be directly coupled or ac coupled. See Figure 13 and Figure 14 for termination details. The outputs also provide pre-emphasis to compensate for ac loss when driving a cable or PCB backplane trace over a long distance (see Figure 5). The level of pre-emphasis is controlled by PRE (see Table 3).

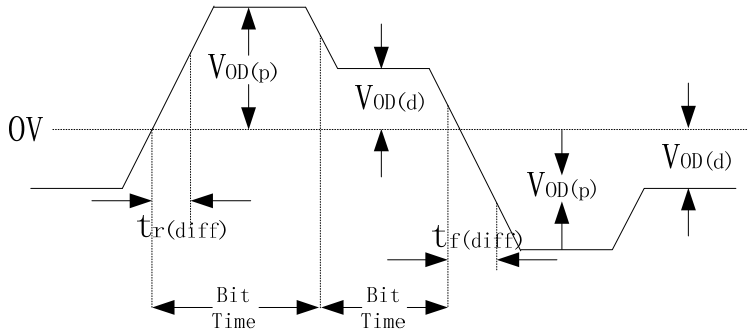


Figure 5 **Output Voltage Under Preemphasis (VTXP–VTXN)**

Table 3 Programmable Preemphasis

PRE	PREEMPHASIS LEVEL (%) VOD(p), VOD(d)(1)
0	5%
1	20%

(1)VOD(p): Voltage swing when there is a transition in the data

stream.

VOD(d): Voltage swing when there is no transition in the data stream.

6.8 Receive Interface

The receiver interface of the BLK2711MQRH accepts 8-bit/10-bit encoded differential serial data. The interpolator and clock recovery circuit locks to the data stream and extracts the bit-rate clock. This recovered clock is used to retime the input data stream. The serial data is then aligned to two separate 10-bit word boundaries, 8-bit/10-bit decoded, and output on a 16-bit-wide parallel bus synchronized to the extracted receive clock. The data is received LSB (RXD0) first.

6.9 Receive Data Bus

The receive bus interface drives 16-bit-wide single-ended TTL parallel data at the RXD0–RXD15 pins. Data is valid on the rising edge of the RX_CLK. The RX_CLK is used as the recovered word clock. The data, RKLSB, RKMSB, and clock signals are aligned as shown in Figure 6. Detailed timing information can be found in the switching characteristics table.

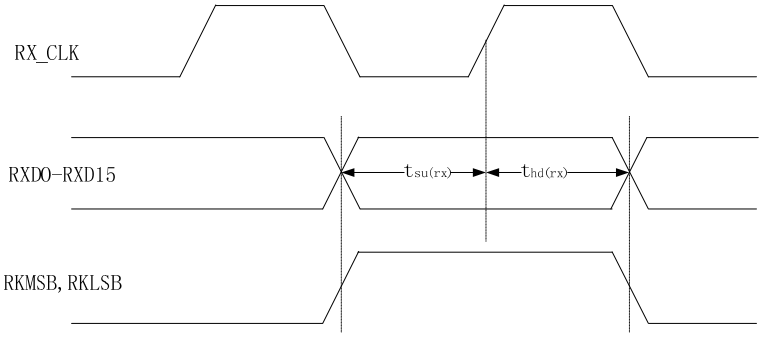


Figure 6 **Receive Timing Waveform**

6.10 Data Reception Latency

The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum receive latency td(Rx latency) is 76 bit times; the maximum is 107 bit times. Figure 7 shows the timing relationship between

the serial receive pins, the recovered word clock (RX_CLK), and the receive data bus.

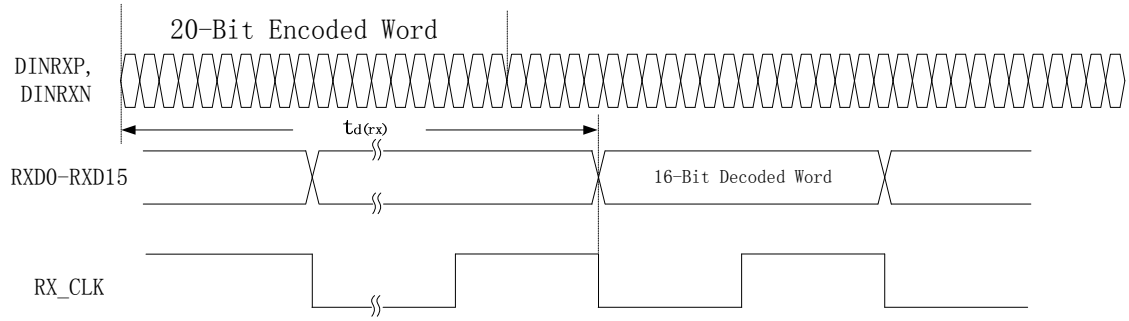


Figure 7 **Receiver Latency**

6.11 Serial to Parallel

Serial data is received on the DINRXP and DINRXN pins. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within 200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. The 10-bit-wide parallel data is then multiplexed and fed into two separate 8-bit/10-bit decoders, where the data is then synchronized to the incoming data stream word boundary by detection of the comma 8-bit/10-bit synchronization pattern.

6.12 Comma Detect and 8-Bit/10-Bit Decoding

The BLK2711MQRH has two parallel 8-bit/10-bit decode circuits. Each 8-bit/10-bit decoder converts 10-bit encoded data (half of the 20-bit received word) back into eight bits. The comma-detect circuit is designed to provide for byte synchronization to an 8-bit/10-bit transmission code. When parallel data is clocked into a parallel-to-serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to recognize the byte boundary. Typically, this is accomplished through the use of a synchronization pattern. This is typically a unique pattern of ones and zeros that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. The 8-bit/10-bit encoding contains a character called the comma (b0011111 or b1100000), which is used by the comma-detect circuit on the BLK2711MQRH to align the received serial data back to its original byte boundary. The decoder detects the comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding; the

comma is mapped into the LSB. The decoder then converts the data back into 8-bit data. The output from the two decoders is latched into the 16-bit register synchronized to the recovered parallel data clock (RX_CLK) and output valid on the rising edge of the RX_CLK.

NOTE

The BLK2711MQRH only achieves byte alignment on the 0011111 comma.

Decoding provides two additional status signals, RKLSB and RKMSB. When RKLSB is asserted, an 8-bit/10-bit K code is received and the specific K code is presented on the data bits RXD0–RXD7; otherwise, an 8-bit/10-bit D code is received. When RKMSB is asserted, an 8-bit/10-bit K code is received and the specific K-code is presented on data bits RXD8–RXD15; otherwise, an 8-bit/10-bit D code is received (see Table 4). The valid K codes the BLK2711MQRH decodes are provided in Table 5. An error detected on either byte, including K codes not in Table 5, causes that byte only to indicate a K0.0 code on the RKxSB and associated data pins, where K0.0 is known to be an invalid 8-bit/10-bit code. A loss of input signal causes a K31.7 code to be presented on both bytes, where K31.7 is also known to be an invalid 8-bit/10-bit code.

Table 4 Receive Status Signals

RKLSB	RKMSB	DECODED 20-BIT OUTPUT
0	0	Valid data on RXD0 to RXD7 Valid data RXD8 to RXD15
0	1	Valid data on RXD0 to RXD7 K code on RXD8 to RXD15
1	0	K code on RXD0 to RXD7 Valid data on RXD8 to RXD15
1	1	K code on RXD0 to RXD7 K code on RXD8 to RXD15

Table 5 Valid K Characters

K CHARACTER	RECEIVE DATA BUS RXD0 to RXD7 OR RXD8 to RXD15
K28.0	000 11100

K28.1(1)	001 11100
K28.2	010 11100
K28.3	011 11100
K28.4	100 11100
K28.5(1)	101 11100
K28.6	110 11100
K28.7(1)	111 11100
K23.7	111 10111
K27.7	111 11011
K29.7	111 11101
K30.7	111 11110

(1) Should only be present on RXD0–RXD7 when in running disparity<0

6.13 Loss of Signal (LOS) Detection

The BLK2711MQRH has a LOS detection circuit for conditions where the incoming signal no longer has a sufficient voltage level to keep the clock recovery circuit in lock. The signal detection circuit is intended to be an indication of gross signal error conditions, such as a detached cable or no signal being transmitted, and not an indication of signal coding health. The BLK2711MQRH reports this condition by asserting RKLSB, RKMSB, and RXD0–RXD15 pins to a high state. As long as the differential signal is above 200mV in differential magnitude, the LOS circuit does not signal an error condition. When the device is disabled (ENABLE = L), RKMSB will output the status of LOS. Active low = LOS detected.

6.14 PRBS Verification

The BLK2711MQRH also has a built-in BERT function in the receiver side that is enabled by the PRBSEN. It can check for errors and report the errors by forcing the RKLSB pin low.

6.15 Reference Clock Input

The reference clock (GTX_CLK) is an external input clock that synchronizes the transmitter interface. The reference clock is then multiplied in frequency 10 times to produce the internal serialization bit clock. The internal serialization bit clock is

frequency locked to the reference clock and used to clock out the serial transmit data on both its rising and falling edges, providing a serial data rate that is 20 times the reference clock.

6.16 Operating Frequency Range

The BLK2711MQRH operates at a serial data rate from 1.6Gbps to 2.5Gbps. To achieve these serial rates, GTX_CLK must be within 80MHz to 125MHz. The GTX_CLK must be within ±100 PPM of the desired parallel data rate clock.

6.17 Testability

The BLK2711MQRH has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable pin allows for all circuitry to be disabled so that a quiescent current test can be performed. The PRBS function allows for built-in self-test (BIST).

6.18 Loopback Testing

The transceiver can provide a self-test function by enabling (LOOPEN) the internal loopback path. Enabling this pin causes serial-transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. The external differential output is held in a high-impedance state during the loopback testing.

6.19 Built-In Self-Test (BIST)

The BLK2711MQRH has a BIST function. By combining PRBS with loopback, an effective self-test of all the circuitry running at full speed can be realized. The successful completion of the BIST is reported on the RKLSB pin.

6.20 Power-On Reset

Upon application of minimum valid power and valid GTX_CLK with device enabled (ENABLE = HIGH), the BLK2711MQRH generates a power-on reset. During the power-on reset the RXD0 to RXD15, RKLSB, and RKMSB signal pins go to a high-impedance state. The RXCLK is held low. LCKREFN must be deasserted (logic high state) with active transitions on the receiver during the power-on reset

period. Active transitions on receiver can be accomplished with transitions on RXP/N or by assertion of LOOPEN. For TX-only applications, LOOPEN and LCKREFN can be driven logic high together. The receiver circuit requires this to properly reset. After power-up reset period, LCKREFN can be asserted for transmit only applications. The length of the power-on reset cycle depends on the GTX_CLK frequency, but is less than 1 ms. See Figure 8 . TI recommends that the receiver be reset immediately after power up. In some conditions, it is possible for the receiver circuit to power up in state with internal contention.

If LCKREFN cannot be deasserted high during or for the complete power-on reset period, it can be deasserted high at the end of or after the power-on reset period for minimum of 1 μS with active transitions on receiver to properly complete reset of receiver.

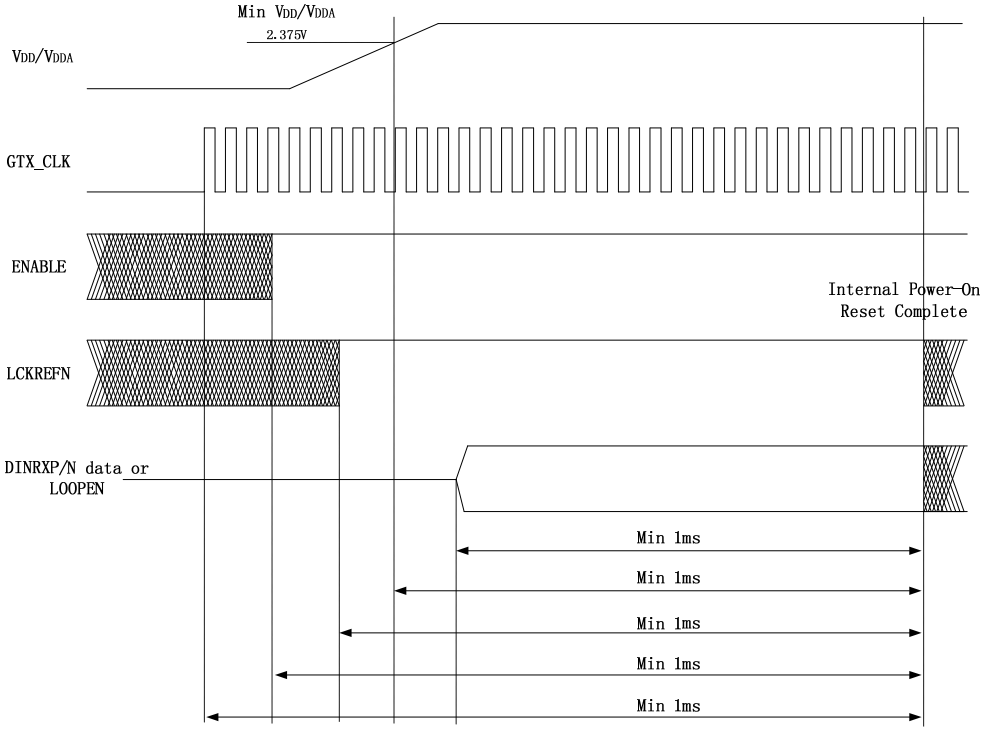


Figure 8 **Power-On Reset Timing Diagram**

7. Specifications

7.1 Absolute Maximum Ratings

Over operating temperature (unless otherwise noted)(1).

PARAMETER		MIN	MAX	UNIT
V_{DD}/V_{DDA}	Supply voltage (2)	–0.3	3	V

Voltage	TXD0 to TXD15, ENABLE, GTX_CLK, TKMSB, TKLSB, LOOPEN, PRBSEN, LCKREFN, PRE, TESTEN	–0.3	4	V
	RXD0 to RXD15, RKMSB, RKLSB, RX_CLK	-0.3V	V_{DD} +0.35	V
	DINRXP, DINRXN, DOUTTXP, DOUTTXN	-0.35V	V_{DDA} +0.35	V
	Maximum cumulative exposure of unpowered receiver to external inputs(3)	—	10	hours
T_C	Characterized case operating temperature	–55	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are stated with respect to network ground.

(3) The BLK2711MQRH shows no performance degradation when an external powered transmitter sends a signal to an unpowered receiver for short periods of time (up to 10 hours of life time of the device). Characterization was performed using maximum V_{OD}, minimum frequency and typical V_{CMT} from recommended operating conditions for the specified period of time.

7.2 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD}/V_{DDA}	Supply voltage	Frequency range 1.6Gbps to 2Gbps	2.375	2.5	2.7	V

		Frequency range 2.0Gbps to 2.5Gbps	2.5	2.6	2.7	V
I_{DD}	Supply current	Frequency = 1.6Gbps, using internal PRBS Generator	—	130	140	mA
		Frequency = 2.5Gbps, using internal PRBS Generator	—	210	222	mA
I_{SHD}	Shutdown current	ENABLE=0, V_{DD}=V_{DDA}=2.7V	—	—	4.5	mA
t_{lck}	PLL startup lock time	V_{DD}=V_{DDA}=2.375V	—	0.1	0.4	ms
	Data acquisition time		—	1024	—	bits
T_C	Operating case temperature		–55	—	125	°C

7.3 ESD Ratings

PARAMETER		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge, Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information(1)

THERMAL METRIC		VALUE	UNIT
RθJC	Junction-to-case thermal resistance	3.5	°C/W

(1) This CFP package has built in vias that electrically and thermally connect the bottom of the die to a pad on the bottom of the package. In order to efficiently remove heat and provide a low-impedance ground path, a thermal land is required on the surface of the PCB directly underneath the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package is soldered to this thermal land creating an efficient thermal path. Normally, the PCB thermal land has a number of thermal vias

within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. We typically recommend an 11,9-mm x 11.9-mm board-mount thermal pad with a 4,2-mm x 4,2-mm solder mask defined pad attach opening. This allows maximum area for thermal dissipation, while allowing leads pad to solder pad clearance. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically ground potential.

7.5 TTL Input Electrical Characteristics

Over recommended operating conditions (unless otherwise noted).
TTL signals: TXD0–TXD15, GTX_CLK, LOOPEN, LCKREFN, ENABLE, PRBSEN, TKLSB, TKMSB, PRE.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	See Figure 9	1.7	—	—	V
V_{IL}	Low-level input voltage	See Figure 9	—	—	0.8	V
I_{IH}	Input high current	Input pins without internal pull-up or pull-down(TXD0-TXD15, GTX_CLK), V_{DD}=2.7V, V_{IN}=2.0V, at 25°C	-200	—	200	nA
		Input pins without internal pull-up or pull-down(TXD0-TXD15, GTX_CLK), V_{DD}=2.7V, V_{IN}=2.0V, -55°C~+125°C	-4	—	4	μA
		Input pins with internal pull-up or pull-down(ENABLE, LCKREFN, TKLSB, TKMSB, PRBSEN, LOOPEN, PRE, TESTEN), V_{DD}=2.7V, V_{IN}=2.0V, -55°C~+125°C	-40	—	40	μA

I_{IL}	Input low current	Input pins without internal pull-up or pull-down(TXD0-TXD15, GTX_CLK), V_{DD}=2.7V, V_{IN}=0.4V, at 25°C	-200	—	200	nA
		Input pins without internal pull-up or pull-down(TXD0-TXD15, GTX_CLK), V_{DD}=2.7V, V_{IN}=0.4V, -55°C~+125°C	-4	—	4	μA
		Input pins with internal pull-up or pull-down(ENABLE, LCKREFN, TKLSB, TKMSB, PRBSEN, LOOPEN, PRE, TESTEN), V_{DD}=2.7V, V_{IN}=0.4V, -55°C~+125°C	-40	—	40	μA
$t_{r(tx)}$(1)	Rise time, GTX_CLK, TKMSB, TKLSB, TXD0 to TXD15	0.7V-1.9V, See Figure 9	—	1	—	ns
$t_{f(tx)}$(1)	Fall time, GTX_CLK, TKMSB, TKLSB, TXD0 to TXD15	1.9V- 0.7V, See Figure 9	—	1	—	ns
$t_{su(tx)}$	TXD0 to TXD15, TKMSB, TKLSB setup to ↑ GTX_CLK	See Figure 9	1.5	—	—	ns
$t_{hd(tx)}$	TXD, TKMSB, TKLSB hold to ↑ GTX_CLK	See Figure 9	0.4	—	—	ns

(1) Nonproduction tested parameters

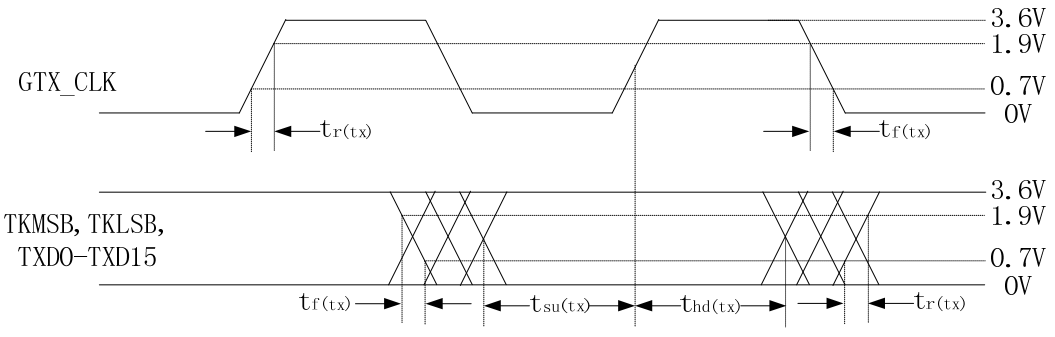


Figure 9 TTL Data Input Valid Levels for AC Measurements

7.6 Transmitter/Receiver Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(p)}$	Preemphasis VOD, direct, VOD(p) = |VTXP – VTXN|	Rt = 50Ω, PREM = high, DC coupled, See Figure 10	655	800	1150	mV
		Rt = 50Ω, PREM = low, DC coupled, See Figure 10	590	750	1050	mV
$V_{OD(pp-p)}$	Differential, peak-to-peak output voltage with preemphasis	Rt = 50Ω, PREM = high, DC coupled, See Figure 10	1310	1600	2300	mV
		Rt = 50Ω, PREM = low, DC coupled, See Figure 10	1180	1500	2100	mV
$V_{OD(d)}$	Deemphais output voltage, VOD(d) =|VTXP – VTXN|	Rt = 50Ω, DC coupled, See Figure 10	540	650	950	mV
$V_{OD(pp-d)}$	Differential, peak-to-peak output voltage with deemphasis	Rt = 50Ω, DC coupled, See Figure 10	1080	1300	1900	mV
V_{CMT}	Transmit common mode voltage range, (VTXP+ VTXN) / 2	Rt =50Ω,DC coupled, See Figure 10	1000	1250	1400	mV
V_{CMR}	Receiver common mode voltage range, (VRXP+ VRXN) / 2		1000	1250	2250	mV
V_{ID}	Receiver input voltage differential, |VRXP – VRXN|		220	—	1600	mV
I_{LKG}	Receiver input leakage current		-10	—	10	uA

$t_{r(diff)}$	Differential output signal rise time (20% to 80%)	R_L =50Ω, See Figure 10	—	—	200	ps
$t_{f(diff)}$	Differential output signal fall time (80% to 20%)	R_L =50Ω, See Figure 10	—	—	200	ps
J_{out}	Serial data total jitter (peak to peak)	Differential output jitter at 2.5Gbps, Random + deterministic, using internal PRBS Generator	—	—	112	ps
		Differential output jitter at 1.6Gbps, Random + deterministic, using internal PRBS Generator	—	—	200	ps
J_{tol}	Jitter tolerance eye closure	Differential input jitter, random + deterministic, PRBS pattern at zero crossing	0.4	—	—	UI(2)
$t_{d(tx)}$	Tx latency	See Figure 4	34	—	38	Bits
$t_{d(rx)}$	Rx latency	See Figure 7	76	—	107	Bits

(1) UI is the time interval of one serialized bit

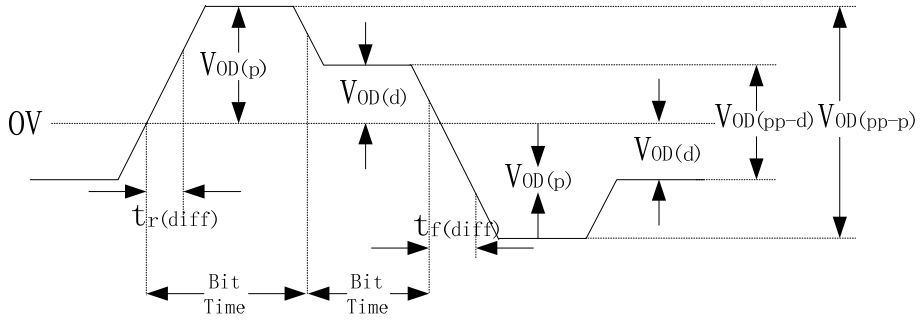


Figure 10 Differential and Common-Mode Output Voltage

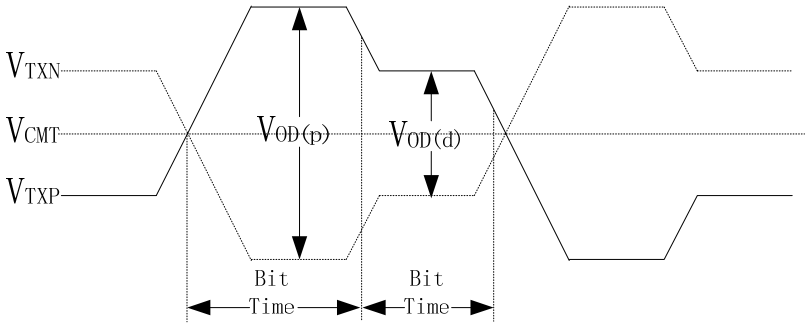


Figure 11 Common-Mode Output Voltage Definitions

7.7 TTL Output Switching Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD}=2.3V, I_{OH}=-2mA	2.1	—	—	V
V_{OL}	Low-level output voltage	V_{DD}=2.3V, I_{OL}=+2mA	—	—	0.5	V
$t_{r(rx)}$	Rising time, magnitude of RX_CLK, RKLSB, RKMSB, RXD0 to RXD15	0.8V-2.0V, See Figure 12	—	—	2.4	ns
$t_{f(rx)}$	Falling time, magnitude of RX_CLK, RKLSB, RKMSB, RXD0 to RXD15	2. 0V-0.8V, See Figure 12	—	—	2.4	ns
$t_{su(rx)}$	RXD0 to RXD15, RKMSB, RKLSB setup to ↑ RX_CLK	GTX_CLK=80MHz, See Figure 12	3.0	—	—	ns
		GTX_CLK=125MHz, See Figure 12	2.5	—	—	ns
$t_{hd(rx)}$	RXD0 to RXD15, RKMSB, RKLSB hold to ↑ RX_CLK	GTX_CLK=80MHz, See Figure 12	3.0	—	—	ns
		GTX_CLK=125MHz, See Figure 12	2.0	—	—	ns

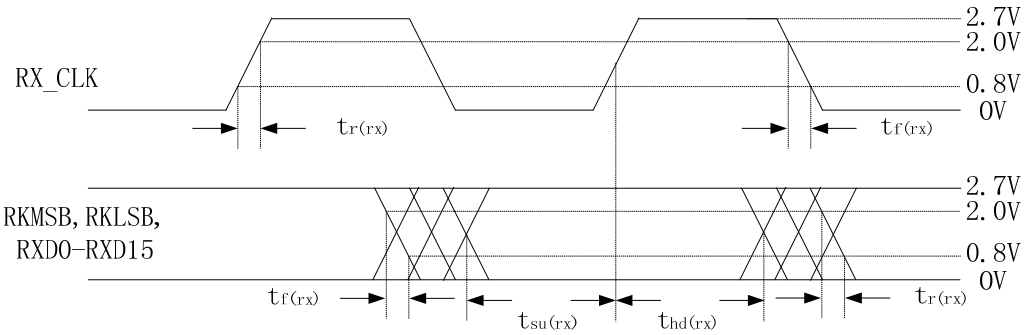


Figure 12 TTL Data Output Valid Levels for AC Measurements

7.8 Reference Clock (GTX_CLK) Timing Requirements

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency tolerance		-100	—	100	ppm
Duty cycle		40%	50%	60%	
Jitter	Peak to peak			40	ps

8. Device Functional Modes

8.1 Power-Down Mode

The BLK2711MQRH goes into power-down mode when the ENABLE pin is pulled low. In the power-down mode, the serial transmit pins (DOUTTXN), the receive data bus pins (RXD0–RXD15), and RKLSB goes into a high-impedance state. In the power-down condition, the signal detection circuit draws less than 15mW. When the BLK2711MQRH is in the power-down mode, the clock signal on the GTX_CLK pin must be provided if LOS functionality is needed.

8.2 High-Speed I/O Directly-Coupled Mode

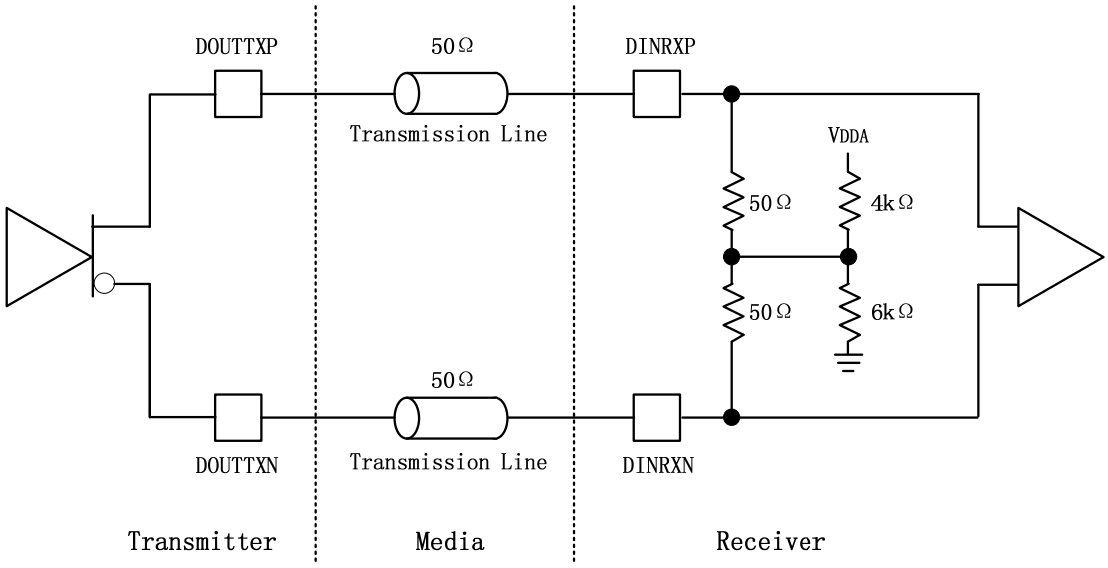


Figure 13 High-Speed I/O Directly-Coupled Mode

8.3 High-Speed I/O AC-Coupled Mode

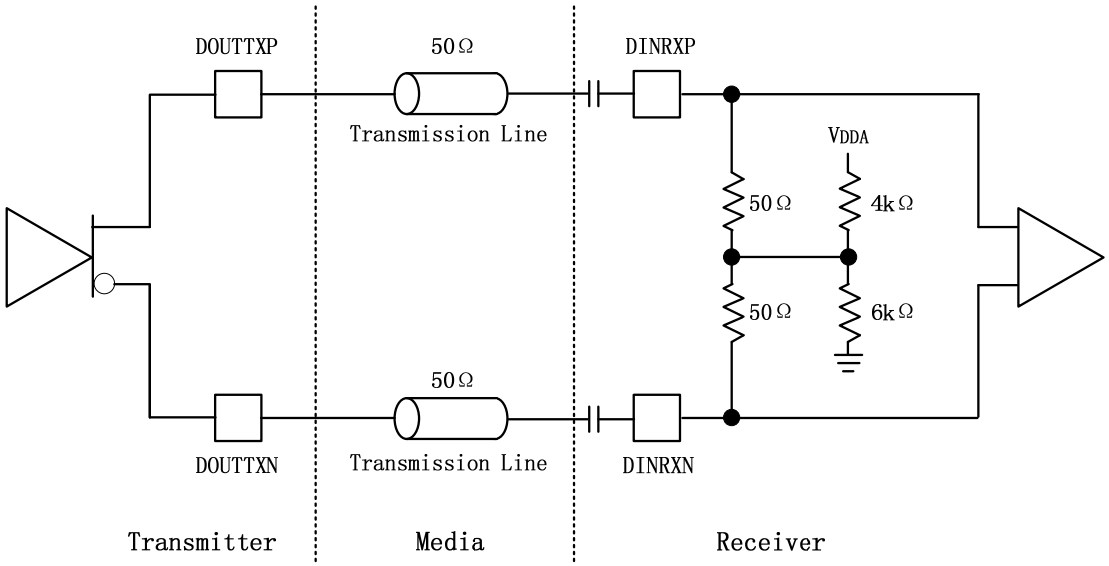


Figure 14 High-Speed I/O AC-Coupled Mode

9. Application and Implementation

NOTE

Information in the following applications sections is not part of the BMTI component specification, and BMTI does not warrant its accuracy or completeness. BMTI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The BLK2711MQRH may be operated as full link with send/receive functions or each end of link may be transmit only or receive only. The transmitter is always operational in either case as GTX_CLK is required to source the PLL. In transmit only cases, LCKREFN can be pulled low to disable the RX interface. See **Power-On Reset** for requirements.

9.2 Typical Applications

9.2.1 External Component Interconnection

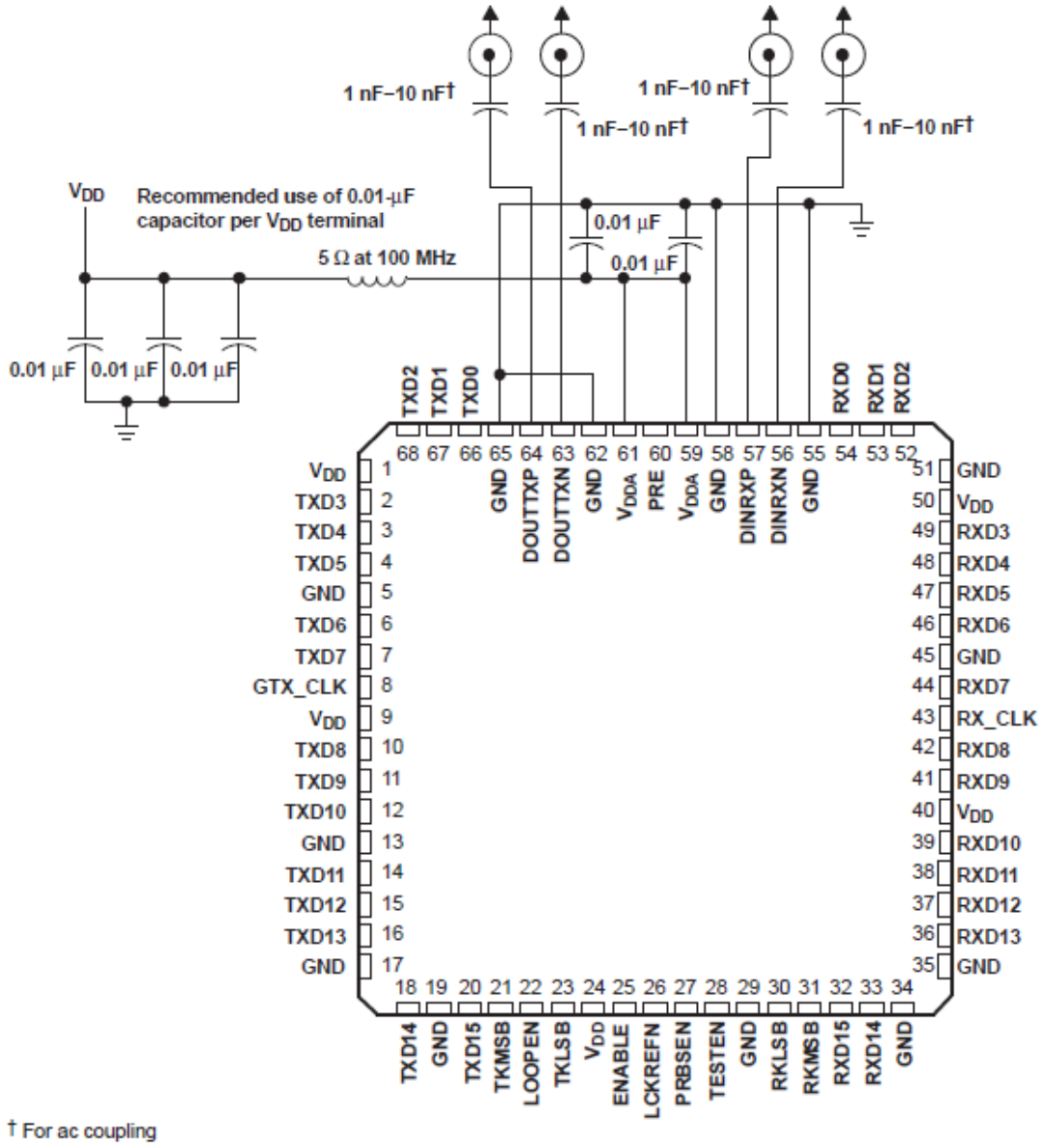


Figure 15 External Component Interconnection

9.2.2 Design Requirements

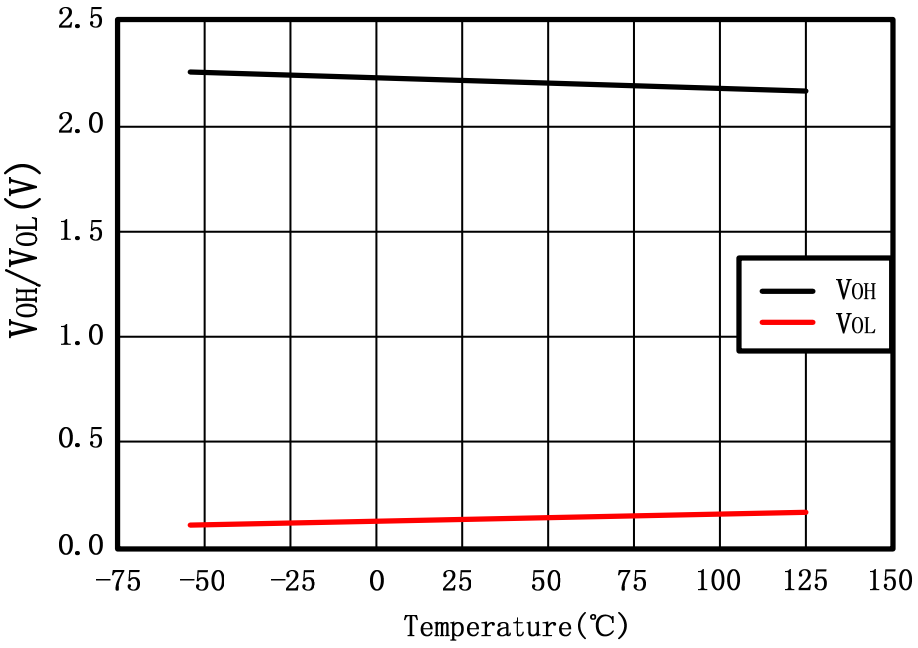
Input conditions in the data sheet were created and validated to achieve a bit error rate (BER) of 1 error in 1E12 bits or better. Other aspects that affect BER are power supply noise, quality (loss), and matching of 50-Ω controlled impedance for transmit and receive differential pins.

9.2.3 Detailed Design Procedure

Detailed design procedures involve careful examination of system properties, design, and error rate goals. Understanding these properties allows for creation of jitter budget to insure design BER goals are achieved.

9.2.4 Application Curves

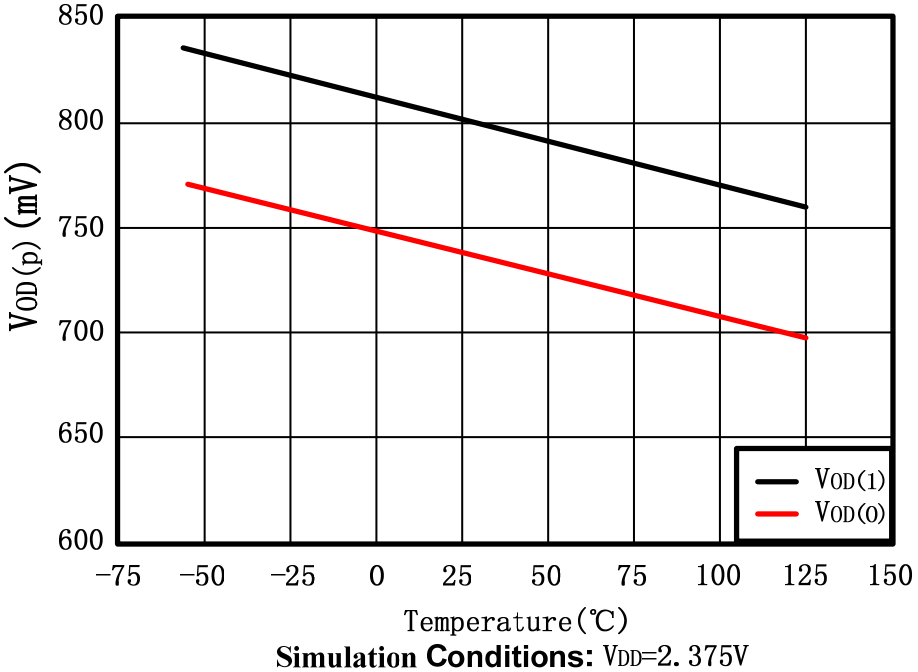
Figure 16 shows the simulation result of TTL output voltage at maximum 2-mA load across temperature at minimum V_{DD} = 2.375 V.



Simulation Conditions: V_{DD}=2.375V, I_{OH}/I_{OL}=±2mA

Figure 16 V_{OH}/V_{OL} vs Temperature

Figure 17 shows the simulation result of differential output voltage $V_{OD(p)}$ across temperature for each pre-emphasis condition at minimum V_{DD} = 2.375 V. $V_{OD(1)}$ represents 20% emphasis enabled. $V_{OD(0)}$ represents 5% emphasis enabled.



Simulation Conditions: V_{DD}=2.375V

Figure 17 **$V_{OD\,(0)}$, $V_{OD\,(1)}$ vs Temperature**

10. Power Supply Recommendations

Power supplies must be within recommended operating range and should have less than 100-mV of ripple. Exceeding 100-mV ripple can impact transmitted jitter and receiver jitter tolerance.

VDDA should be filtered from VDD. Filter values should be set to minimize any frequency components from power supply and/or digital logic that may exist in the system in the range of the PLL jitter transfer characteristics. The PLL is sensitive to noise in the range of 300KHz to 3MHz.

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