

BLL8H1214L-500; BLL8H1214LS-500

LDMOS L-band radar power transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

500 W LDMOS power transistor intended for L-band radar applications in the 1.2 GHz to 1.4 GHz range.

Table 1. Test information

Typical RF performance at $T_{case} = 25\text{ °C}$; $t_p = 300\text{ }\mu\text{s}$; $\delta = 10\%$; $I_{Dq} = 150\text{ mA}$; in a class-AB production test circuit.

Test signal	f (GHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η_D (%)	t _r (ns)	t _f (ns)
pulsed RF	1.2 to 1.4	50	500	17	50	20	6

1.2 Features and benefits

- Easy power control
- Integrated dual side ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1.2 GHz to 1.4 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- L-band power amplifiers for radar applications in the 1.2 GHz to 1.4 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLL8H1214L-500 (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLL8H1214LS-500 (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLL8H1214L-500	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLL8H1214LS-500	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{GS}	gate-source voltage		-6	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_{case} = 85\text{ °C}; P_L = 500\text{ W}$		
		$t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.046	K/W
		$t_p = 200\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.059	K/W
		$t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.069	K/W
		$t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.064	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.7\text{ mA}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 270\text{ mA}$	1.3	1.8	2.2	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	32	42	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 270\text{ mA}$	1.7	3	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 9.5\text{ A}$	-	100	164	$\text{m}\Omega$

Table 7. RF characteristics

Test signal: pulsed RF; $t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$; RF performance at $V_{DS} = 50\text{ V}; I_{DQ} = 150\text{ mA}$; $T_{case} = 25\text{ °C}$; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$P_L = 500\text{ W}$	-	-	50	V
G_p	power gain	$P_L = 500\text{ W}$	15	17	-	dB
RL_{in}	input return loss	$P_L = 500\text{ W}$	-	-10	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		-	600	-	W
η_D	drain efficiency	$P_L = 500\text{ W}$	45	50	-	%
$P_{droop(pulse)}$	pulse droop power	$P_L = 500\text{ W}$	-	0	0.3	dB
t_r	rise time	$P_L = 500\text{ W}$	-	20	50	ns
t_f	fall time	$P_L = 500\text{ W}$	-	6	50	ns

7. Test information

7.1 Ruggedness in class-AB operation

The BLL8H1214L-500 and BLL8H1214LS-500 are capable of withstanding a load mismatch corresponding to $V_{SWR} = 10 : 1$ through all phases under the following conditions: $V_{DS} = 50\text{ V}; I_{DQ} = 150\text{ mA}; P_L = 500\text{ W}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$.

7.2 Impedance information

Table 8. Typical impedance

Typical values per section unless otherwise specified.

f (GHz)	Z _S (Ω)	Z _L (Ω)
1.2	1.268 – j2.623	2.987 – j1.664
1.3	2.193 – j2.457	2.162 – j1.326
1.4	2.359 – j2.052	1.604 – j1.887

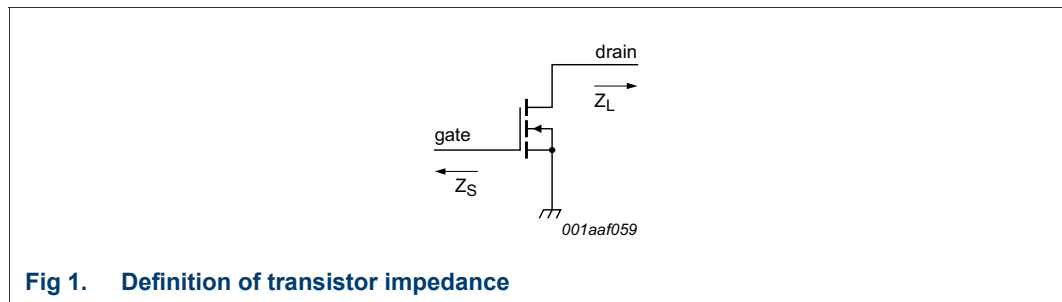


Fig 1. Definition of transistor impedance

7.3 Test circuit

Table 9. List of components

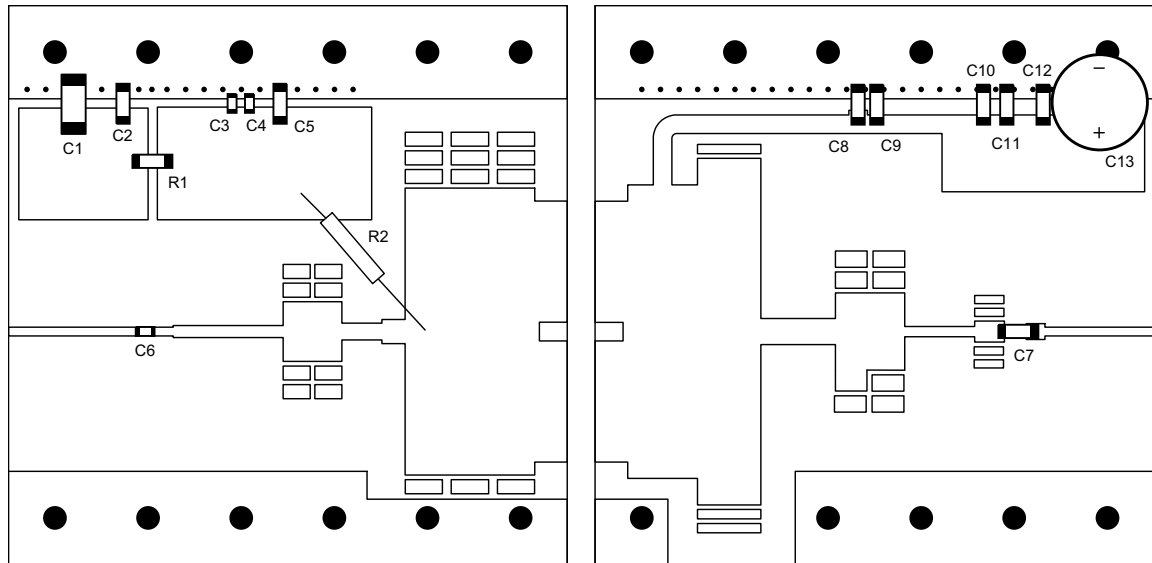
For test circuit see [Figure 2](#).

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	22 μF, 35 V	
C2	multilayer ceramic chip capacitor	51 pF	[1]
C3, C4	multilayer ceramic chip capacitor	100 pF	[1]
C5, C11, C12	multilayer ceramic chip capacitor	1 nF	[2]
C6	multilayer ceramic chip capacitor	47 pF	[1]
C7, C8, C10	multilayer ceramic chip capacitor	51 pF	[3]
C9	multilayer ceramic chip capacitor	100 pF	[3]
C13	electrolytic capacitor	10 μF, 63 V	
R1	SMD resistor	56 Ω	SMD 0603
R2	metal film resistor	51 Ω	

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 800B or capacitor of same quality.



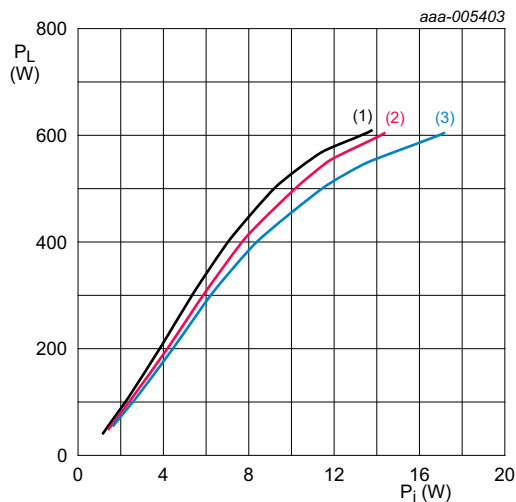
001aaj490

Printed-Circuit Board (PCB): Duroid 6006; $\epsilon_r = 6.15$ F/m; thickness = 0.64 mm; thickness copper plating = 35 μ m.
See [Table 9](#) for a list of components.

Fig 2. Component layout for class-AB production test circuit

7.4 RF performance graphs

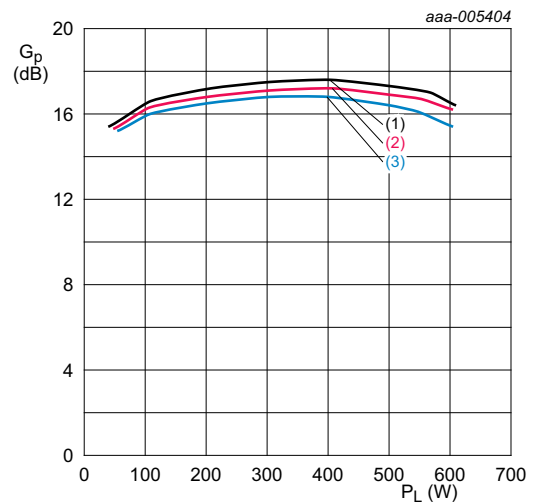
7.4.1 Performance curves measured with $\delta = 10\%$, $t_p = 300 \mu$ s and $T_h = 25 \text{ }^\circ\text{C}$



$V_{DS} = 50 \text{ V}$; $I_{Dq} = 150 \text{ mA}$.

- (1) $f = 1200 \text{ MHz}$
- (2) $f = 1300 \text{ MHz}$
- (3) $f = 1400 \text{ MHz}$

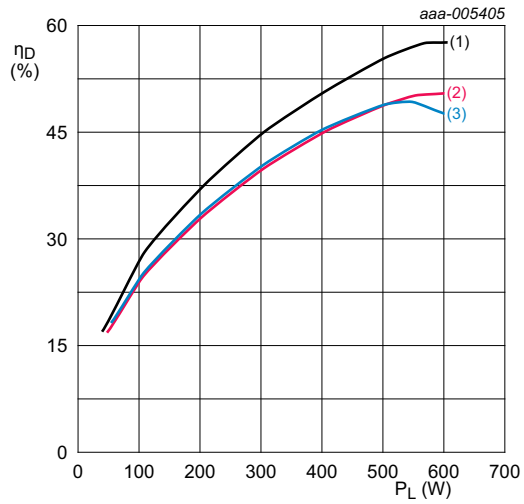
Fig 3. Output power as a function of input power; typical values



$V_{DS} = 50 \text{ V}$; $I_{Dq} = 150 \text{ mA}$.

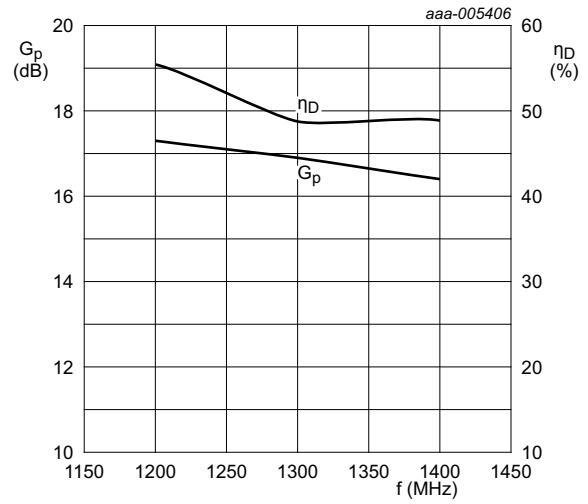
- (1) $f = 1200 \text{ MHz}$
- (2) $f = 1300 \text{ MHz}$
- (3) $f = 1400 \text{ MHz}$

Fig 4. Power gain as a function of output power; typical values



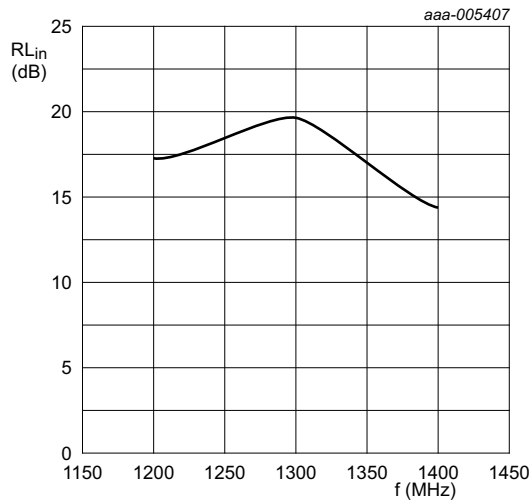
$V_{DS} = 50$ V; $I_{Dq} = 150$ mA.
 (1) $f = 1200$ MHz
 (2) $f = 1300$ MHz
 (3) $f = 1400$ MHz

Fig 5. Drain efficiency as a function of output power; typical values



$V_{DS} = 50$ V; $P_L = 500$ W; $I_{Dq} = 150$ mA.

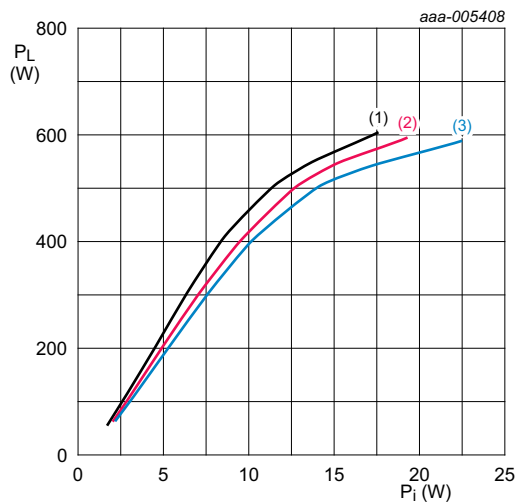
Fig 6. Power gain and drain efficiency as function of frequency; typical values



$V_{DS} = 50$ V; $P_L = 500$ W; $I_{Dq} = 150$ mA.

Fig 7. Input return loss as a function of frequency; typical value

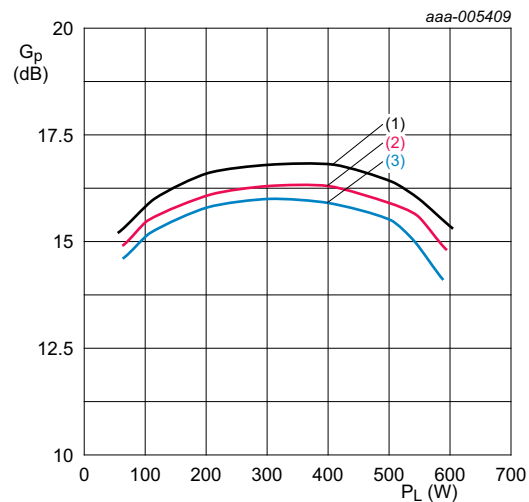
7.4.2 Performance curves measured with $\delta = 10\%$, $t_p = 300 \mu s$ and $T_h = 65^\circ C$



$V_{DS} = 50 V$; $I_{Dq} = 150 mA$.

- (1) $f = 1200 MHz$
- (2) $f = 1300 MHz$
- (3) $f = 1400 MHz$

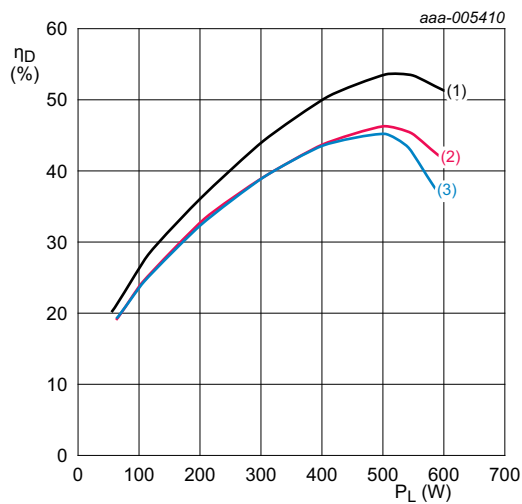
Fig 8. Output power as a function of input power; typical values



$V_{DS} = 50 V$; $I_{Dq} = 150 mA$.

- (1) $f = 1200 MHz$
- (2) $f = 1300 MHz$
- (3) $f = 1400 MHz$

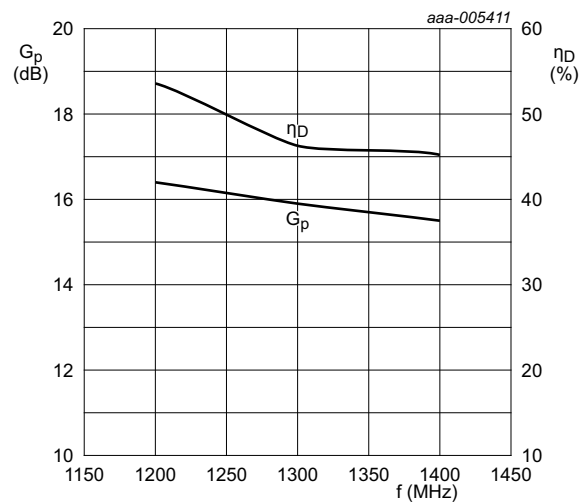
Fig 9. Power gain as a function of output power; typical values



$V_{DS} = 50 V$; $I_{Dq} = 100 mA$.

- (1) $f = 1200 MHz$
- (2) $f = 1300 MHz$
- (3) $f = 1400 MHz$

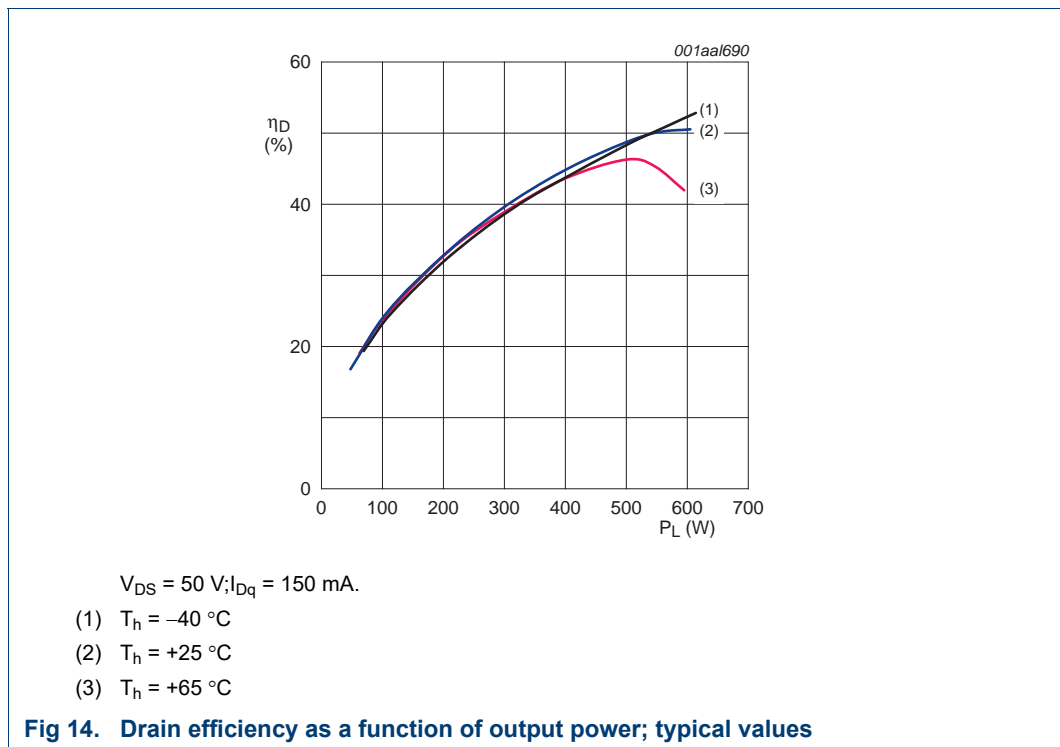
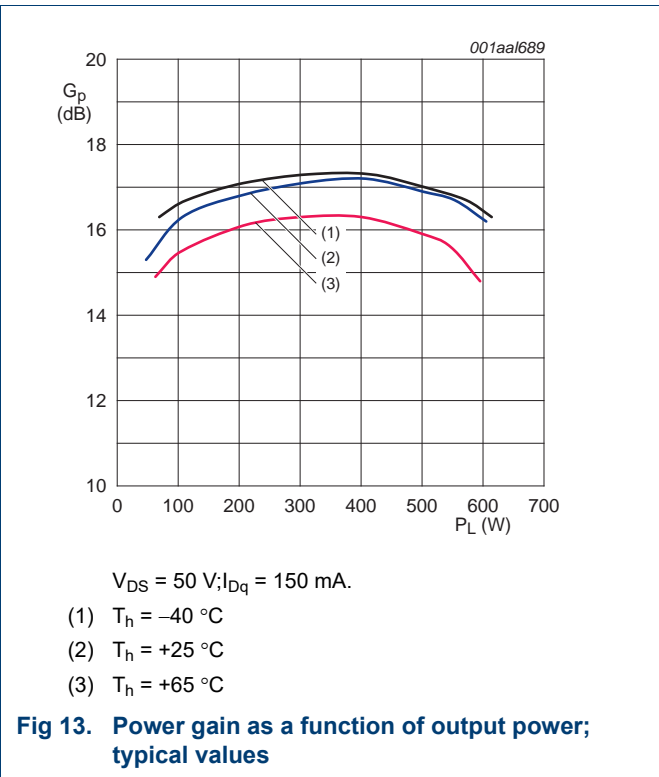
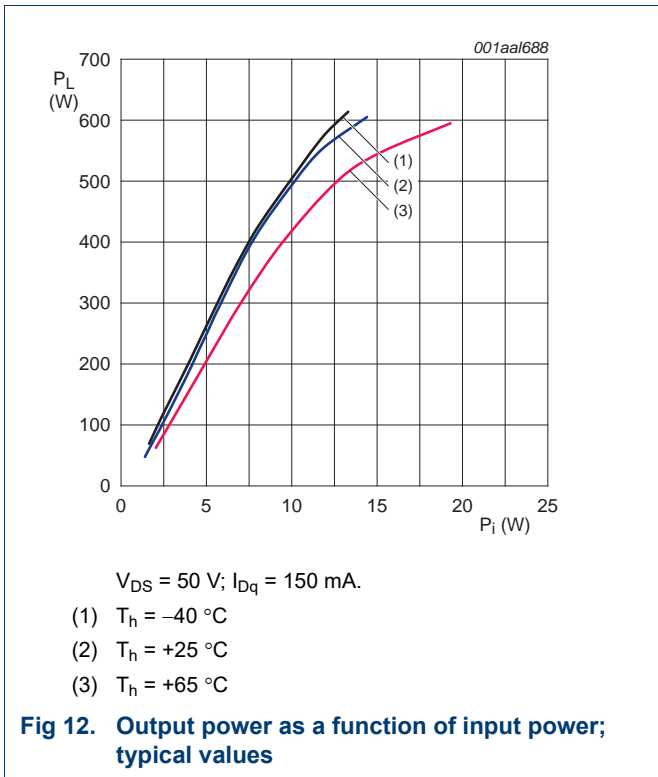
Fig 10. Drain efficiency as a function of output power; typical values



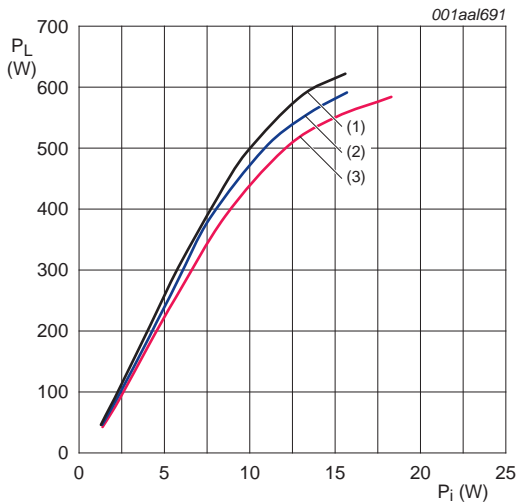
$V_{DS} = 50 V$; $P_L = 500 W$; $I_{Dq} = 100 mA$.

Fig 11. Power gain and drain efficiency as function of frequency; typical values

7.4.3 Performance curves measured with $\delta = 10\%$, $t_p = 300\ \mu\text{s}$ and $f = 1300\ \text{MHz}$

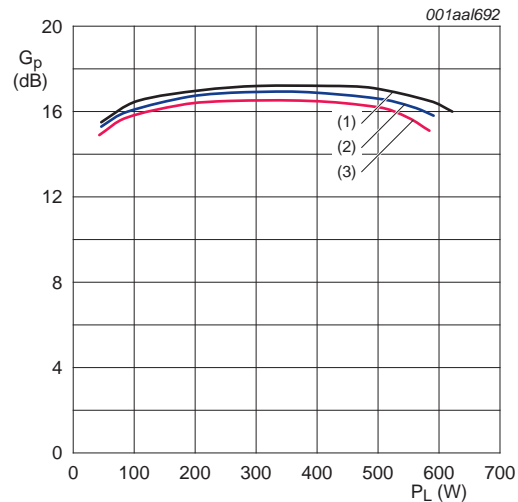


7.4.4 Performance curves measured with $\delta = 20\%$, $t_p = 500 \mu s$ and $T_h = 25^\circ C$



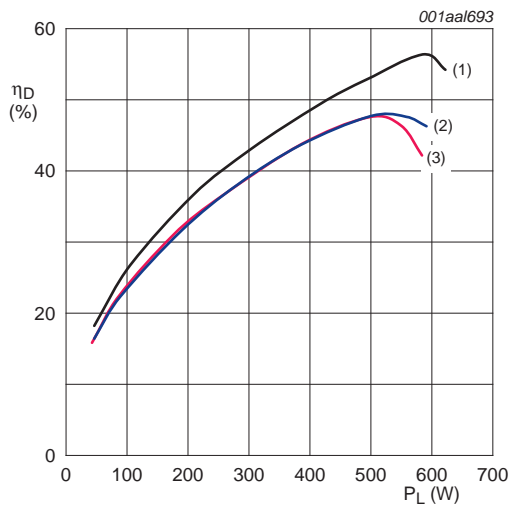
$V_{DS} = 50 V$; $I_{Dq} = 150 mA$.
 (1) $f = 1200 MHz$
 (2) $f = 1300 MHz$
 (3) $f = 1400 MHz$

Fig 15. Output power as a function of input power; typical values



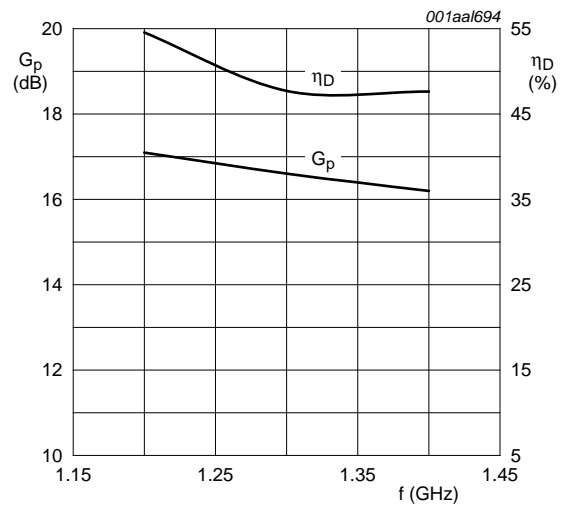
$V_{DS} = 50 V$; $I_{Dq} = 150 mA$.
 (1) $f = 1200 MHz$
 (2) $f = 1300 MHz$
 (3) $f = 1400 MHz$

Fig 16. Power gain as a function of output power; typical values



$V_{DS} = 50 V$; $I_{Dq} = 150 mA$.
 (1) $f = 1200 MHz$
 (2) $f = 1300 MHz$
 (3) $f = 1400 MHz$

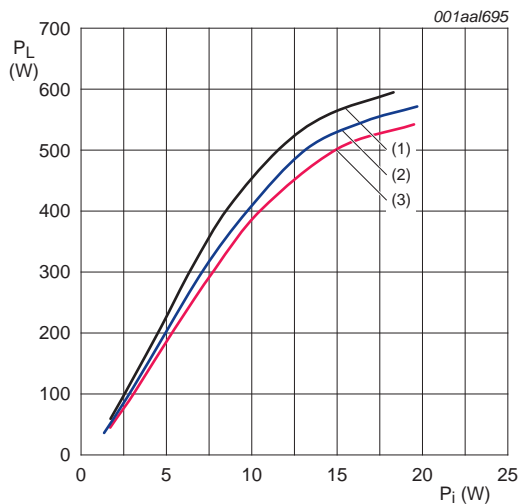
Fig 17. Drain efficiency as a function of output power; typical values



$V_{DS} = 50 V$; $I_{Dq} = 150 mA$.

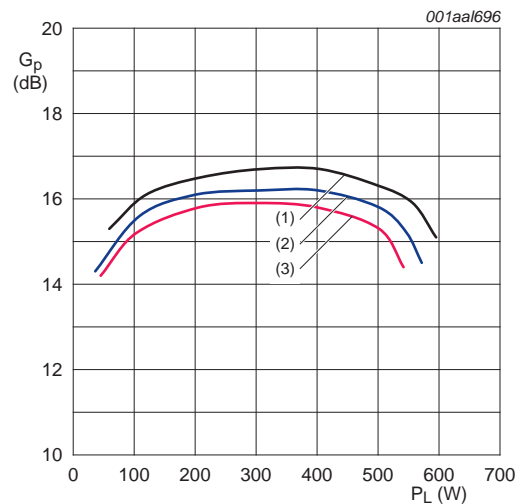
Fig 18. Power gain and drain efficiency as function of frequency; typical values

7.4.5 Performance curves measured with $\delta = 20\%$, $t_p = 500 \mu s$ and $T_h = 65^\circ C$



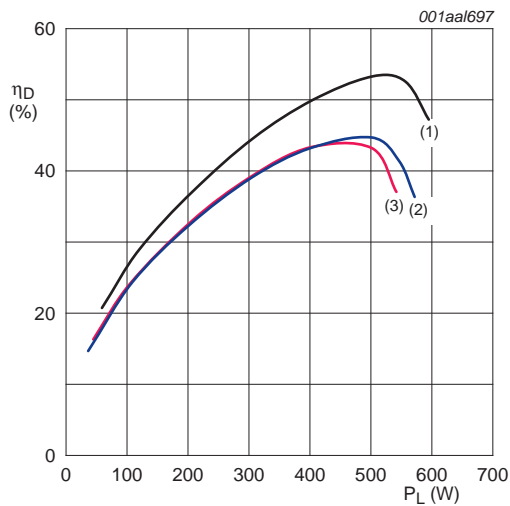
$V_{DS} = 50 V$; $I_{Dq} = 150 mA$.
 (1) $f = 1200 MHz$
 (2) $f = 1300 MHz$
 (3) $f = 1400 MHz$

Fig 19. Output power as a function of input power; typical values



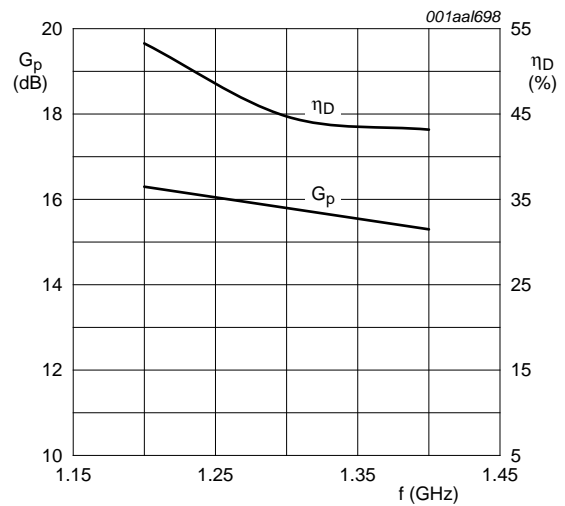
$V_{DS} = 50 V$; $I_{Dq} = 150 mA$.
 (1) $f = 1200 MHz$
 (2) $f = 1300 MHz$
 (3) $f = 1400 MHz$

Fig 20. Power gain as a function of output power; typical values



$V_{DS} = 50 V$; $I_{Dq} = 150 mA$.
 (1) $f = 1200 MHz$
 (2) $f = 1300 MHz$
 (3) $f = 1400 MHz$

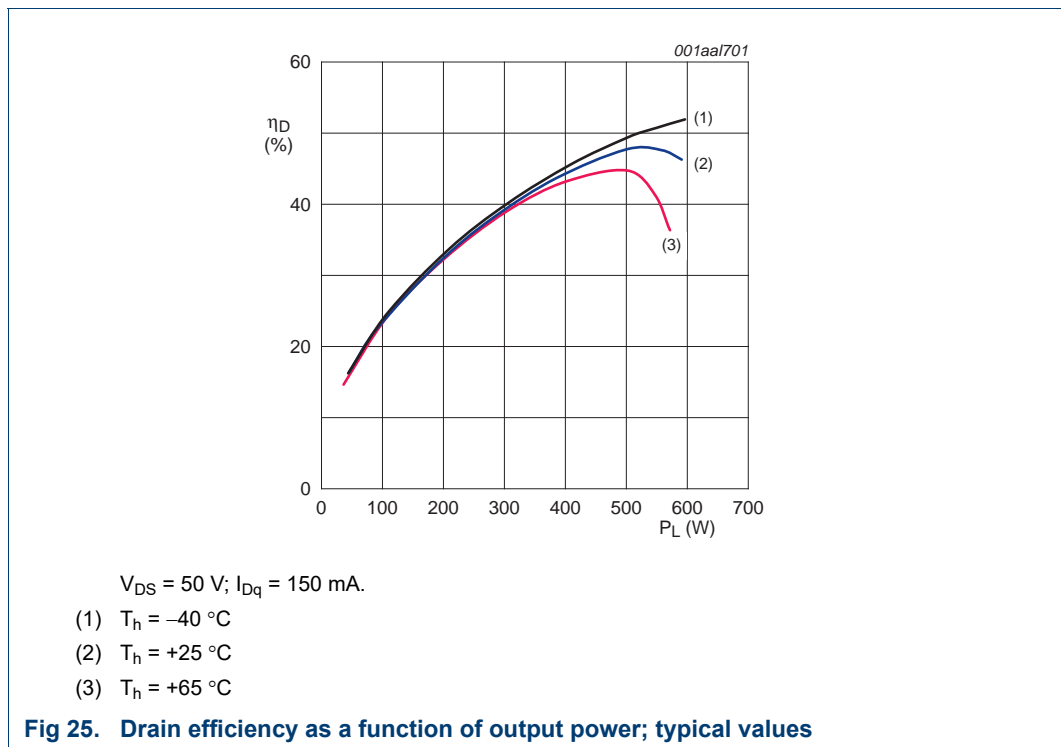
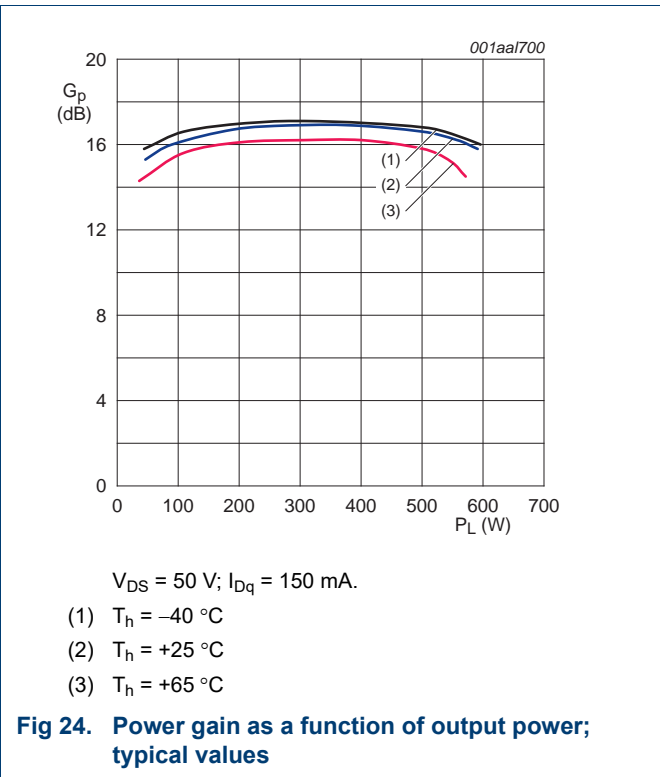
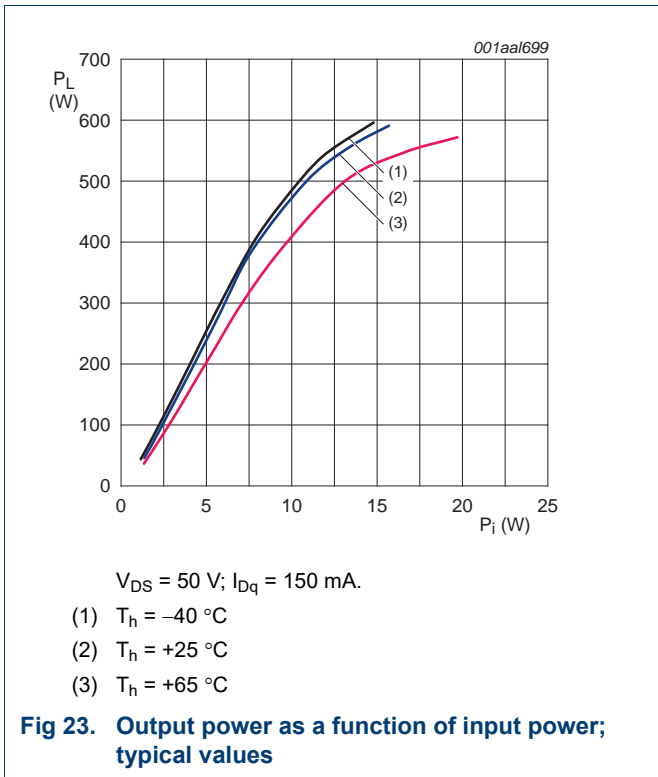
Fig 21. Drain efficiency as a function of output power; typical values



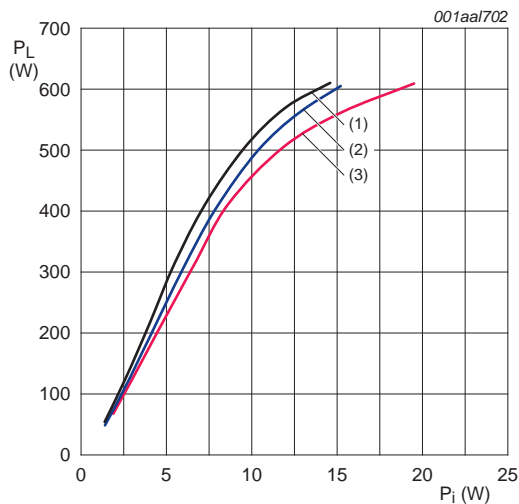
$V_{DS} = 50 V$; $I_{Dq} = 150 mA$.

Fig 22. Power gain and drain efficiency as function of frequency; typical values

7.4.6 Performance curves measured with $\delta = 20\%$, $t_p = 500 \mu s$ and $f = 1300 \text{ MHz}$

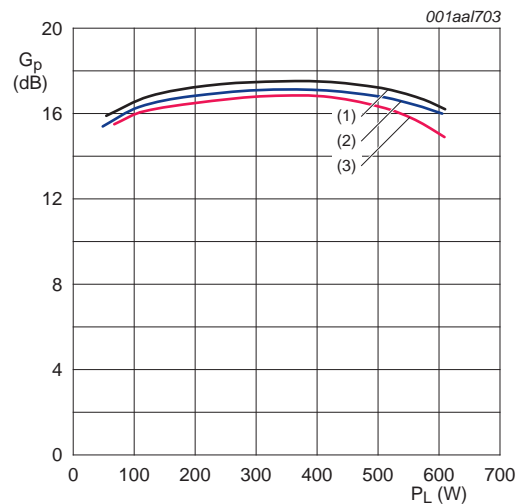


7.4.7 Performance curves measured with $\delta = 10\%$, $t_p = 1\text{ ms}$ and $T_h = 25\text{ }^\circ\text{C}$



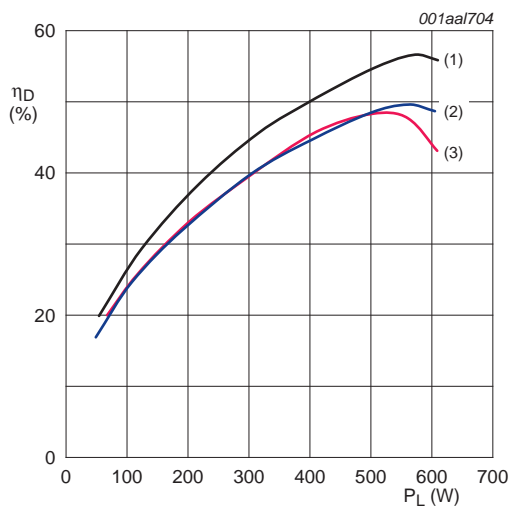
$V_{DS} = 50\text{ V}$; $I_{Dq} = 150\text{ mA}$.
 (1) $f = 1200\text{ MHz}$
 (2) $f = 1300\text{ MHz}$
 (3) $f = 1400\text{ MHz}$

Fig 26. Output power as a function of input power; typical values



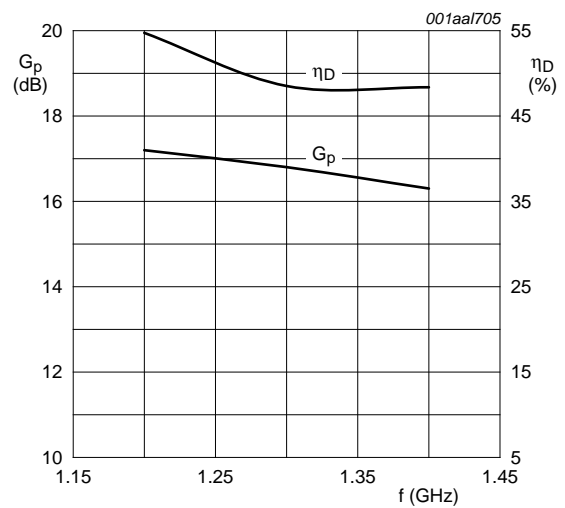
$V_{DS} = 50\text{ V}$; $I_{Dq} = 150\text{ mA}$.
 (1) $f = 1200\text{ MHz}$
 (2) $f = 1300\text{ MHz}$
 (3) $f = 1400\text{ MHz}$

Fig 27. Power gain as a function of output power; typical values



$V_{DS} = 50\text{ V}$; $I_{Dq} = 150\text{ mA}$.
 (1) $f = 1200\text{ MHz}$
 (2) $f = 1300\text{ MHz}$
 (3) $f = 1400\text{ MHz}$

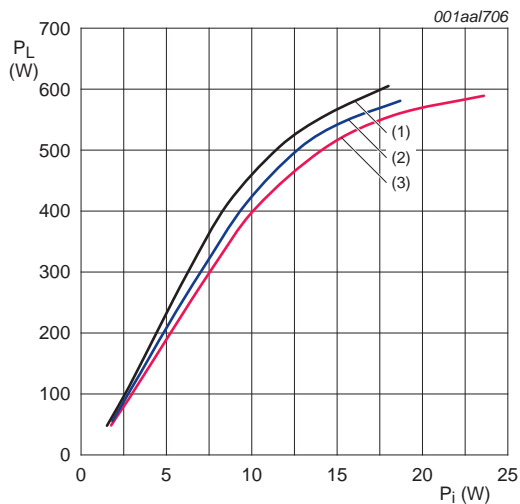
Fig 28. Drain efficiency as a function of output power; typical values



$V_{DS} = 50\text{ V}$; $I_{Dq} = 150\text{ mA}$.

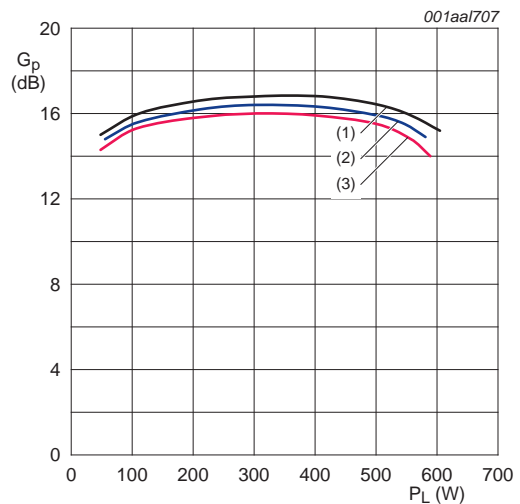
Fig 29. Power gain and drain efficiency as function of frequency; typical values

7.4.8 Performance curves measured with $\delta = 10\%$, $t_p = 1\text{ ms}$ and $T_h = 65\text{ }^\circ\text{C}$



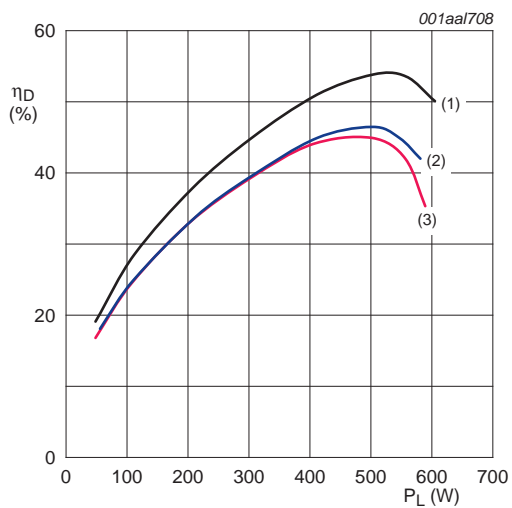
$V_{DS} = 50\text{ V}; I_{Dq} = 150\text{ mA}$.
 (1) $f = 1200\text{ MHz}$
 (2) $f = 1300\text{ MHz}$
 (3) $f = 1400\text{ MHz}$

Fig 30. Output power as a function of input power; typical values



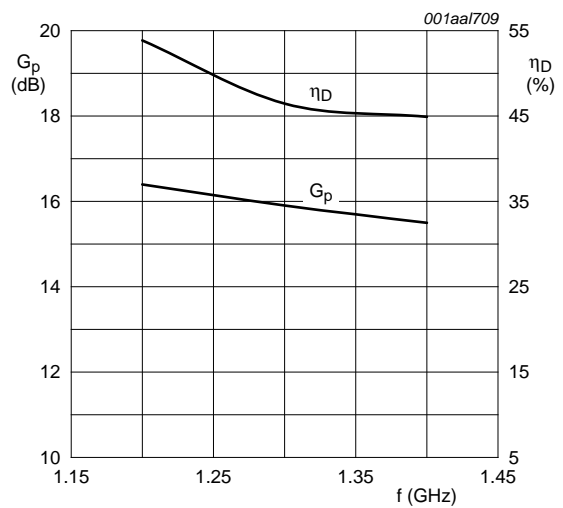
$V_{DS} = 50\text{ V}; I_{Dq} = 150\text{ mA}$.
 (1) $f = 1200\text{ MHz}$
 (2) $f = 1300\text{ MHz}$
 (3) $f = 1400\text{ MHz}$

Fig 31. Power gain as a function of output power; typical values



$V_{DS} = 50\text{ V}; I_{Dq} = 150\text{ mA}$.
 (1) $f = 1200\text{ MHz}$
 (2) $f = 1300\text{ MHz}$
 (3) $f = 1400\text{ MHz}$

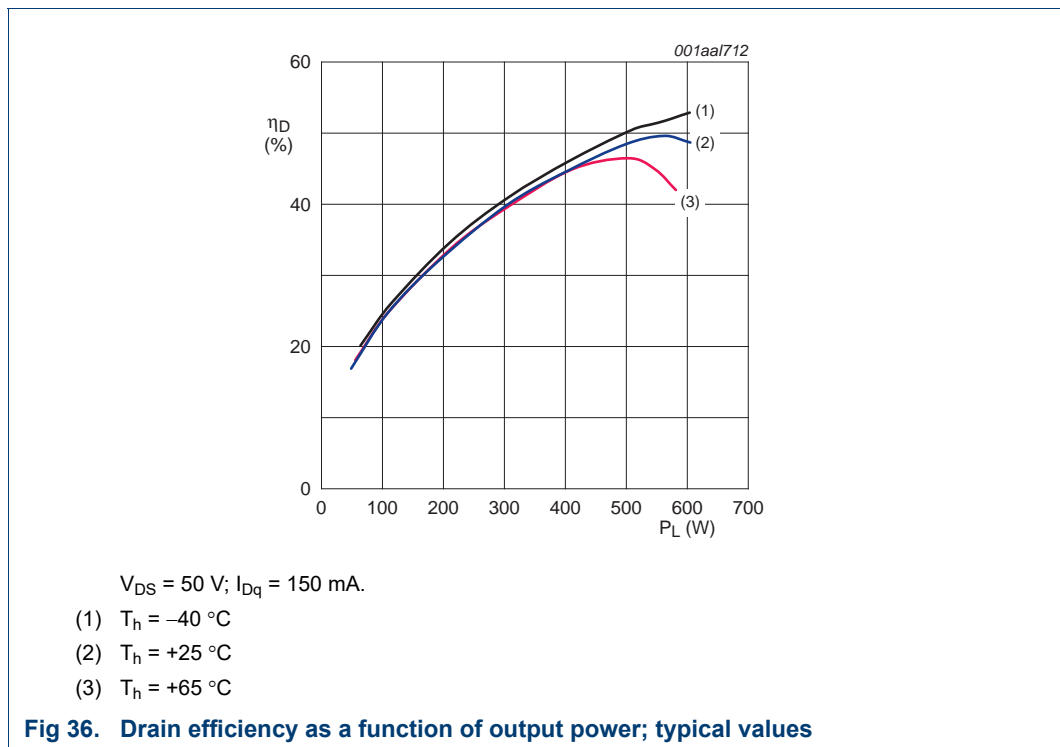
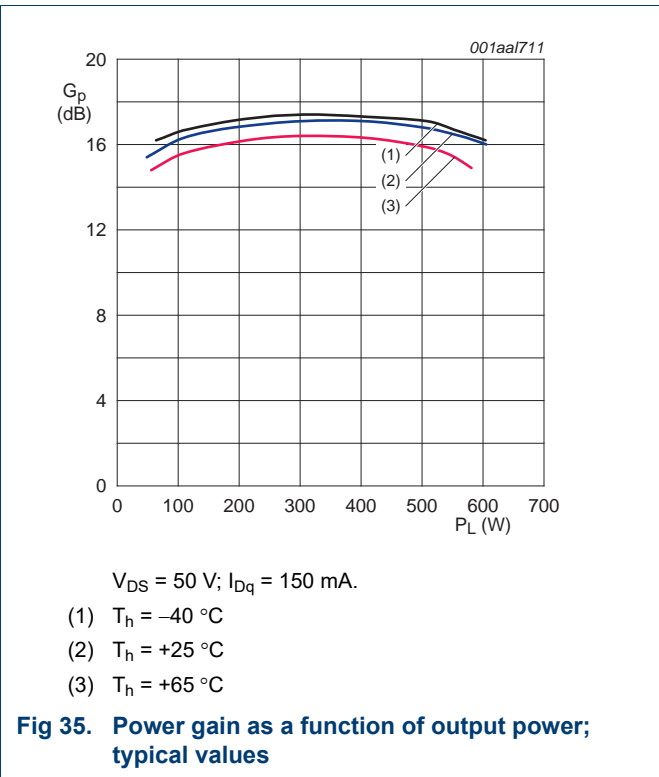
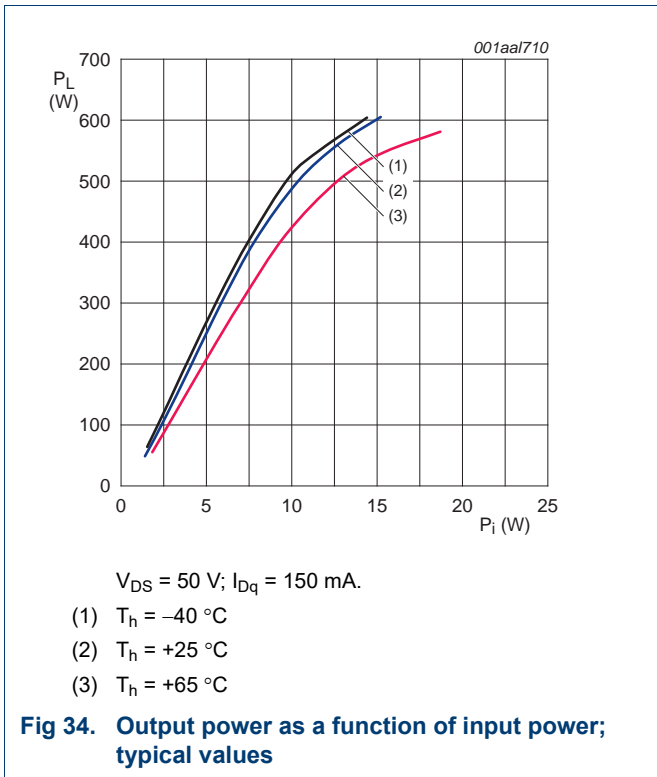
Fig 32. Drain efficiency as a function of output power; typical values



$V_{DS} = 50\text{ V}; I_{Dq} = 150\text{ mA}$.

Fig 33. Power gain and drain efficiency as function of frequency; typical values

7.4.9 Performance curves measured with $\delta = 10\%$, $t_p = 1\text{ ms}$ and $f = 1300\text{ MHz}$



8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

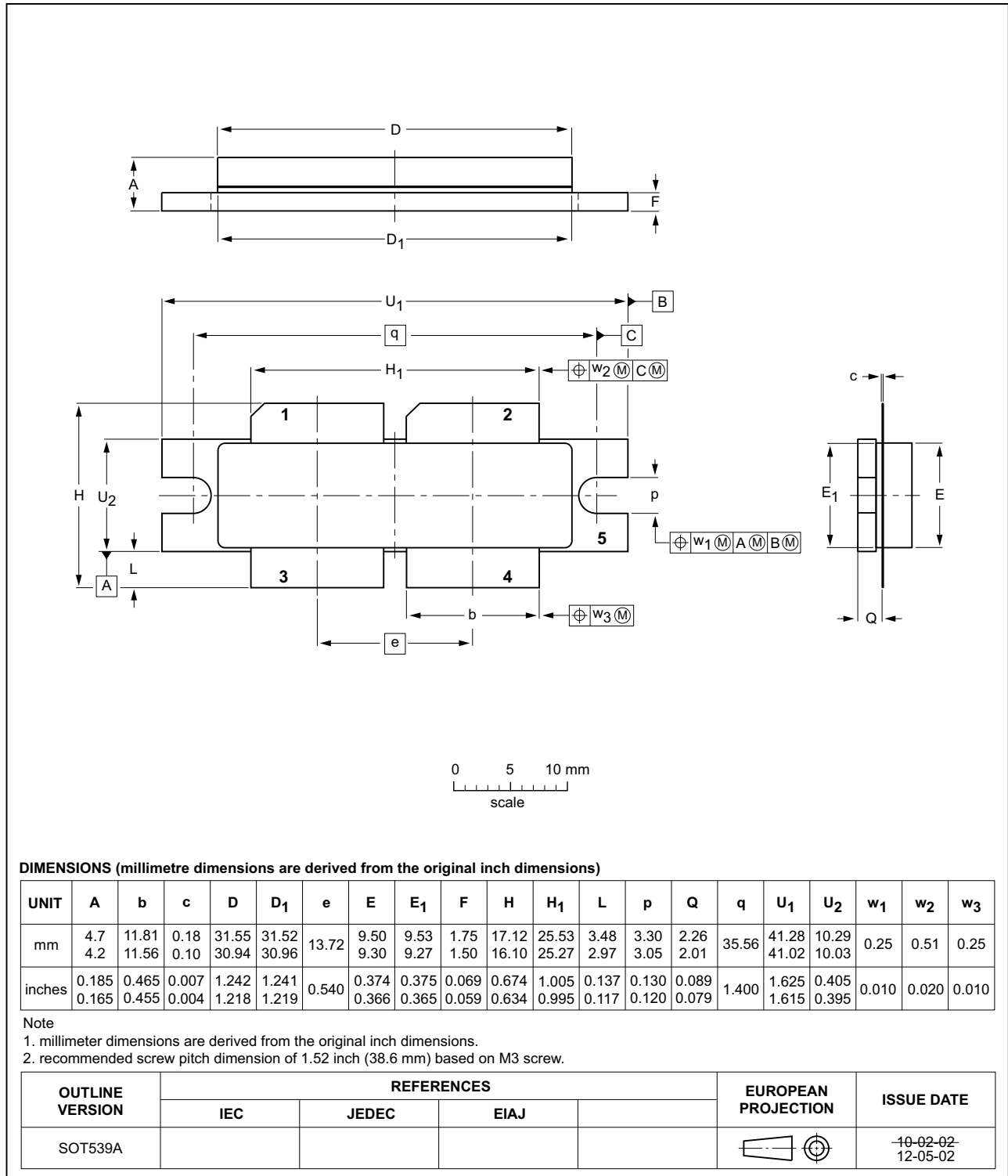


Fig 37. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B

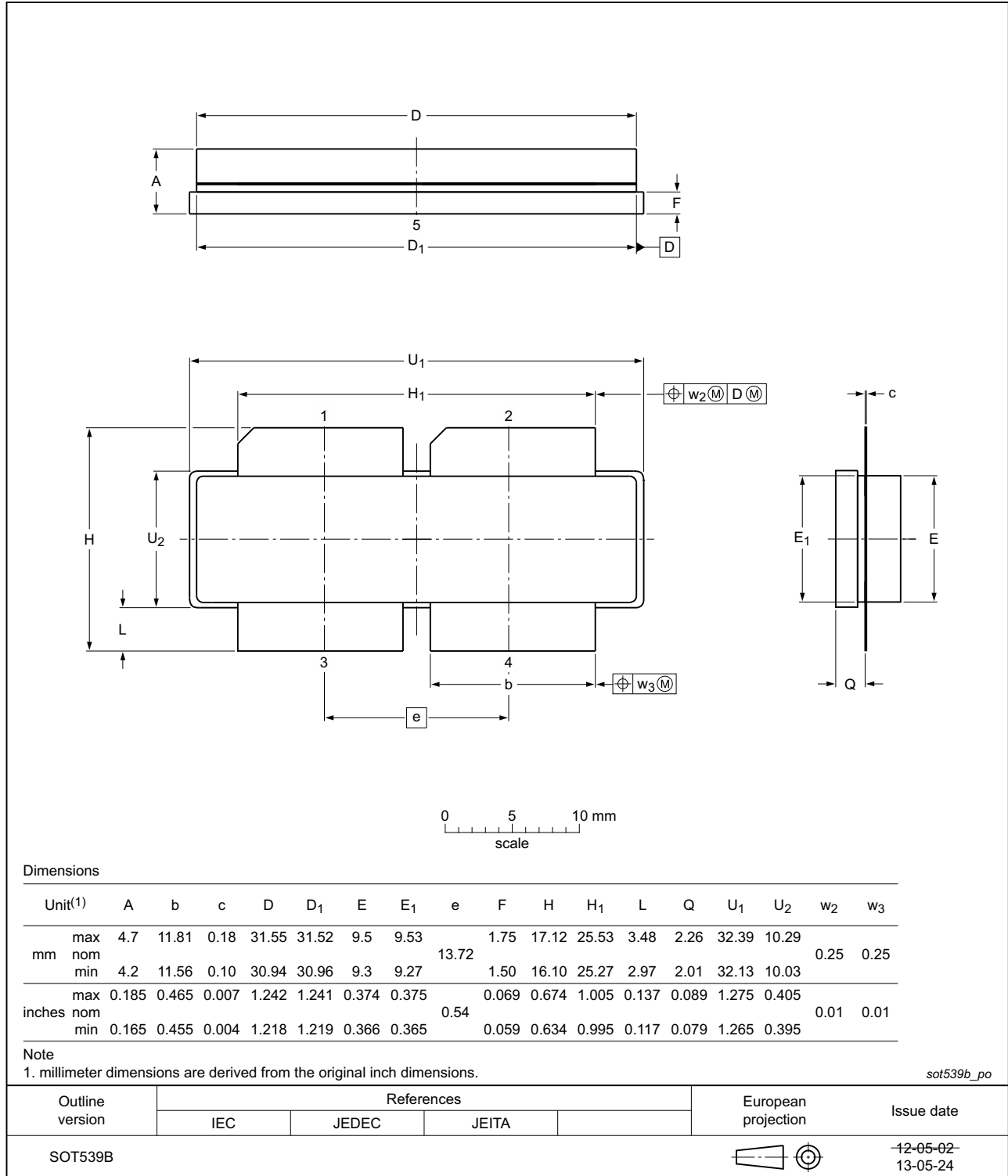


Fig 38. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
L-band	Long wave Band
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL8H1214L-500_1214LS-500 #3	20150901	Product data sheet	-	BLL8H1214L-500_1214LS-500 #2
Modifications:	<ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. 			
BLL8H1214L-500_1214LS-500 #2	20150209	Product data sheet	-	BLL8H1214L-500_1214LS-500 #1
BLL8H1214L-500_1214LS-500 #1	20140930	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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