

100V N-Channel Power MOSFET

DESCRIPTION

The BLM22N10 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

Application

- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply

KEY CHARACTERISTICS

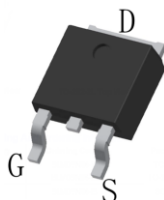
- $V_{DS} = 100V, I_D = 50A$
 $R_{DS(ON)} < 22m\Omega @ V_{GS}=10V$
- Special process technology for high ESD capability
- High density cell design for lower $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation

100% UIS TESTED !

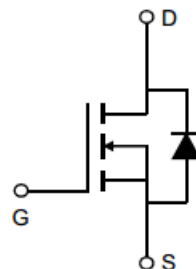
100% DVDS TESTED !



TO-220 Top View



TO-252-2L Top View



Schematic diagram

Package Marking And Ordering Information

Device Marking	Ordering Codes	Package	Product Code	Packing
M22N10	BLM22N10-P	TO-220	BLM22N10	Tube
M22N10	BLM22N10-D	TO-252-2L	BLM22N10	Tape Reel

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D (TO-220)	50	A
	I_D (TO-252)	40	A
Drain Current-Pulsed (Note 1)	I_{DM}	200	A
Maximum Power Dissipation($T_c=25^\circ C$)	P_D (TO-220)	125	W
	P_D (TO-252)	83	W
Single pulse avalanche energy (Note 2)	E_{AS}	180	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic (TO-220)

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.2	$^{\circ}\text{C/W}$
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Thermal Characteristic (TO-252)

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.8	$^{\circ}\text{C/W}$
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Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-Source On-State Resistance ^(Note 3)	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	18	22	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =15A	-	18.8	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	3030	-	pF
Output Capacitance	C _{oss}		-	182	-	pF
Reverse Transfer Capacitance	C _{rss}		-	152	-	pF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =30A, V _{GS} =10V, R _{GEN} =3Ω	-	12	-	nS
Turn-on Rise Time	t _r		-	9	-	nS
Turn-Off Delay Time	t _{d(off)}		-	20	-	nS
Turn-Off Fall Time	t _f			18	-	nS
Total Gate Charge	Q _g	V _{DS} =80V, I _D =25A V _{GS} =10V	-	65	-	nC
Gate-Source Charge	Q _{gs}		-	21	-	nC
Gate-Drain Charge	Q _{gd}		-	20	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =30A	-	-	1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. EAS condition : $T_j=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production.

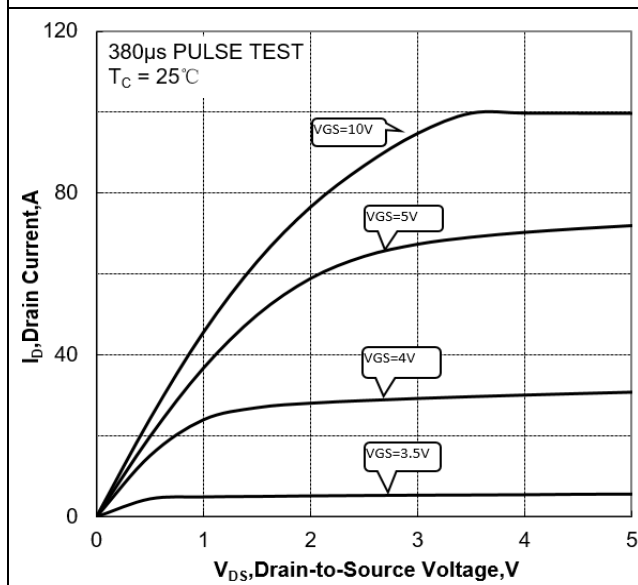
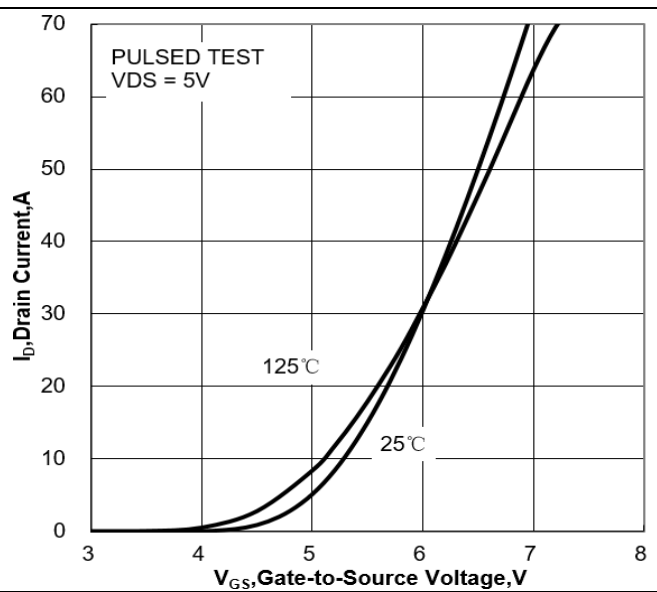
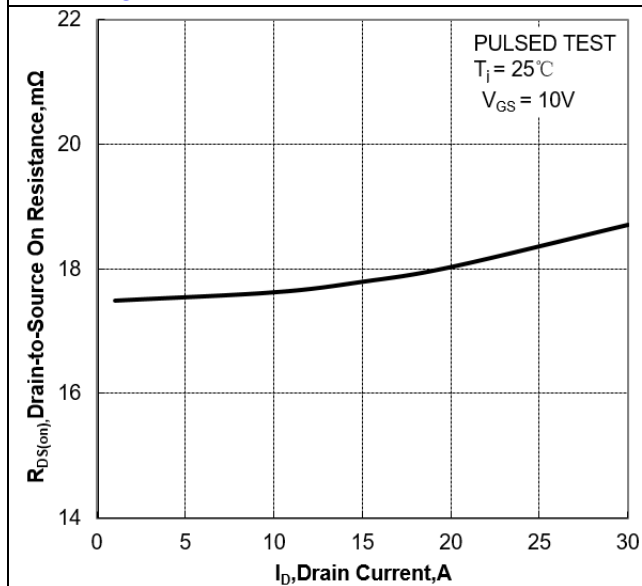
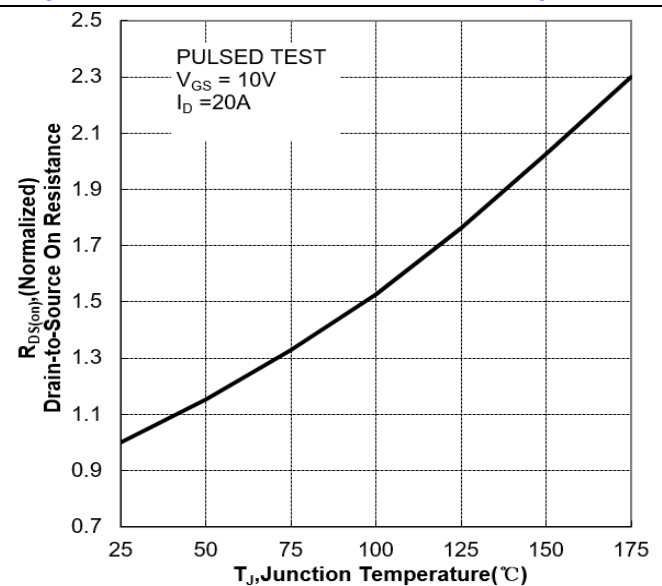
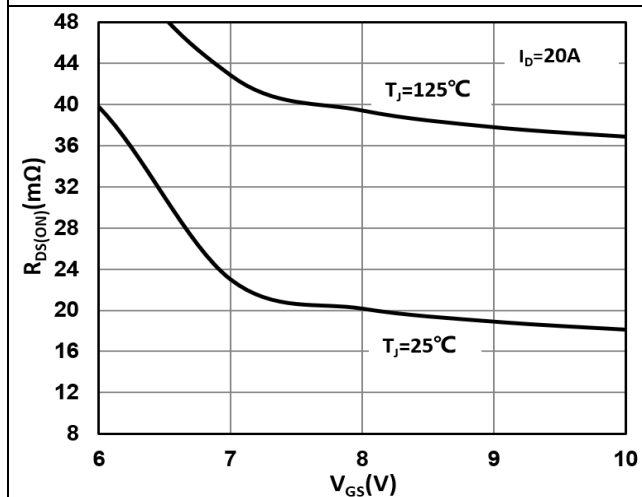
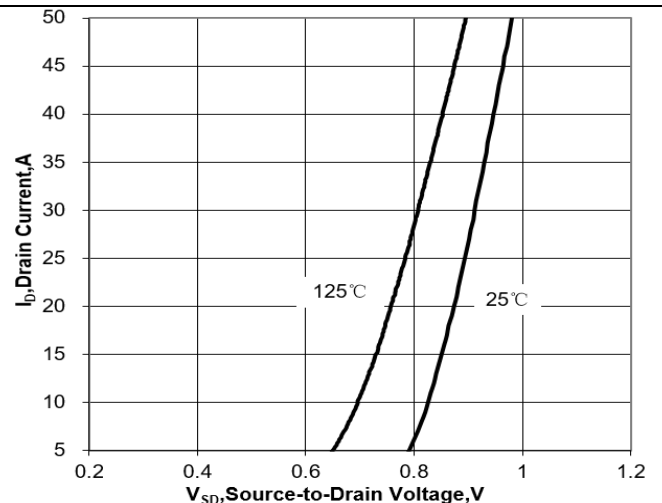
Characteristics Curves
Figure 1 Output Characteristics

Figure 2 Transfer Characteristics

Figure 3 On-Resistance vs. I_D and V_{GS}

Figure 4 On-Resistance vs. Junction Temperature

Figure 5 On-Resistance vs. V_{GS}

Figure 6 Body Diode Forward Voltage


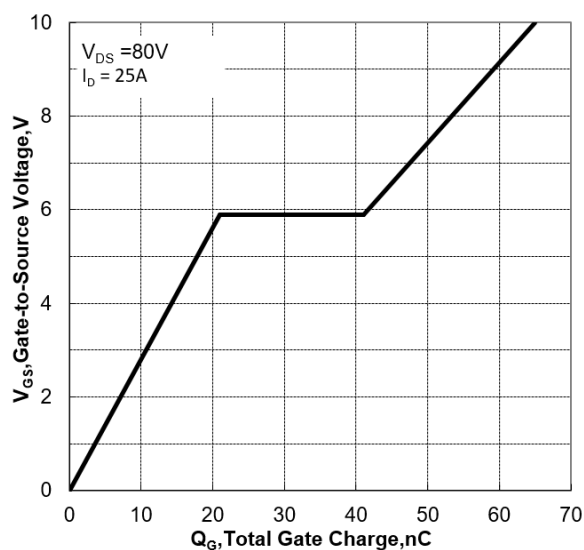
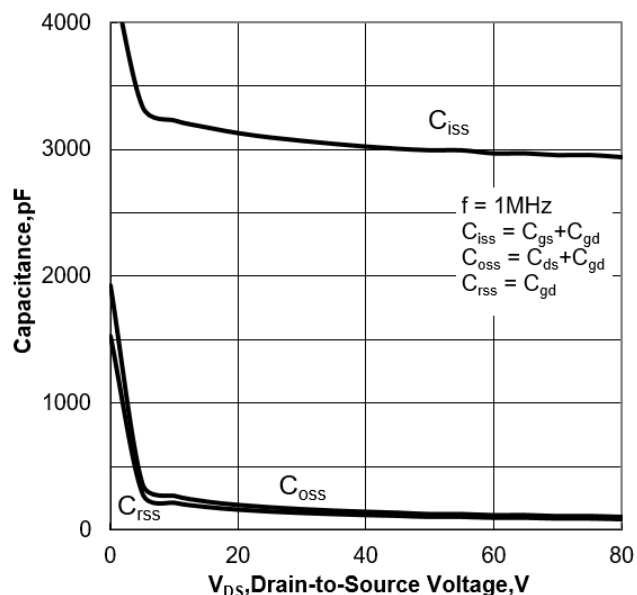
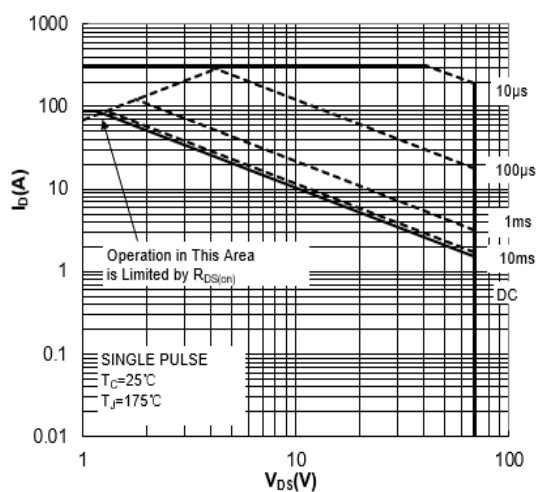
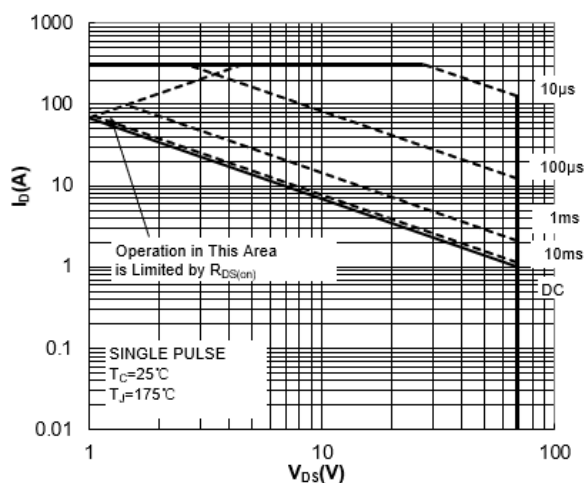
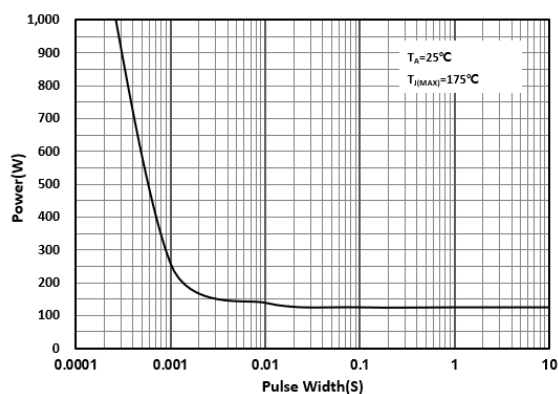
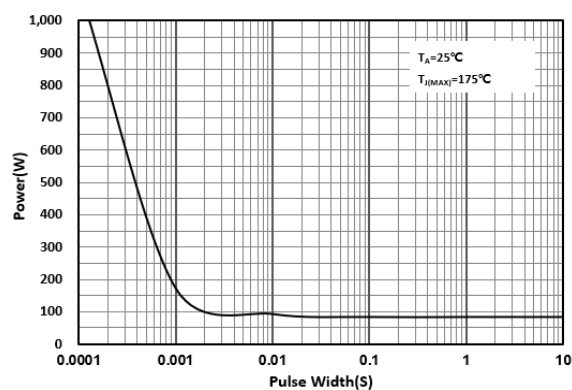
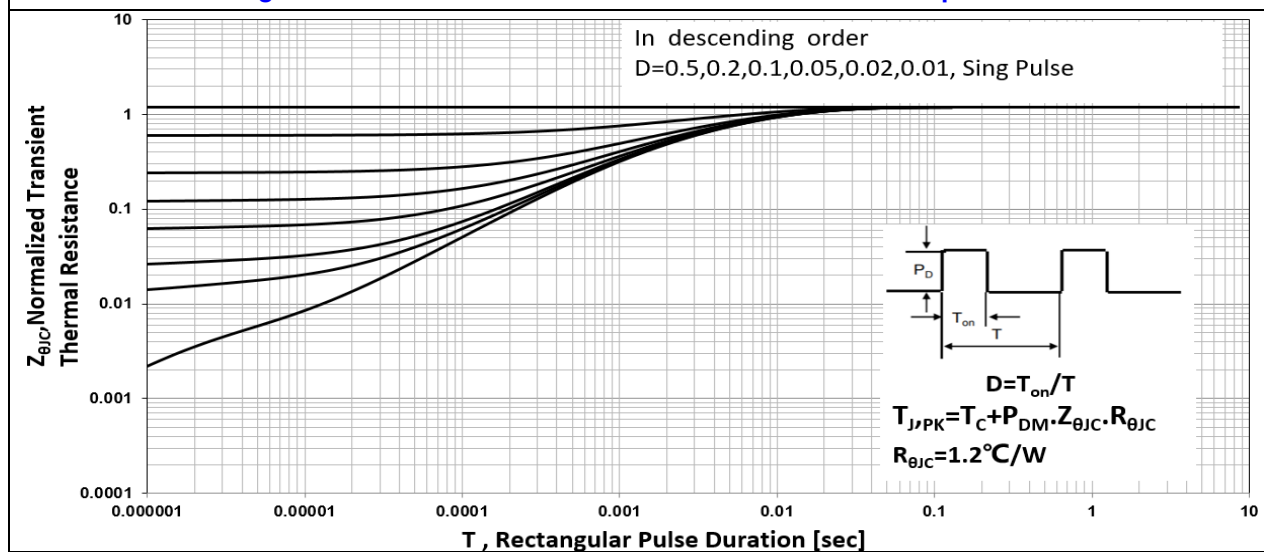
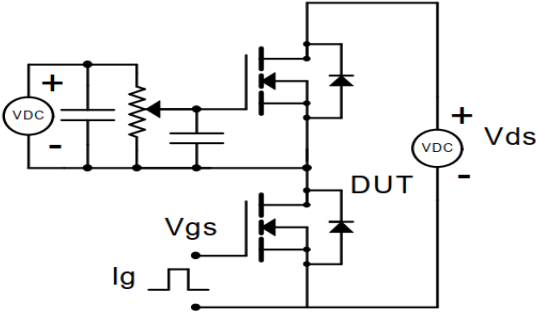
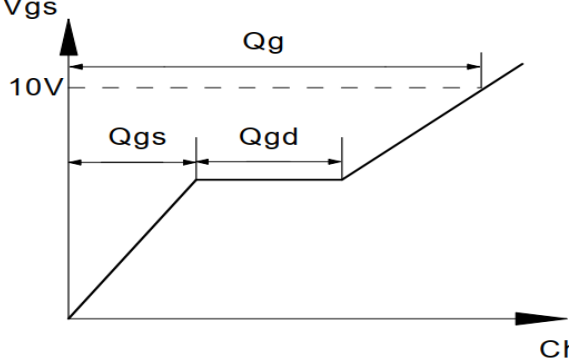
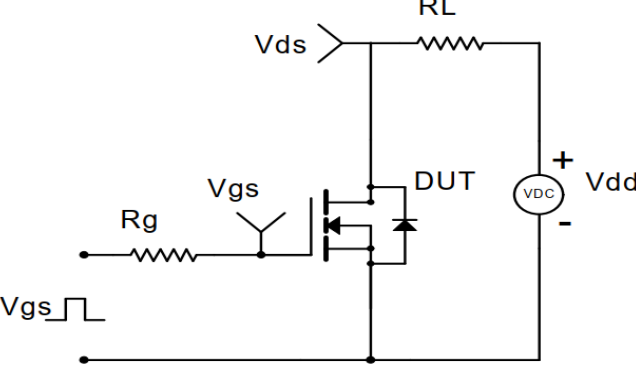
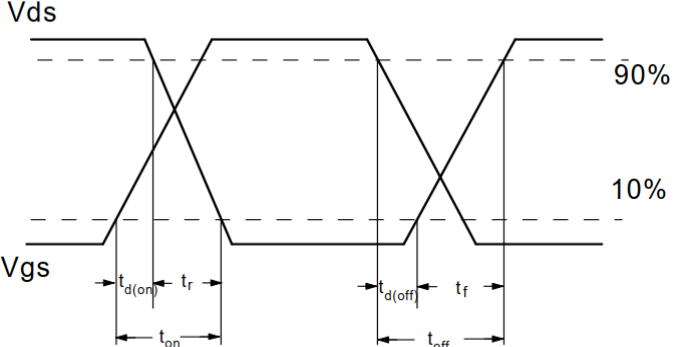
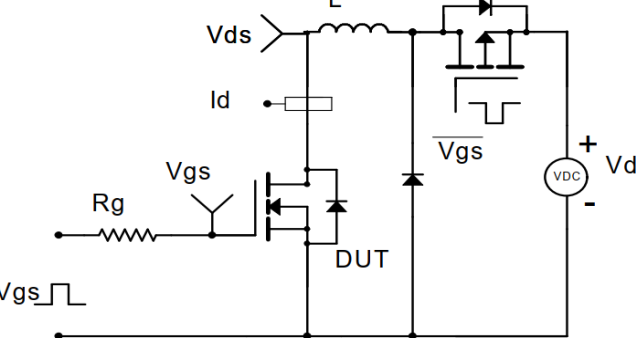
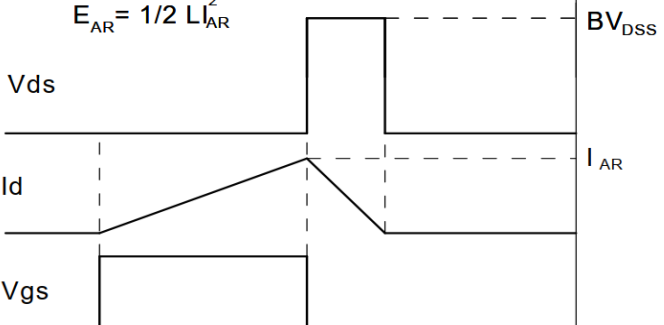
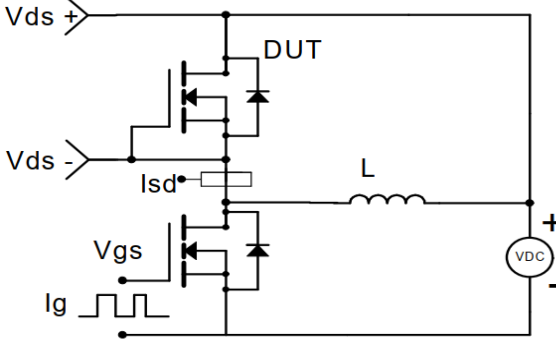
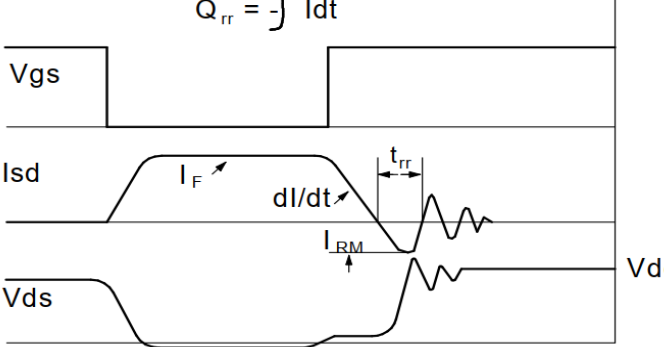
Figure 7 Gate-Charge Characteristics

Figure 8 Capacitance Characteristics

Figure 9A Maximum Forward Biased Safe Operation Area (TO-220)

Figure 9B Maximum Forward Biased Safe Operation Area (TO-252)

Figure 10A Single Pulse Power Rating Junction-to-Ambient (TO-220)

Figure 10B Single Pulse Power Rating Junction-to-Ambient (TO-252)


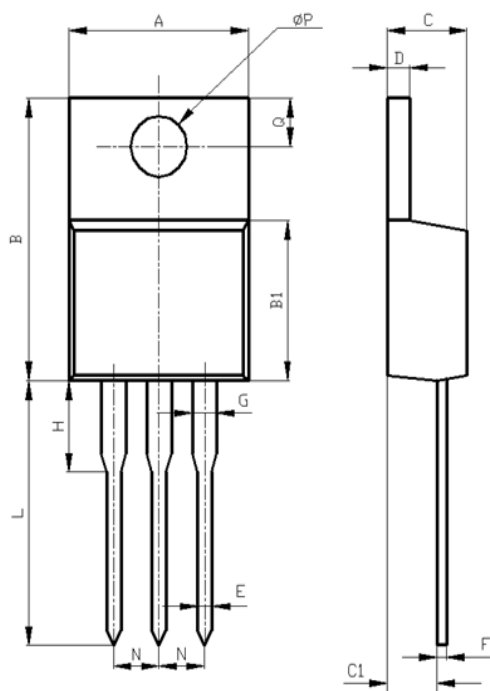
Figure 11 Normalized Maximum Transient Thermal Impedance



Test Circuit and Waveform

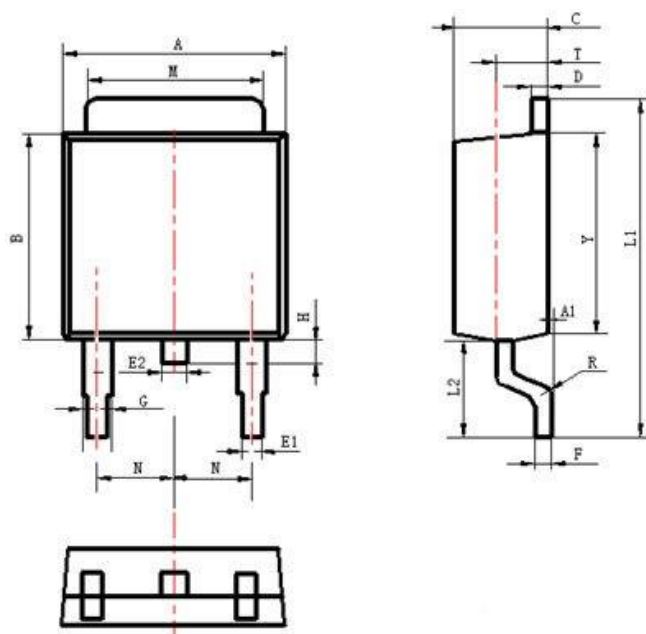
Gate Charge Test Circuit	Gate Charge Test Waveform
	
Resistive Switching Test Circuit	Resistive Switching Test Waveforms
	
Unclamped Inductive Switching (UIS) Test Circuit	Unclamped Inductive Switching (UIS) Test Waveforms
	
Diode Recovery Test Circuit	Diode Recovery Test Waveforms
	

Package Description



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
Ø P	3.50	3.90

TO-220 Package



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.13
B	5.70	6.30
C	2.10	2.50
D	0.30	0.60
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.20
L1	9.60	10.50
L2	2.70	3.10
H	0.60	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shanghai Belling reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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