BLP05H6110XR; BLP05H6110XRG

Power LDMOS transistor

AMPLEON

Rev. 4 — 30 August 2016

Product data sheet

1. Product profile

1.1 General description

A 110 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 600 MHz band.

Table 1. Application information

Test signal	f	V _{DS}	PL	G _p	η_{D}
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	108	50	110	27	75

1.2 Features and benefits

- Easy power control
- Integrated double sided ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 600 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLP05H6	110XR (SOT1223-2)		
1	gate 2		,
2	gate 1	4 3	4
3	drain 1		
4	drain 2	pin 1 index	
5	source	[1]	
			3 aaa-003574
BLP05H6	110XRG (SOT1224-2)		
1	gate 2	4 3	4
2	gate 1		-
3	drain 1		
4	drain 2	pin 1 index	
5	source	[1]	3 aaa-003574

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BLP05H6110XR	HSOP4F	plastic, heatsink small outline package; 4 leads (flat)	SOT1223-2		
BLP05H6110XRG	HSOP4F	plastic, heatsink small outline package; 4 leads	SOT1224-2		

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	135	V
V_{GS}	gate-source voltage		-6	+11	V
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature	[1]	-	225	°C

^[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Тур	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T _j = 125 °C	[1][2]	0.9	K/W
Z _{th(j-c)}	transient thermal impedance from junction to case	T_j = 150 °C; t_p = 100 μs; $δ$ = 20 %	[3]	0.31	K/W

- [1] T_i is the junction temperature.
- [2] $R_{th(j-c)}$ is measured under RF conditions.
- [3] See Figure 1.

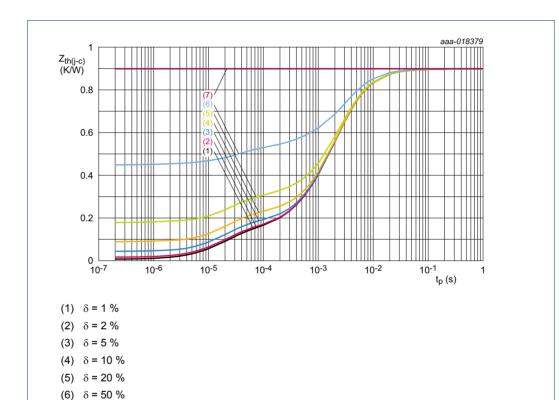


Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics

(7) $\delta = 100 \% (DC)$

 T_i = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.375 \text{ mA}$	135	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 37.5 mA	1.25	1.8	2.25	V
V_{GSq}	gate-source quiescent voltage	V _{DS} = 50 V; I _D = 10 mA	-	1.7	-	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 50 V	-	-	1.4	μΑ

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Table 6. DC characteristics ...continued

 T_i = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	5.4	_	Α
I_{GSS}	gate leakage current	$V_{GS} = 11 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	140	nA
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 1.31 \text{ A}$	-	1.1	_	Ω

Table 7. AC characteristics

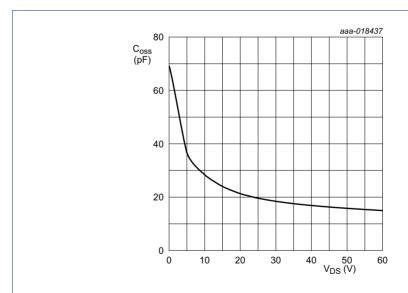
 T_i = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _{rs}	feedback capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	0.4	-	pF
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	46	-	pF
C _{oss}	output capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	17	-	pF

Table 8. RF characteristics

Test signal: pulsed RF; t_p = 100 μ s; δ = 20 %; f = 108 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 20 mA; T_{case} = 25 $^{\circ}$ C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	P _L = 110 W	25.5	27	-	dB
RLin	input return loss	P _L = 110 W	-	-9	-	dB
η_{D}	drain efficiency	P _L = 110 W	72	75	-	%



 $V_{GS} = 0 V$; f = 1 MHz.

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

7. Test information

7.1 Ruggedness in class-AB operation

The BLP05H6110XR and BLP05H6110XRG are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions: $V_{DS} = 50 \text{ V}$; $I_{Dq} = 20 \text{ mA}$; $P_L = 110 \text{ W pulsed}$; f = 108 MHz.

7.2 Impedance information

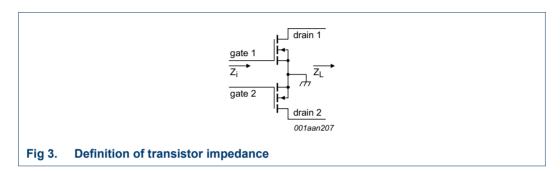


Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 50 V and P_L = 110 W.

f	Z_i	Z L
(MHz)	(Ω)	(Ω)
108	42 – j116	34 + j8.1

7.3 UIS avalanche energy

Table 10. Typical avalanche data per section

 T_{amb} = 25 °C; typical test data; test jig without water cooling.

I _{AS}	E _{AS}
(A)	(J)
3	0.27
3.8	0.17
4.5	0.13

For information see application note AN10273.

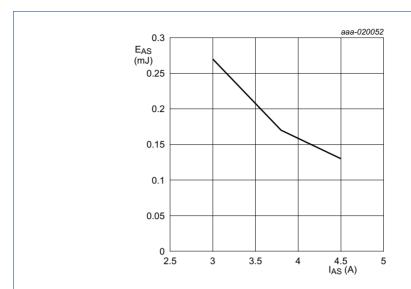
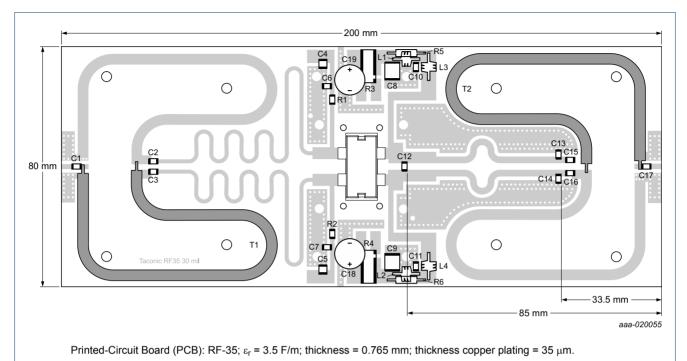


Fig 4. Non-repetitive avalanche energy as a function of single pulse avalanche current; typical values

7.4 Test circuit



See <u>Table 11</u> for a list of components.

Fig 5. Component layout for class-AB production test circuit

Table 11. List of components

For test circuit see Figure 5.

Component	Description	Value		Remarks
C1	multilayer ceramic chip capacitor	100 pF	[1]	
C2, C3	multilayer ceramic chip capacitor	1 nF	[1]	
C4, C5	multilayer ceramic chip capacitor	4.7 μF, 50 V		Kemet: C1210X475K5RAC-T4
C6, C7	multilayer ceramic chip capacitor	750 pF	[1]	
C8, C9	multilayer ceramic chip capacitor	4.7 μF, 100 V		TDK: C5750X7R2A475KT
C10, C11	multilayer ceramic chip capacitor	750 pF	[1]	
C12	multilayer ceramic chip capacitor	13 pF	[1]	
C13, C14	multilayer ceramic chip capacitor	27 pF	[1]	
C15, C16	multilayer ceramic chip capacitor	1 nF	[1]	
C17	multilayer ceramic chip capacitor	47 pF	[1]	
C18,C19	electrolytic capacitor	2200 μF, 64 V		
L1, L2	wire inductor	5 turns, D = 3 mm, 1 mm copper wire		
L3, L4	wire inductor	8 turns, D = 3 mm, 1 mm copper wire		
R1, R2	resistor	4.7 kΩ		SMD 1206
R3, R4	shunt resistor	0.01 Ω		Ohmite: FC4L110R010FER
R5, R6	metal film resistor	10 Ω, 0.6 W		
T1, T2	semi rigid coax	50 Ω, length = 160 mm		EZ Form: EZ-141-AL-TP-M17

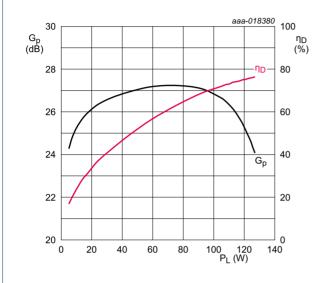
[1] American Technical Ceramics type 100B or capacitor of same quality.

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7.5 Graphical data

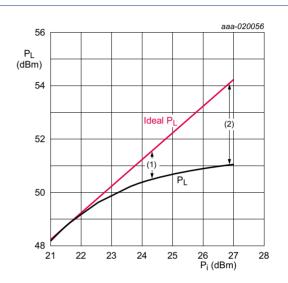
The following figures are measured in a class-AB production test circuit.

7.5.1 1-Tone CW pulsed



 V_{DS} = 50 V; I_{Dq} = 40 mA; f = 108 MHz; t_p = 100 $\mu s;$ δ = 20 %.

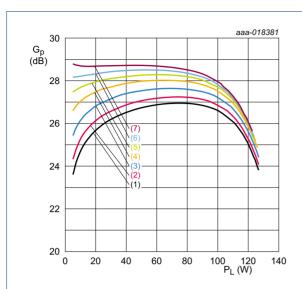
Fig 6. Power gain and drain efficiency as function of output power; typical values



 V_{DS} = 50 V; I_{Dq} = 40 mA; f = 108 MHz; t_p = 100 $\mu s;$ δ = 20 %.

- (1) $P_{L(1dB)} = 50.5 \text{ dBm}$ (111 W)
- (2) $P_{L(3dB)} = 51.0 \text{ dBm } (126 \text{ W})$

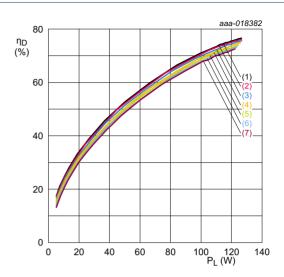
Fig 7. Output power as a function of input power; typical values



 V_{DS} = 50 V; f = 108 MHz; t_p = 100 μ s; δ = 20 %.

- (1) $I_{Dq} = 20 \text{ mA}$
- (2) $I_{Dq} = 40 \text{ mA}$
- (3) $I_{Dq} = 100 \text{ mA}$
- (4) $I_{Dq} = 200 \text{ mA}$
- (5) $I_{Dq} = 300 \text{ mA}$
- (6) $I_{Dq} = 400 \text{ mA}$
- (7) $I_{Dq} = 500 \text{ mA}$

Fig 8. Power gain as a function of output power; typical values

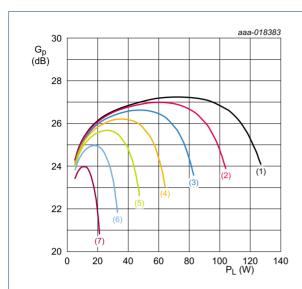


 V_{DS} = 50 V; f = 108 MHz; t_p = 100 μ s; δ = 20 %.

- (1) $I_{Dq} = 20 \text{ mA}$
- (2) $I_{Dq} = 40 \text{ mA}$
- (3) $I_{Dq} = 100 \text{ mA}$
- (4) $I_{Dq} = 200 \text{ mA}$
- (5) $I_{Dq} = 300 \text{ mA}$
- (6) $I_{Dq} = 400 \text{ mA}$ (7) $I_{Dq} = 500 \text{ mA}$

typical values

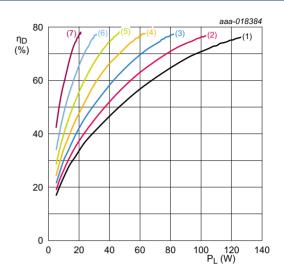
Fig 9. Drain efficiency as a function of output power;



 I_{Dq} = 40 mA; f = 108 MHz; t_p = 100 μ s; δ = 20 %.

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$
- (4) $V_{DS} = 35 V$
- (5) $V_{DS} = 30 \text{ V}$
- (6) $V_{DS} = 25 V$
- (7) $V_{DS} = 20 \text{ V}$

Fig 10. Power gain as a function of output power; typical values



 I_{Dq} = 40 mA; f = 108 MHz; t_p = 100 μ s; δ = 20 %.

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$
- (4) $V_{DS} = 35 V$
- (5) $V_{DS} = 30 \text{ V}$
- (6) $V_{DS} = 25 V$
- (7) $V_{DS} = 20 \text{ V}$

Fig 11. Drain efficiency as a function of output power; typical values

8. Package outline

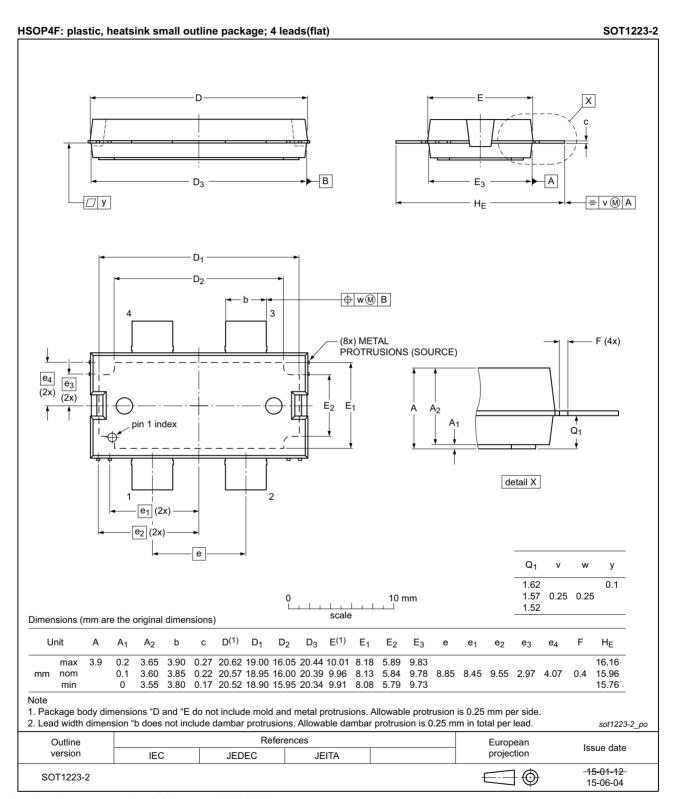


Fig 12. Package outline SOT1223-2 (HSOP4F)

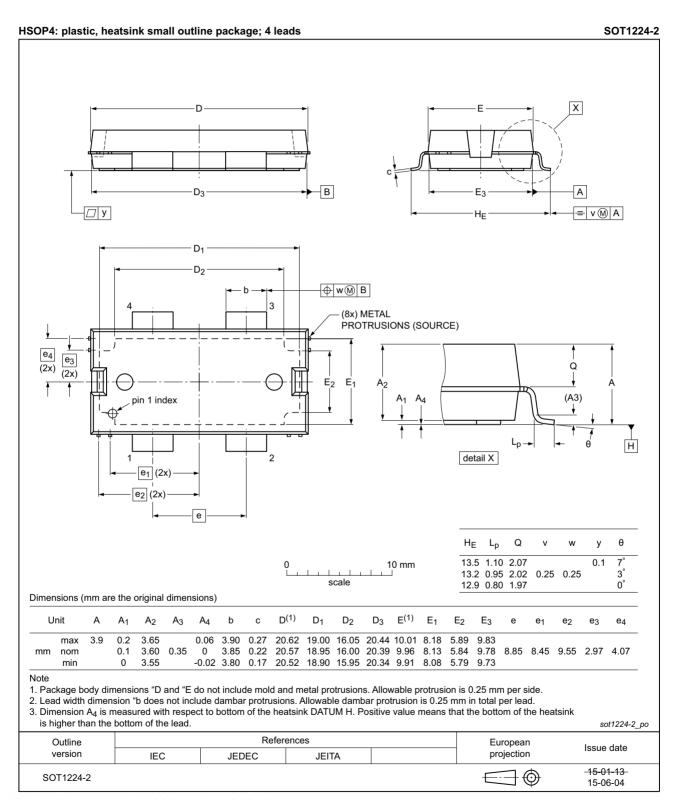


Fig 13. Package outline SOT1224-2 (HSOP4F)

Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
UIS	Unclamped Inductive Switching
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
BLP05H6110XR_H6110XRG v.4	20160830	Product data sheet	-	BLP05H6110XR v.3		
Modifications	 The document now describes both the straight lead and gull-wing versions of this product: BLP05H6110XR and BLP05H6110XRG respectively 					
	• Table 2 on page 2: added BLP05H6110XRG data					
	Table 3 on page 2: added BLP05H6110XRG data					
	 Section 7.1 on page 5: added BLP05H6110XRG 					
	• Figure 13 or	n page 12: added figure S	OT1224-2			
BLP05H6110XR v.3	20160203	Product data sheet	-	BLP05H6110XR#2		
BLP05H6110XR#2	20150901	Objective data sheet	-	BLP05H6110XR v.1		
BLP05H6110XR v.1	20150518	Objective data sheet	-	-		

12. Legal information

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions"
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