

# BLP05H6150XR; BLP05H6150XRG

Power LDMOS transistor

Rev. 4 — 21 September 2016

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

A 150 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 600 MHz band.

Table 1. Application information

Test signal	f	V <sub>DS</sub>	P <sub>L</sub>	G <sub>p</sub>	η <sub>D</sub>	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
pulsed RF	108	50	150	27	75	-
CW	1.8 to 30	50	100	29	60	-
	135	50	150	26	73	-
	174 to 230	50	150	22	67	-
DVB-T	174 to 230	50	25	23	29	-36

### 1.2 Features and benefits

- Easy power control
- Integrated double sided ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 600 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLP05H6150XR (SOT1223-2)</b>			
1	gate 2		
2	gate 1		
3	drain 1		
4	drain 2		
5	source <a href="#">[1]</a>		
<b>BLP05H6150XRG (SOT1224-2)</b>			
1	gate 2		
2	gate 1		
3	drain 1		
4	drain 2		
5	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP05H6150XR	HSOP4F	plastic, heatsink small outline package; 4 leads (flat)	SOT1223-2
BLP05H6150XRG	HSOP4F	plastic, heatsink small outline package; 4 leads	SOT1224-2

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	135	V
$V_{GS}$	gate-source voltage		-6	+11	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<a href="#">[1]</a>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

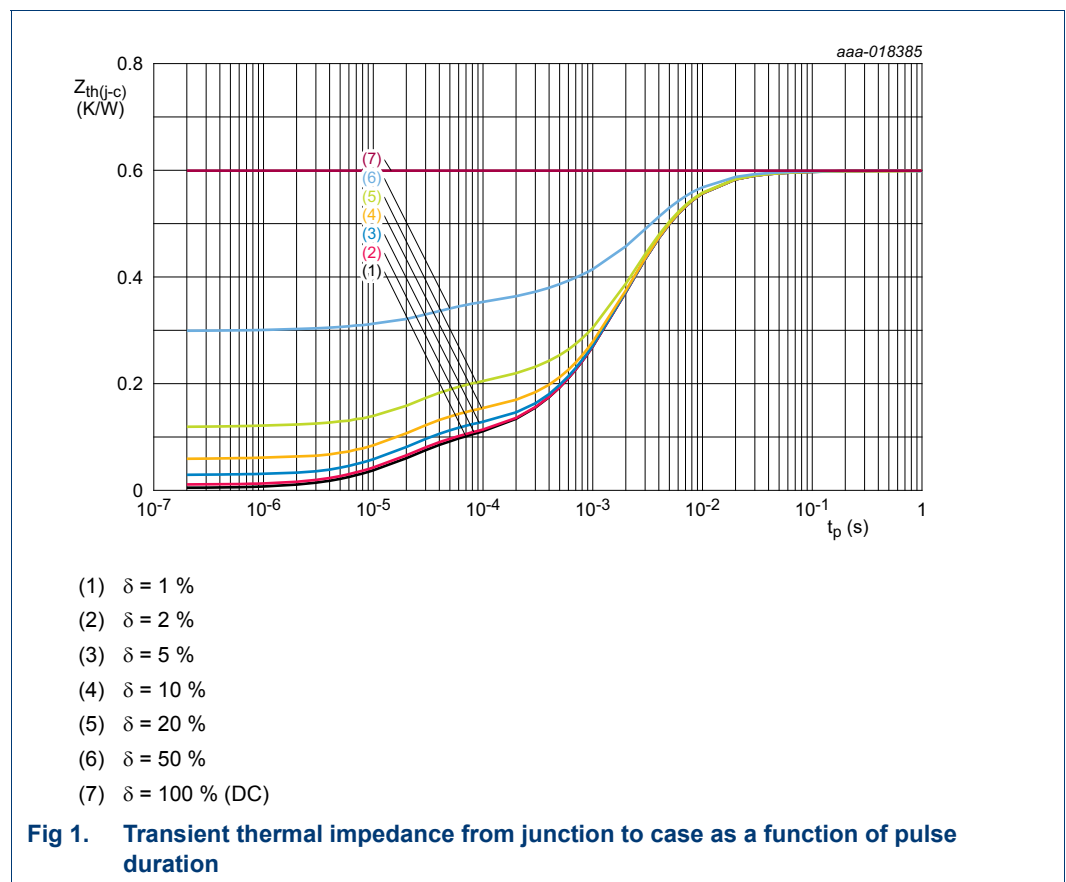
Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_j = 125\text{ °C}$ [1][2]	0.6	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_j = 150\text{ °C}; t_p = 100\text{ }\mu\text{s}; \delta = 20\%$ [3]	0.21	K/W

[1]  $T_j$  is the junction temperature.

[2]  $R_{th(j-c)}$  is measured under RF conditions.

[3] See Figure 1.



## 6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C};$  per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.5\text{ mA}$	135	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 50\text{ mA}$	1.25	1.8	2.25	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 50\text{ V}; I_D = 20\text{ mA}$	-	1.7	-	V

**Table 6. DC characteristics ...continued**  
*T<sub>j</sub> = 25 °C; per section unless otherwise specified.*

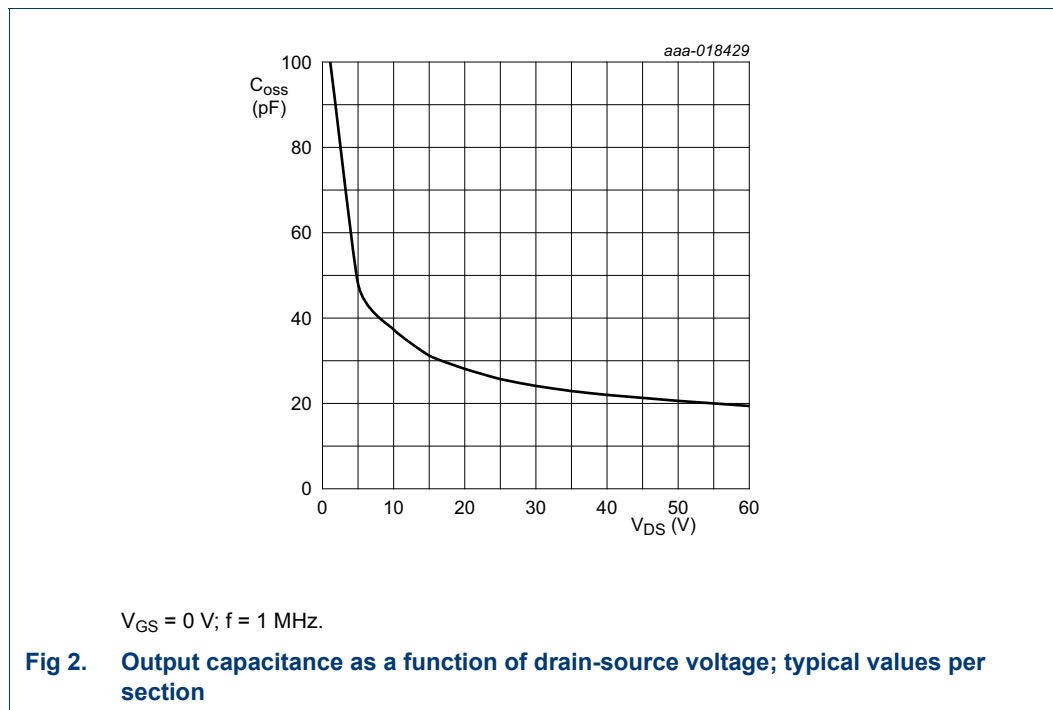
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V	-	-	1.4	μA
I <sub>DSX</sub>	drain cut-off current	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; V <sub>DS</sub> = 10 V	-	7.2	-	A
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	140	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; I <sub>D</sub> = 1.75 A	-	0.8	-	Ω

**Table 7. AC characteristics**  
*T<sub>j</sub> = 25 °C; per section unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C <sub>rs</sub>	feedback capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; f = 1 MHz	-	0.5	-	pF
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; f = 1 MHz	-	60	-	pF
C <sub>oss</sub>	output capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; f = 1 MHz	-	21	-	pF

**Table 8. RF characteristics**  
*Test signal: pulsed RF; t<sub>p</sub> = 100 μs; δ = 20 %; f = 108 MHz; RF performance at V<sub>DS</sub> = 50 V; I<sub>Dq</sub> = 100 mA; T<sub>case</sub> = 25 °C; unless otherwise specified; in a class-AB production test circuit.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G <sub>p</sub>	power gain	P <sub>L</sub> = 150 W	25.5	27	-	dB
RL <sub>in</sub>	input return loss	P <sub>L</sub> = 150 W	-	-8	-	dB
η <sub>D</sub>	drain efficiency	P <sub>L</sub> = 150 W	73	75	-	%



## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLP05H6150XR and BLP05H6150XRG are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions:  $V_{DS} = 50\text{ V}$ ;  $I_{DQ} = 40\text{ mA}$ ;  $P_L = 150\text{ W}$  pulsed;  $f = 108\text{ MHz}$ .

### 7.2 Impedance information

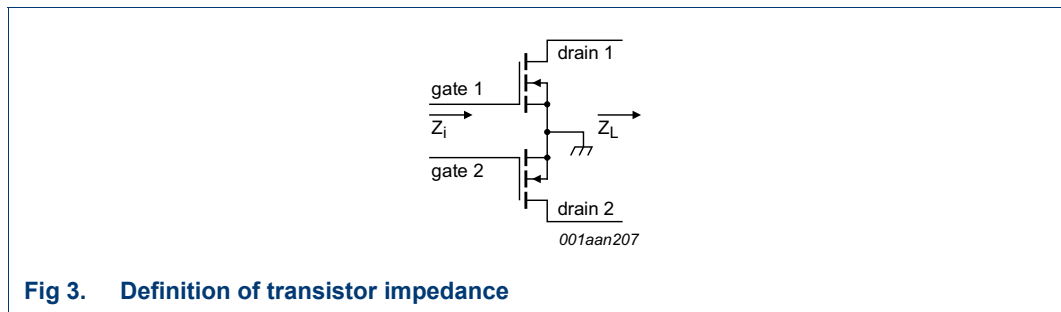


Fig 3. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated  $Z_i$  and  $Z_L$  device impedance; impedance info at  $V_{DS} = 50\text{ V}$  and  $P_L = 150\text{ W}$ .

f (MHz)	$Z_i$ ( $\Omega$ )	$Z_L$ ( $\Omega$ )
108	$32 - j99$	$25 + j6.0$

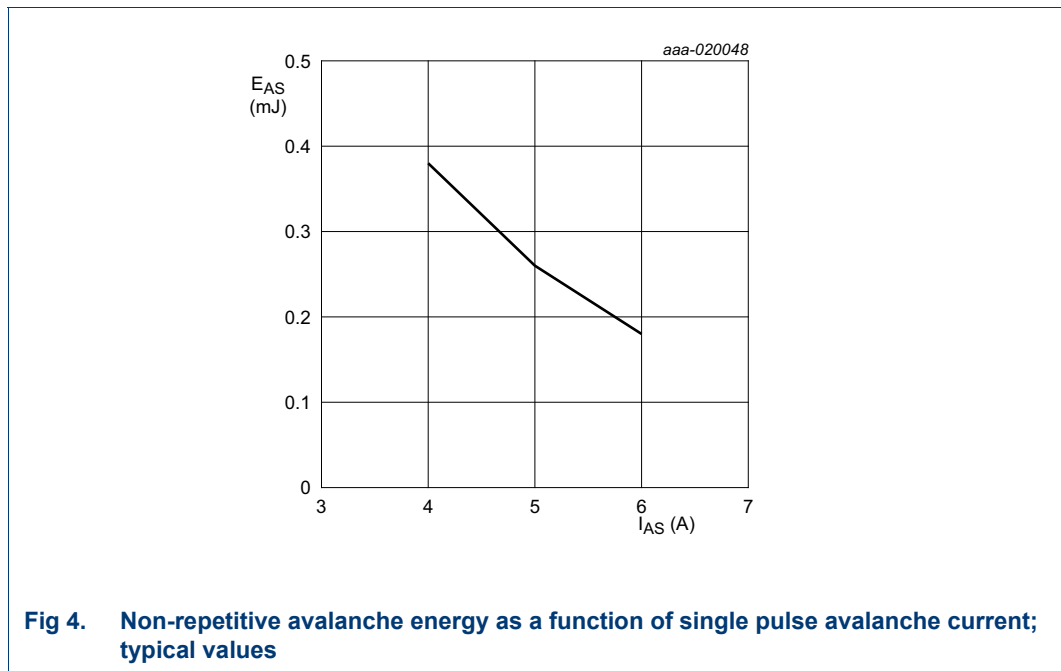
### 7.3 UIS avalanche energy

Table 10. Typical avalanche data per section

$T_{amb} = 25\text{ }^\circ\text{C}$ ; typical test data; test jig without water cooling.

$I_{AS}$ (A)	$E_{AS}$ (J)
4	0.38
5	0.26
6	0.18

For information see application note AN10273.



7.4 Test circuit

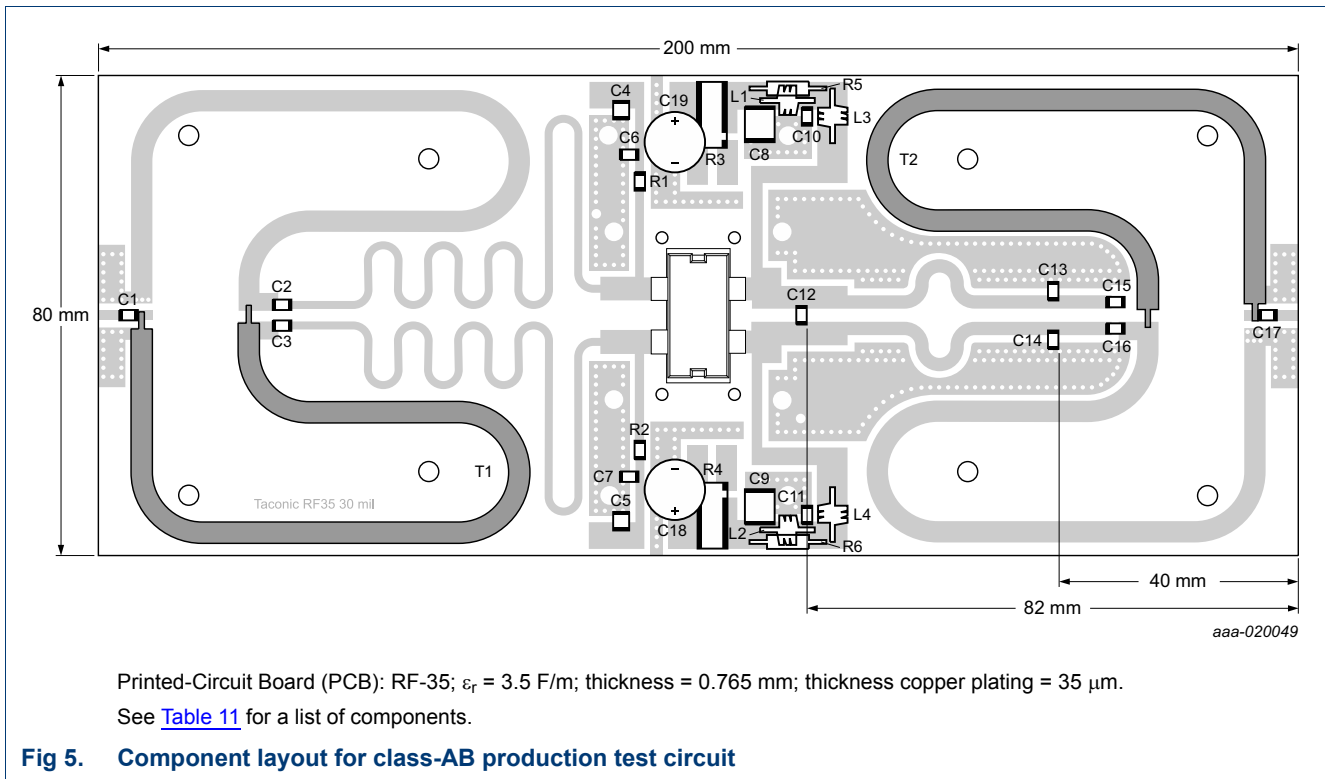


Table 11. List of components

For test circuit see [Figure 5](#).

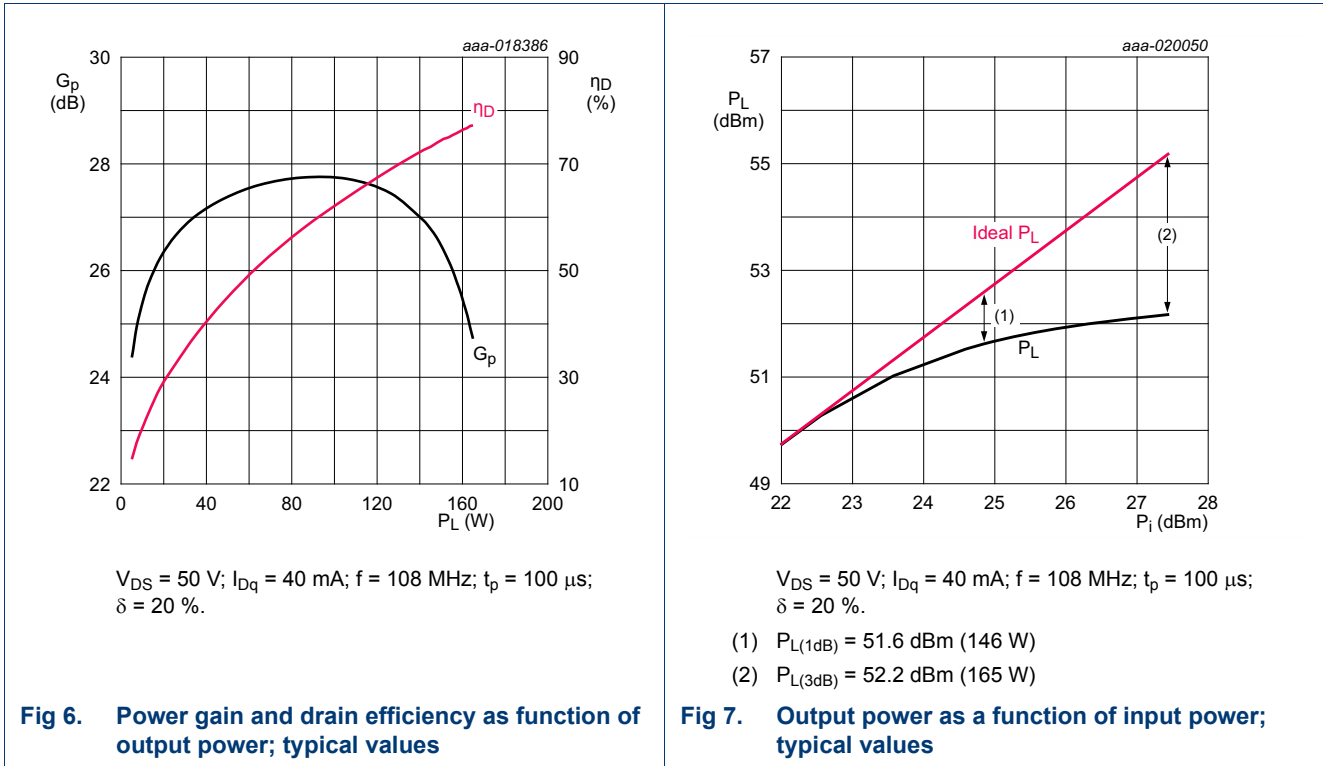
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	68 pF	[1]
C2, C3	multilayer ceramic chip capacitor	220 pF	[1]
C4, C5	multilayer ceramic chip capacitor	4.7 $\mu$ F, 50 V	Kemet: C1210X475K5RAC-T4
C6, C7	multilayer ceramic chip capacitor	750 pF	[1]
C8, C9	multilayer ceramic chip capacitor	4.7 $\mu$ F, 100 V	TDK: C5750X7R2A475KT
C10, C11	multilayer ceramic chip capacitor	750 pF	[1]
C12	multilayer ceramic chip capacitor	10 pF	[1]
C13, C14	multilayer ceramic chip capacitor	43 pF	[1]
C15, C16	multilayer ceramic chip capacitor	390 pF	[1]
C17	multilayer ceramic chip capacitor	47 pF	[1]
C18,C19	electrolytic capacitor	2200 $\mu$ F, 64 V	
L1, L2	wire inductor	5 turns, D = 3 mm, 1 mm copper wire	
L3, L4	wire inductor	6 turns, D = 3 mm, 1 mm copper wire	
R1, R2	resistor	4.7 k $\Omega$	SMD 1206
R3, R4	shunt resistor	0.01 $\Omega$	Ohmite: FC4L110R010FER
R5, R6	metal film resistor	10 $\Omega$ , 0.6 W	
T1, T2	semi rigid coax	50 $\Omega$ , length = 160 mm	EZ Form: EZ-141-AL-TP-M17

[1] American Technical Ceramics type 100B or capacitor of same quality.

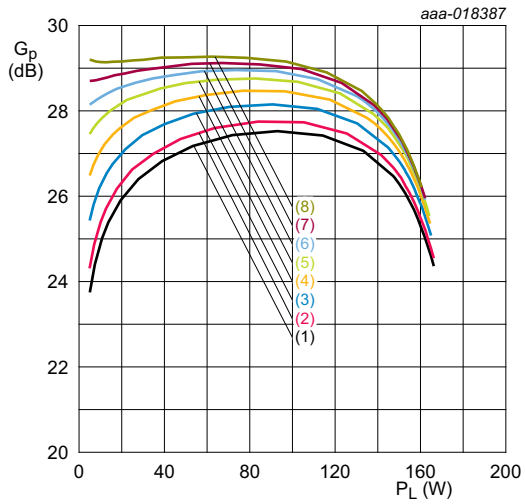
7.5 Graphical data

The following figures are measured in a class-AB production test circuit.

7.5.1 1-Tone CW pulsed



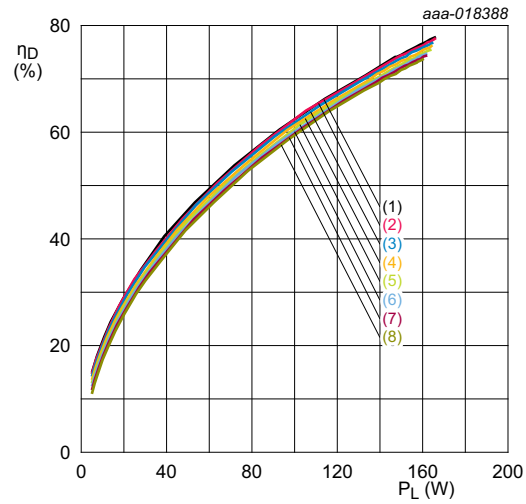




$V_{DS} = 50 \text{ V}; f = 108 \text{ MHz}; t_p = 100 \text{ }\mu\text{s}; \delta = 20 \text{ \%}$ .

- (1)  $I_{Dq} = 20 \text{ mA}$
- (2)  $I_{Dq} = 40 \text{ mA}$
- (3)  $I_{Dq} = 100 \text{ mA}$
- (4)  $I_{Dq} = 200 \text{ mA}$
- (5)  $I_{Dq} = 300 \text{ mA}$
- (6)  $I_{Dq} = 400 \text{ mA}$
- (7)  $I_{Dq} = 500 \text{ mA}$
- (8)  $I_{Dq} = 600 \text{ mA}$

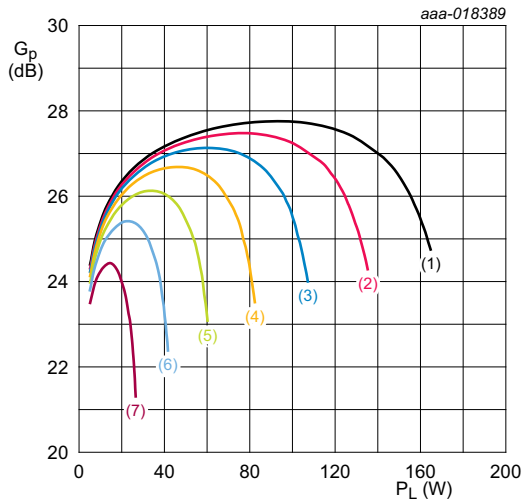
**Fig 8. Power gain as a function of output power; typical values**



$V_{DS} = 50 \text{ V}; f = 108 \text{ MHz}; t_p = 100 \text{ }\mu\text{s}; \delta = 20 \text{ \%}$ .

- (1)  $I_{Dq} = 20 \text{ mA}$
- (2)  $I_{Dq} = 40 \text{ mA}$
- (3)  $I_{Dq} = 100 \text{ mA}$
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- (5)  $I_{Dq} = 300 \text{ mA}$
- (6)  $I_{Dq} = 400 \text{ mA}$
- (7)  $I_{Dq} = 500 \text{ mA}$
- (8)  $I_{Dq} = 600 \text{ mA}$

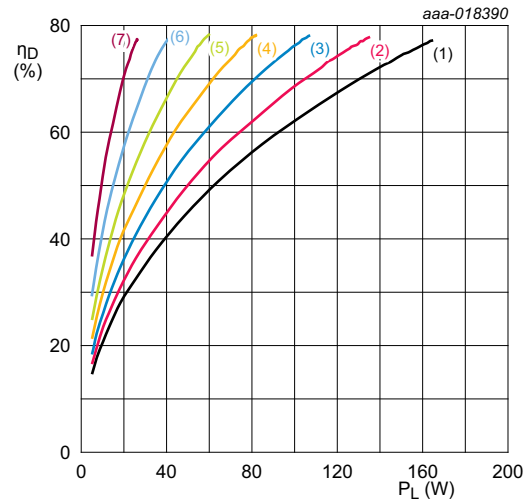
**Fig 9. Drain efficiency as a function of output power; typical values**



$I_{Dq} = 40 \text{ mA}; f = 108 \text{ MHz}; t_p = 100 \text{ }\mu\text{s}; \delta = 20 \text{ \%}.$

- (1)  $V_{DS} = 50 \text{ V}$
- (2)  $V_{DS} = 45 \text{ V}$
- (3)  $V_{DS} = 40 \text{ V}$
- (4)  $V_{DS} = 35 \text{ V}$
- (5)  $V_{DS} = 30 \text{ V}$
- (6)  $V_{DS} = 25 \text{ V}$
- (7)  $V_{DS} = 20 \text{ V}$

**Fig 10. Power gain as a function of output power; typical values**



$I_{Dq} = 40 \text{ mA}; f = 108 \text{ MHz}; t_p = 100 \text{ }\mu\text{s}; \delta = 20 \text{ \%}.$

- (1)  $V_{DS} = 50 \text{ V}$
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- (6)  $V_{DS} = 25 \text{ V}$
- (7)  $V_{DS} = 20 \text{ V}$

**Fig 11. Drain efficiency as a function of output power; typical values**

### 8. Package outline

HSOP4F: plastic, heatsink small outline package; 4 leads(flat)

SOT1223-2

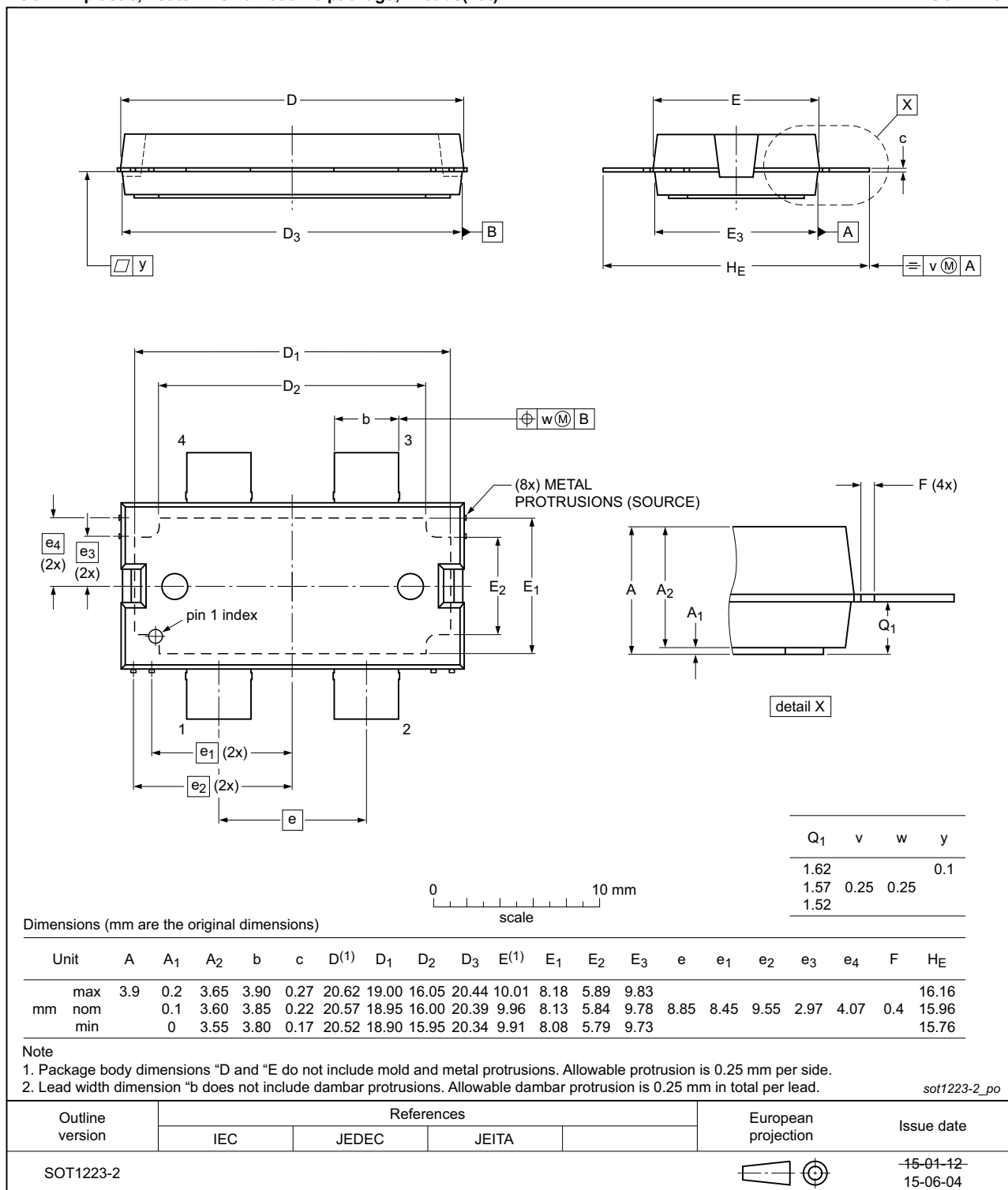


Fig 12. Package outline SOT1223-2 (HSOP4F)

HSOP4: plastic, heatsink small outline package; 4 leads

SOT1224-2

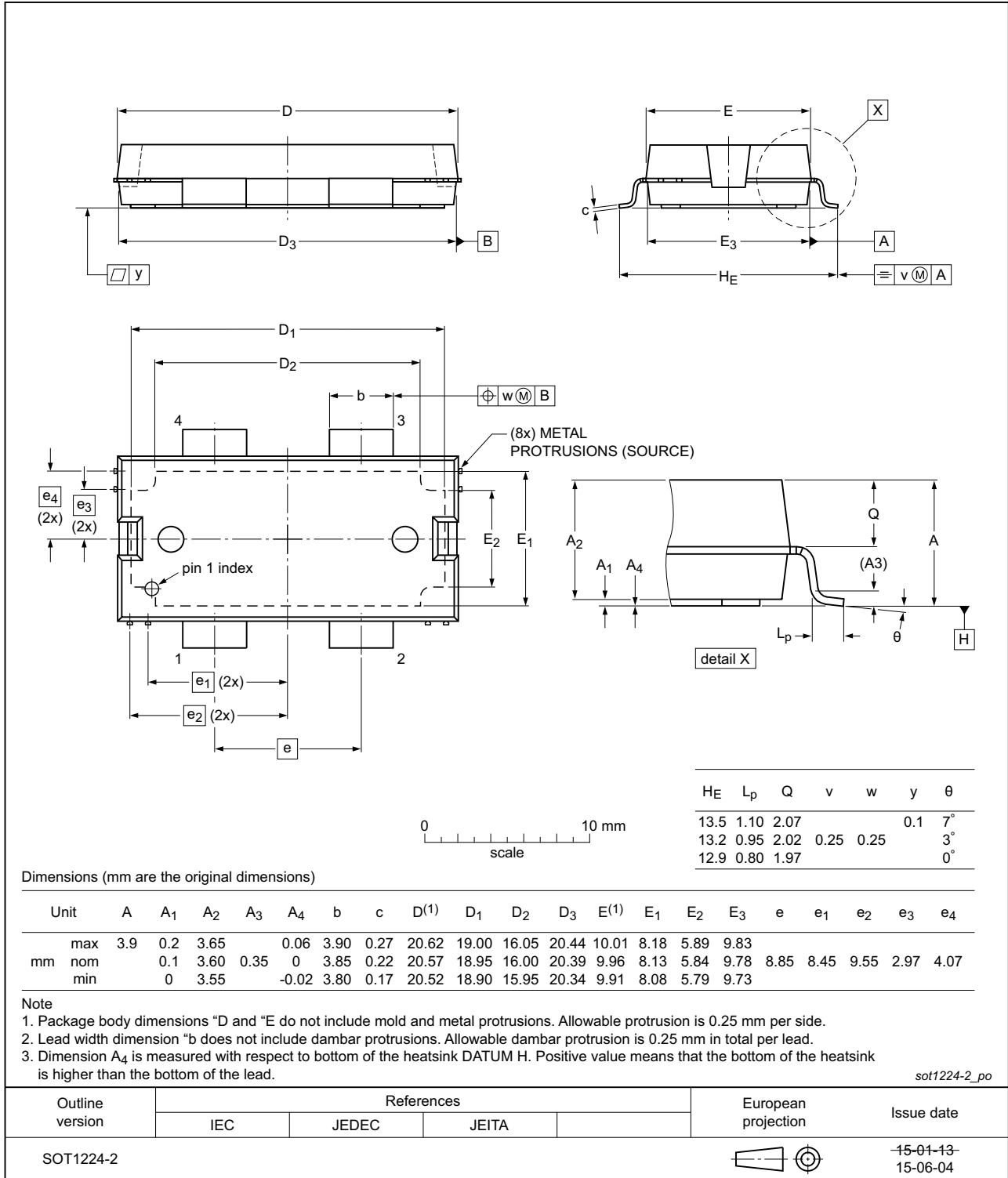


Fig 13. Package outline SOT1224-2 (HSOP4F)

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
UIS	Unclamped Inductive Switching
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP05H6150XR_H6150XRG v.4	20160921	Product data sheet	-	BLP05H6150XR v.3
Modifications	<ul style="list-style-type: none"> <li>The document now describes both the straight lead and gull-wing versions of this product: BLP05H6150XR and BLP05H6150XRG respectively</li> <li><a href="#">Table 2 on page 2</a>: added BLP05H6150XRG data</li> <li><a href="#">Table 3 on page 2</a>: added BLP05H6150XRG data</li> <li><a href="#">Section 7.1 on page 5</a>: added BLP05H6150XRG</li> <li><a href="#">Figure 13 on page 12</a>: added figure SOT1224-2</li> </ul>			
BLP05H6150XR v.3	20160108	Product data sheet	-	BLP05H6150XR#2
BLP05H6150XR#2	20150901	Objective data sheet	-	BLP05H6150XR v.1
BLP05H6150XR v.1	20150518	Objective data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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14. Contents

1 **Product profile** . . . . . 1

1.1 General description . . . . . 1

1.2 Features and benefits . . . . . 1

1.3 Applications . . . . . 1

2 **Pinning information** . . . . . 2

3 **Ordering information** . . . . . 2

4 **Limiting values** . . . . . 2

5 **Thermal characteristics** . . . . . 3

6 **Characteristics** . . . . . 3

7 **Test information** . . . . . 5

7.1 Ruggedness in class-AB operation . . . . . 5

7.2 Impedance information . . . . . 5

7.3 UIS avalanche energy . . . . . 5

7.4 Test circuit . . . . . 7

7.5 Graphical data . . . . . 8

7.5.1 1-Tone CW pulsed . . . . . 8

8 **Package outline** . . . . . 11

9 **Handling information** . . . . . 13

10 **Abbreviations** . . . . . 13

11 **Revision history** . . . . . 13

12 **Legal information** . . . . . 14

12.1 Data sheet status . . . . . 14

12.2 Definitions . . . . . 14

12.3 Disclaimers . . . . . 14

12.4 Licenses . . . . . 15

12.5 Trademarks . . . . . 15

13 **Contact information** . . . . . 15

14 **Contents** . . . . . 16

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