BLP05H6350XR; BLP05H6350XRG Power LDMOS transistor

AMPLEON

Rev. 4 — 21 September 2016

Product data sheet

Product profile

1.1 General description

A 350 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 600 MHz band.

Table 1. **Application information**

Test signal	f	V _{DS}	PL	G _p	η _D
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	108	50	350	27	75

1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 600 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outlin	e Graphic symbol
BLP05H6	6350XR (SOT1223-2)		
1	gate 2		
2	gate 1	4 3	4
3	drain 1		
4	drain 2	pin 1 index	5
5	source	[1]	2
		1 2	'
			aaa-003574
BLP05H6	6350XRG (SOT1224-2)		
1	gate 2		
2	gate 1	4 3	-
3	drain 1	□ ○ pin 1 index	
4	drain 2	pin 1 index	5
5	source	[1] 1 2	
			'
			aaa-003574

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package			
	Name	Description	Version	
BLP05H6350XR	HSOP4F	plastic, heatsink small outline package; 4 leads (flat)	SOT1223-2	
BLP05H6350XRG	HSOP4F	plastic, heatsink small outline package; 4 leads	SOT1224-2	

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	135	V
V_{GS}	gate-source voltage		-6	+11	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

^[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

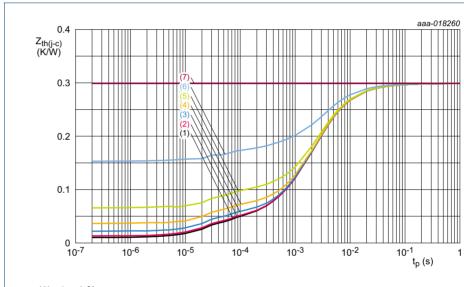
BLP05H6350XR_H6350XRG

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	T _j = 115 °C	[1][2]	0.30	K/W
Z _{th(j-c)}	transient thermal impedance from junction to case	T_j = 150 °C; t_p = 100 μs; δ = 20 %	[3]	0.098	K/W

- [1] T_i is the junction temperature.
- [2] $R_{th(j-c)}$ is measured under RF conditions.
- [3] See Figure 1.



- (1) $\delta = 1 \%$
- (2) $\delta = 2 \%$
- (3) $\delta = 5 \%$
- (4) $\delta = 10 \%$
- (5) $\delta = 20 \%$
- (6) $\delta = 50 \%$
- (7) $\delta = 100 \% (DC)$

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics

 $T_j = 25$ °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 1.5 \text{ mA}$	135	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_{D} = 150 mA	1.33	2.0	2.33	٧
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_{D} = 50 mA	-	1.9	-	V

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Table 6. DC characteristics ...continued

 T_i = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{DSS}	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}$	-	-	1.4	μΑ
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	21	-	Α
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	140	nA
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ $I_D = 5.25 A$	-	0.29	-	Ω

Table 7. AC characteristics

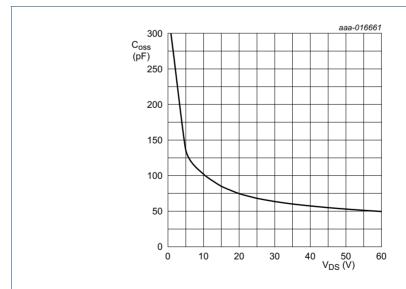
 T_i = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _{rs}	feedback capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	-	1.3	-	pF
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	161	-	pF
Coss	output capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	53	-	pF

Table 8. RF characteristics

Test signal: pulsed RF; t_p = 100 μ s; δ = 20 %; f = 108 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 100 mA; T_{case} = 25 $^{\circ}$ C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	P _L = 350 W	26.5	27.5	-	dB
RLin	input return loss	P _L = 350 W	-	-10	-	dB
η_{D}	drain efficiency	P _L = 350 W	71	75	-	%



 $V_{GS} = 0 \text{ V; } f = 1 \text{ MHz.}$

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

7. Test information

7.1 Ruggedness in class-AB operation

The BLP05H6350XR and BLP05H6350XRG are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions: $V_{DS} = 50 \text{ V}$; $I_{Dq} = 100 \text{ mA}$; $P_L = 350 \text{ W}$ pulsed; f = 108 MHz.

7.2 Impedance information

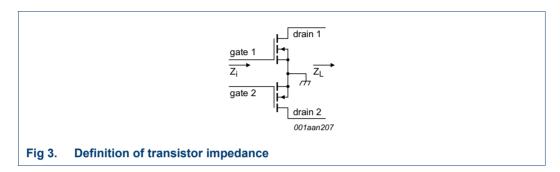


Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 50 V and P_L = 350 W.

f	Z _i	Z _L
(MHz)	(Ω)	(Ω)
108	10.6 – j36.2	10.8 + j2.5

7.3 UIS avalanche energy

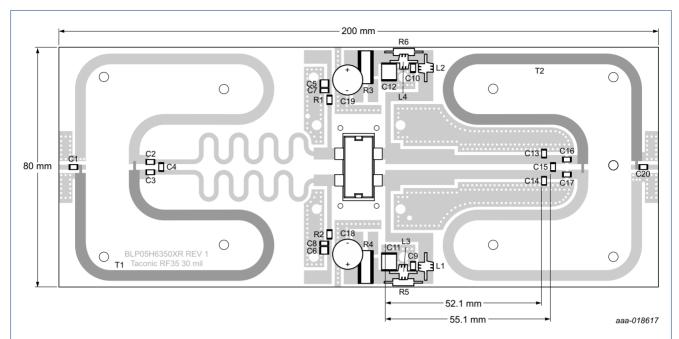
Table 10. Typical avalanche data per section

 T_{amb} = 25 °C; typical test data; test jig without water cooling.

las	E _{AS}
	(J)
10	1.8
12.5	1.3
15	0.9

For information see application note AN10273.

7.4 Test circuit



Printed-Circuit Board (PCB): Taconic RF-35; ϵ_r = 3.5 F/m; thickness = 0.765 mm; thickness copper plating = 35 μ m, gold plated.

See Table 11 for a list of components.

Fig 4. Component layout for class-AB production test circuit

Table 11. List of components

For test circuit see Figure 4.

Component	Description	Value	Remarks
C1, C4	multilayer ceramic chip capacitor	51 pF [1]	
C2, C3	multilayer ceramic chip capacitor	150 pF [1]	
C5, C6	multilayer ceramic chip capacitor	4.7 μF, 50 V	
C7, C8	multilayer ceramic chip capacitor	820 pF [1]	
C9, C10	multilayer ceramic chip capacitor	820 pF [1]	
C11, C12	multilayer ceramic chip capacitor	4.7 μF, 100 V	
C13, C14	multilayer ceramic chip capacitor	62 pF [1]	
C15	electrolytic capacitor	7.5 pF [1]	
C16, C17	multilayer ceramic chip capacitor	110 pF [1]	
C18,C19	electrolytic capacitor	2200 μF, 64 V	
C20	multilayer ceramic chip capacitor	51 pF [1]	
L1, L2, L3, L4	wire inductor	3 turns, D = 3 mm, 1 mm copper wire	
R1, R2	resistor	510 Ω	SMD 1206
R3, R4	shunt resistor	0.01 Ω	Ohmite: FC4L110R010FER
R5, R6	metal film resistor	10 Ω, 0.6 W	
T1, T2	semi rigid coax	50 Ω, length = 160 mm	EZ Form: EZ-141-AL-TP-M17

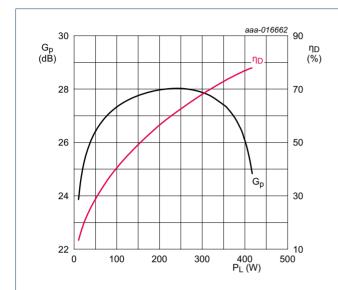
^[1] American Technical Ceramics type 100B or capacitor of same quality.

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7.5 Graphical data

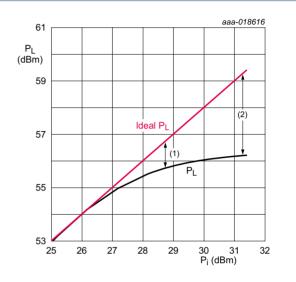
The following figures are measured in a class-AB production test circuit.

7.5.1 1-Tone CW pulsed



 V_{DS} = 50 V; I_{Dq} = 100 mA; f = 108 MHz; t_p = 100 $\mu s;$ δ = 20 %.

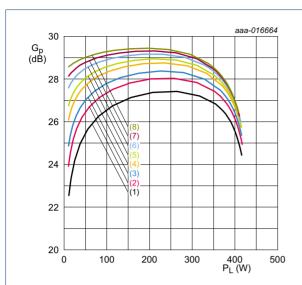
Fig 5. Power gain and drain efficiency as function of output power; typical values



 V_{DS} = 50 V; I_{Dq} = 100 mA; f = 108 MHz; t_p = 100 $\mu s;$ δ = 20 %.

- (1) $P_{L(1dB)} = 55.7 \text{ dBm } (372 \text{ W})$
- (2) $P_{L(3dB)} = 56.2 \text{ dBm } (415 \text{ W})$

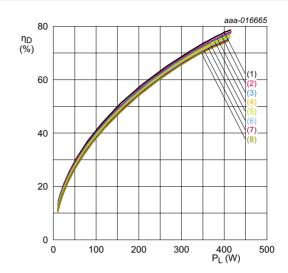
Fig 6. Output power as a function of input power; typical values



 V_{DS} = 50 V; f = 108 MHz; t_p = 100 μ s; δ = 20 %.

- (1) $I_{Dq} = 20 \text{ mA}$
- (2) $I_{Dq} = 100 \text{ mA}$
- (3) $I_{Dq} = 200 \text{ mA}$
- (4) $I_{Dq} = 400 \text{ mA}$
- (5) $I_{Dq} = 600 \text{ mA}$
- (6) $I_{Dq} = 800 \text{ mA}$
- (7) $I_{Dq} = 1000 \text{ mA}$
- (8) $I_{Dq} = 1200 \text{ mA}$

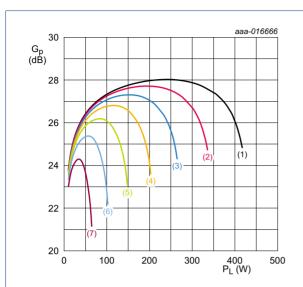
Fig 7. Power gain as a function of output power; typical values



 V_{DS} = 50 V; f = 108 MHz; t_p = 100 μ s; δ = 20 %.

- (1) $I_{Dq} = 20 \text{ mA}$
- (2) $I_{Dq} = 100 \text{ mA}$
- (3) $I_{Dq} = 200 \text{ mA}$
- (4) $I_{Dq} = 400 \text{ mA}$
- (5) $I_{Dq} = 600 \text{ mA}$
- (6) $I_{Dq} = 800 \text{ mA}$
- (7) $I_{Dq} = 1000 \text{ mA}$
- (8) $I_{Dq} = 1200 \text{ mA}$

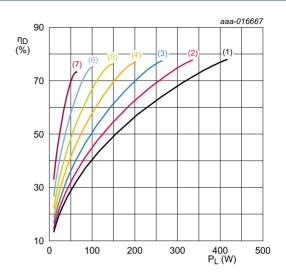
Fig 8. Drain efficiency as a function of output power; typical values



 I_{Dq} = 100 mA; f = 108 MHz; t_p = 100 μ s; δ = 20 %.

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$
- (4) $V_{DS} = 35 \text{ V}$
- (5) $V_{DS} = 30 \text{ V}$
- (6) $V_{DS} = 25 \text{ V}$
- (7) $V_{DS} = 20 \text{ V}$

Fig 9. Power gain as a function of output power; typical values



 I_{Dq} = 100 mA; f = 108 MHz; t_p = 100 μ s; δ = 20 %.

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$
- (4) $V_{DS} = 35 V$
- (5) $V_{DS} = 30 \text{ V}$ (6) $V_{DS} = 25 \text{ V}$
- (7) $V_{DS} = 20 \text{ V}$

Fig 10. Drain efficiency as a function of output power; typical values

Package outline

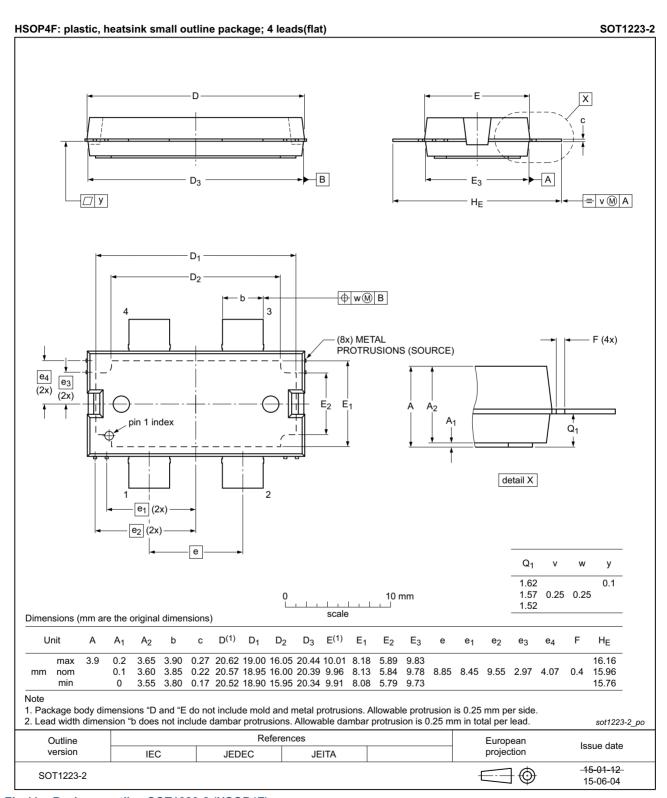


Fig 11. Package outline SOT1223-2 (HSOP4F)

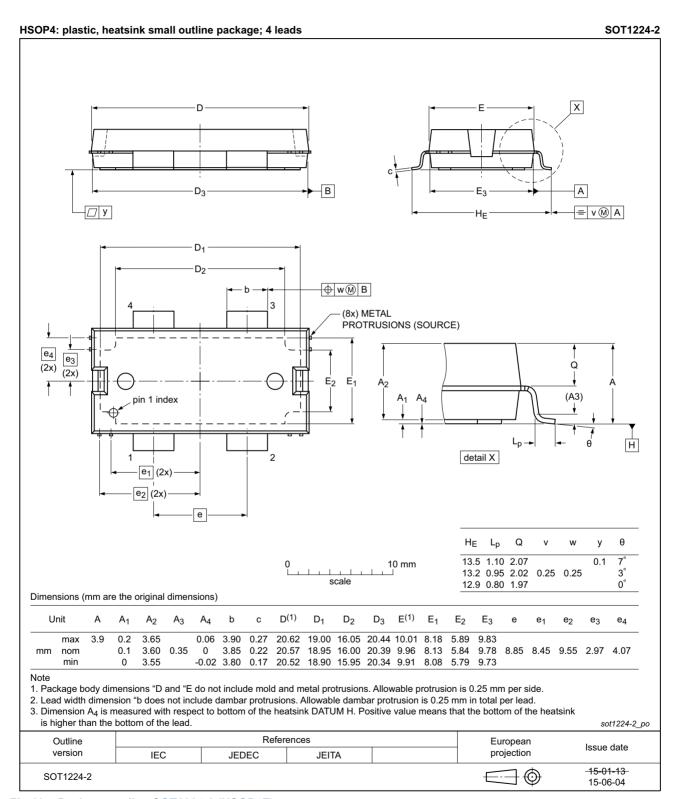


Fig 12. Package outline SOT1224-2 (HSOP4F)

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
UIS	Unclamped Inductive Switching
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BLP05H6350XR_H6350XRG v.4	20160921	Product data sheet	-	BLP05H6350XR v.3	
Modifications:	 The document now describes both the straight lead and gull-wing versions of this product: BLP05H6350XR and BLP05H6350XRG respectively 				
	 <u>Table 2 on page 2</u>: added BLP05H6350XRG data 				
	 <u>Table 3 on page 2</u>: added BLP05H6350XRG data 				
	Section 7.1 on page 5: added BLP05H6350XRG				
	Figure 12 on page 11: added figure SOT1224-2				
BLP05H6350XR v.3	20151012	Product data sheet	-	BLP05H6350XR#2	
BLP05H6350XR#2	20150901	Preliminary data sheet	-	BLP05H6350XR v.1	
BLP05H6350XR v.1	20150703	Preliminary data sheet	-	-	

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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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