BLP10H603

Broadband LDMOS driver transistor

Rev. 1 — 2 October 2014 **Product data sheet**

1. Product profile

1.1 General description

A 2.5 W plastic LDMOS power transistor for broadcast transmitter and ISM applications at frequencies from HF to 1400 MHz.

Table 1. Application performance

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	860	50	2.5	22.8	62

1.2 Features and benefits

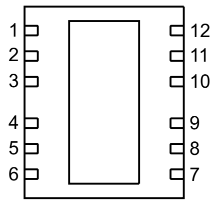
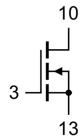
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 1400 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1, 2, 4, 5, 6, 7, 8, 9, 11, 12	n.c.	 Transparent top view	 aaa-012010
3	gate1		
10	drain1		
13	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP10H603	HVSON12	plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 5 × 6 × 0.85 mm	SOT1352-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	104	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	150	°C

5. Recommended operating conditions

See application note *AN11520* for more details.

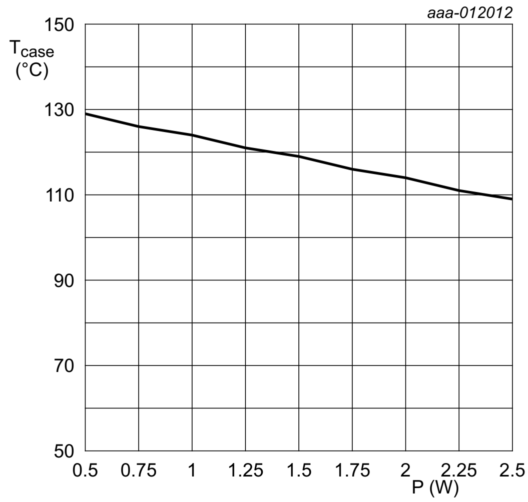


Fig 1. Recommended operating area; case temperature as a function of power dissipation

6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 2.5 W [1]	9.9	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions

7. Characteristics

Table 6. DC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.03 mA	104	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 3 mA	1.25	1.65	2.25	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 15 mA	1.3	1.73	2.15	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	0.5	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 105 mA	-	9	-	Ω

Table 7. AC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	0.03	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 0 V; f = 1 MHz	-	3.4	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	1.12	-	pF

Table 8. RF characteristics

Test signal: pulsed CW; f = 860 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 15 mA; t_p = 50 μs; δ = 10 %; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 2.5 W	21.4	22.8	25.5	dB
η_D	drain efficiency	P_L = 2.5 W	60	62	-	%

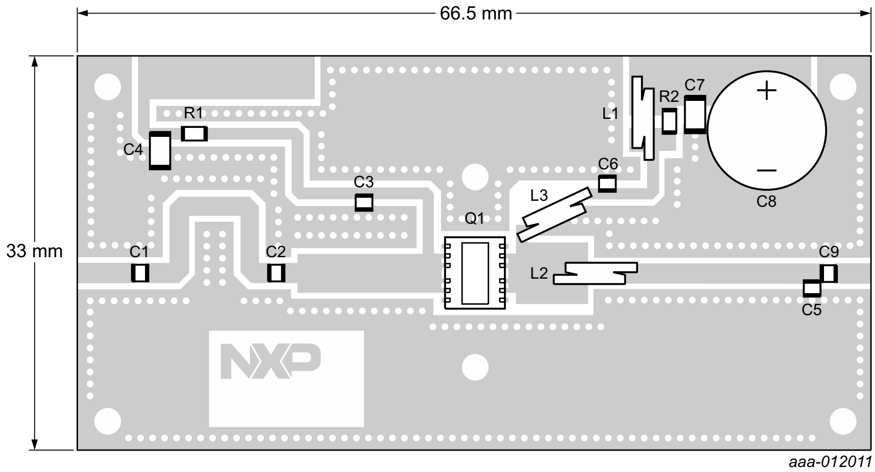
[1] The industrial test method is performed on special hardware to accommodate the requirements of production. The test results in this table are correlated to correspond with a performance in the application.

8. Test information

8.1 Ruggedness in class-AB operation

The BLP10H603 is capable of withstanding a load mismatch corresponding to VSWR = 35 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 15 mA; P_L = 2.5 W; f = 860 MHz.

8.2 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350; ε_r = 3.48; height = 0.762 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 2. Component layout

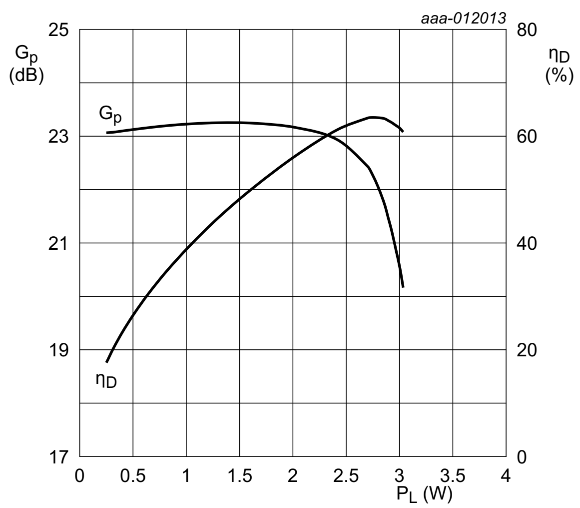
Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value		Remarks
C1, C3, C6, C9	multilayer ceramic chip capacitor	100 pF	[1]	
C2	multilayer ceramic chip capacitor	3.9 pF	[1]	
C4	multilayer ceramic chip capacitor	1 μF, 25 V		Murata GRM31MR71E105KA01L
C5	multilayer ceramic chip capacitor	4.7 pF	[1]	
C7	multilayer ceramic chip capacitor	1 μF, 50 V		Murata GRM32RR71H105KA01L
C8	electrolytic capacitor	220 μF, 63 V		
L1	wire inductor, 0.8 mm copper wire	2 turn, D = 3 mm		
L2	wire inductor, 0.8 mm copper wire	2 turn, D = 2.7 mm		
L3	wire inductor, 0.8 mm copper wire	2 turn, D = 3 mm		
R1	resistor	0 Ω		SMD 0805
R2	resistor	10 Ω		SMD 0805
Q1	transistor	-		BLP10H603

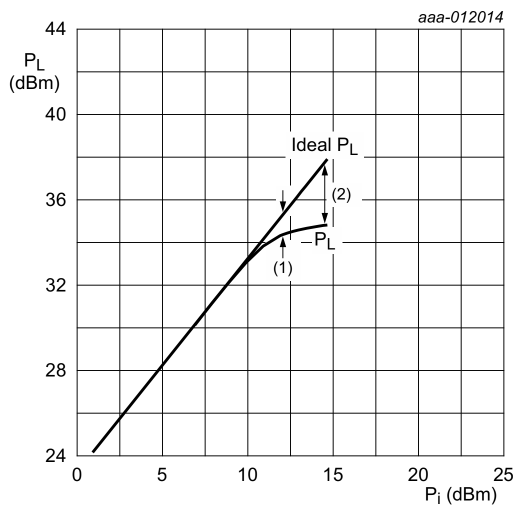
[1] American Technical Ceramics type 100A or capacitor of same quality.

8.3 Graphical data



V_{DS} = 50 V; I_{Dq} = 15 mA; f = 860 MHz.

Fig 3. Power gain and drain efficiency as function of output power; typical values

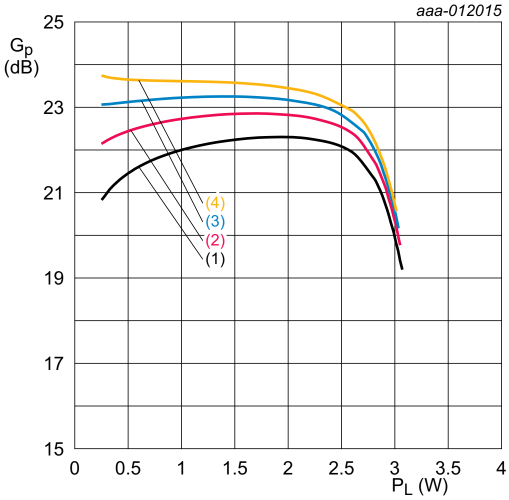


V_{DS} = 50 V; I_{Dq} = 15 mA; f = 860 MHz.

(1) $P_{L(1dB)}$ = 34.4 dBm (2.8 W)

(2) $P_{L(3dB)}$ = 34.8 dBm (3.0 W)

Fig 4. Output power as a function of input power; typical values



V_{DS} = 50 V; f = 860 MHz.

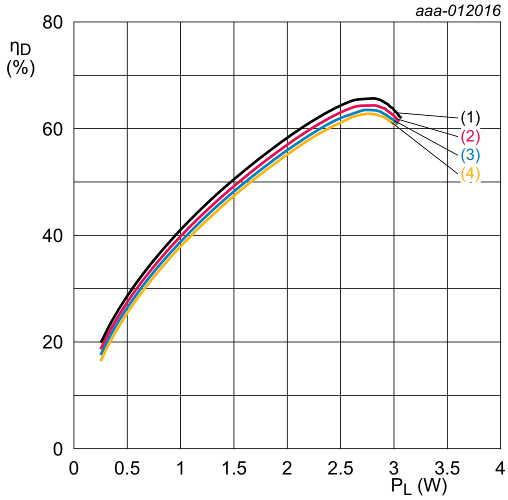
(1) I_{Dq} = 5 mA

(2) I_{Dq} = 10 mA

(3) I_{Dq} = 15 mA

(4) I_{Dq} = 20 mA

Fig 5. Power gain as a function of output power; typical values



V_{DS} = 50 V; f = 860 MHz.

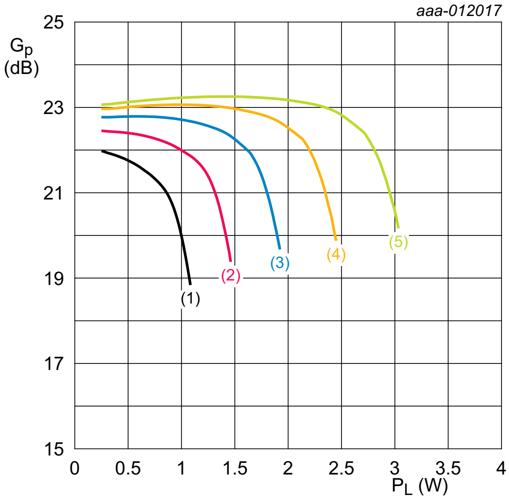
(1) I_{Dq} = 5 mA

(2) I_{Dq} = 10 mA

(3) I_{Dq} = 15 mA

(4) I_{Dq} = 20 mA

Fig 6. Drain efficiency as a function of output power; typical values



I_{Dq} = 15 mA; f = 860 MHz.

(1) V_{DS} = 30 V

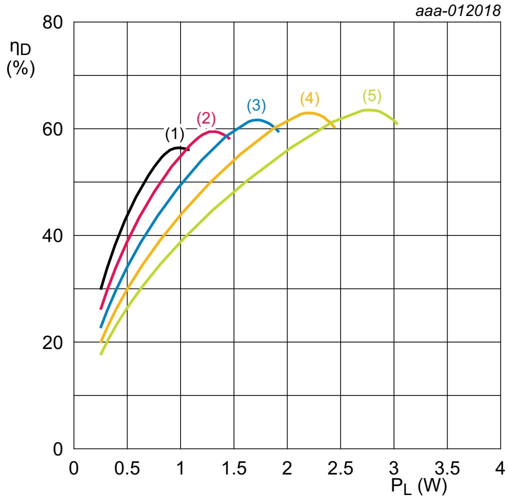
(2) V_{DS} = 35 V

(3) V_{DS} = 40 V

(4) V_{DS} = 45 V

(5) V_{DS} = 50 V

Fig 7. Power gain as a function of output power; typical values



I_{Dq} = 15 mA; f = 860 MHz.

(1) V_{DS} = 30 V

(2) V_{DS} = 35 V

(3) V_{DS} = 40 V

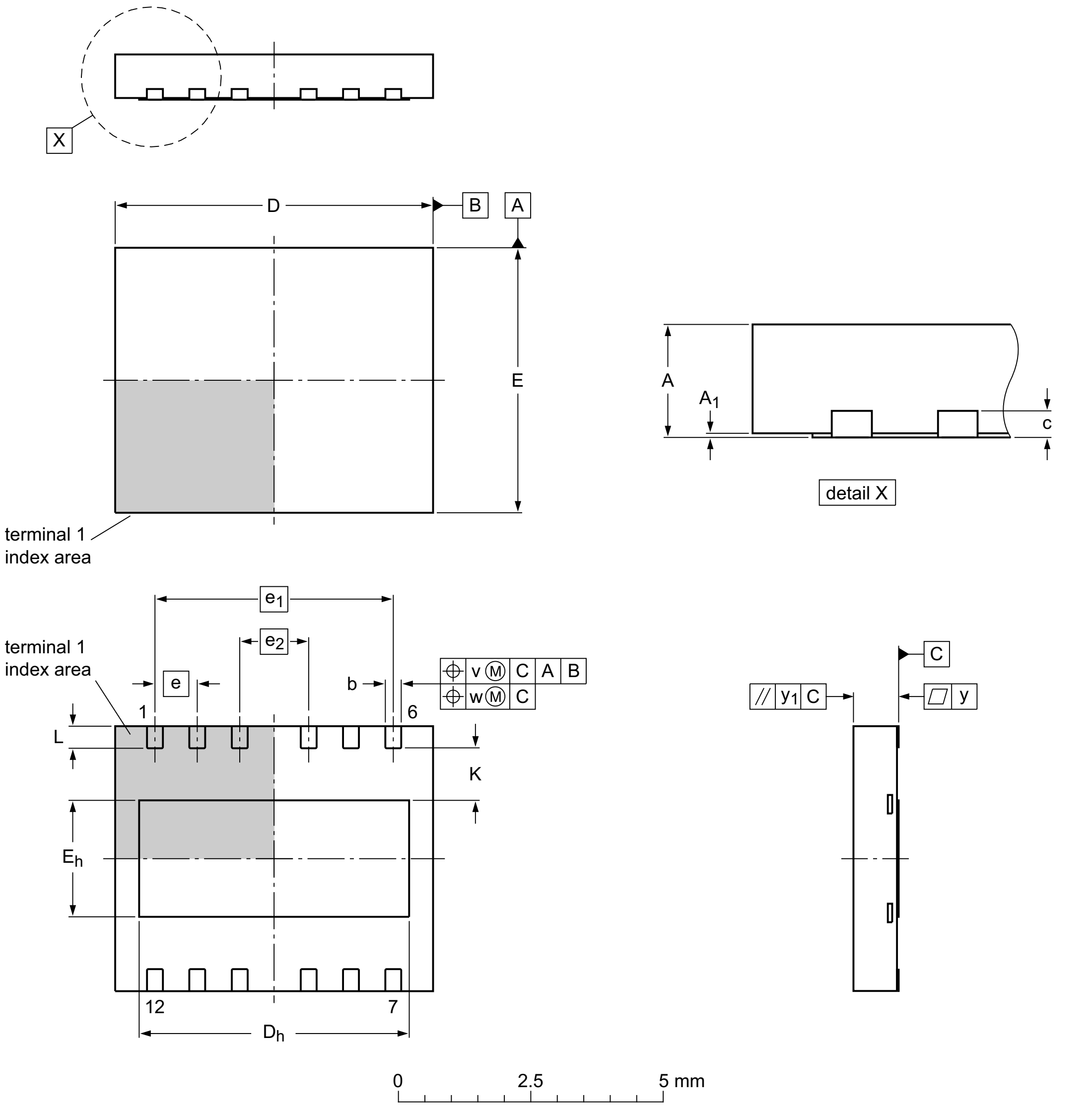
(4) V_{DS} = 45 V

(5) V_{DS} = 50 V

Fig 8. Drain efficiency as a function of output power; typical values

9. Package outline

HVSON12: plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 5 x 6 x 0.85 mm **SOT1352-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	K	L	v	w	y	y_1
	max	1.00	0.05	0.35		6.1	5.2	5.1	2.3					0.5				
mm	nom	0.85	0.03	0.30	0.2	6.0	5.1	5.0	2.2	0.8	4.5	1.3		0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.25		5.9	5.0	4.9	2.1				1.0	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1352-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1352-1	- - -	MO-229	- - -			~~13-03-26~~ 13-07-16

Fig 9. Package outline SOT1352-1 (HVSON12)

10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
HF	High Frequency
ISM	Industrial, Scientific and Medical
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP10H603 v.1	20141002	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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15. Contents

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