BLP10H6120P; BLP10H6120PG

Power LDMOS transistor

AMPLEON

Rev. 1 — 20 December 2016

Product data sheet

1. Product profile

1.1 General description

A 120 W LDMOS power transistor for broadcast and industrial applications in the HF to 1000 MHz band.

Table 1. Application information

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	720	50	120	18	72
pulsed RF	915	50	160	14.9	70.2
CW	915	50	143	15.1	62.3

1.2 Features and benefits

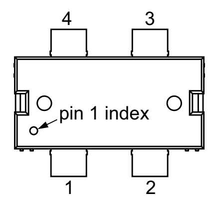
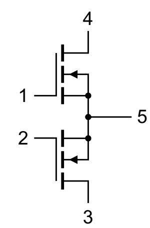
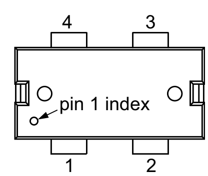
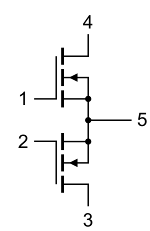
- Easy power control
- Integrated dual sided ESD protection enables class C operation and complete switch off of the transistor
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 1000 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLP10H6120P (SOT1223-2)			
1	gate 2		 aaa-003574
2	gate 1		
3	drain 1		
4	drain 2		
5	source [1]		
BLP10H6120PG (SOT1224-2)			
1	gate 2		 aaa-003574
2	gate 1		
3	drain 1		
4	drain 2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP10H6120P	HSOP4F	plastic, heatsink small outline package; 4 leads (flat)	SOT1223-2
BLP10H6120PG	HSOP4	plastic, heatsink small outline package; 4 leads	SOT1224-2

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

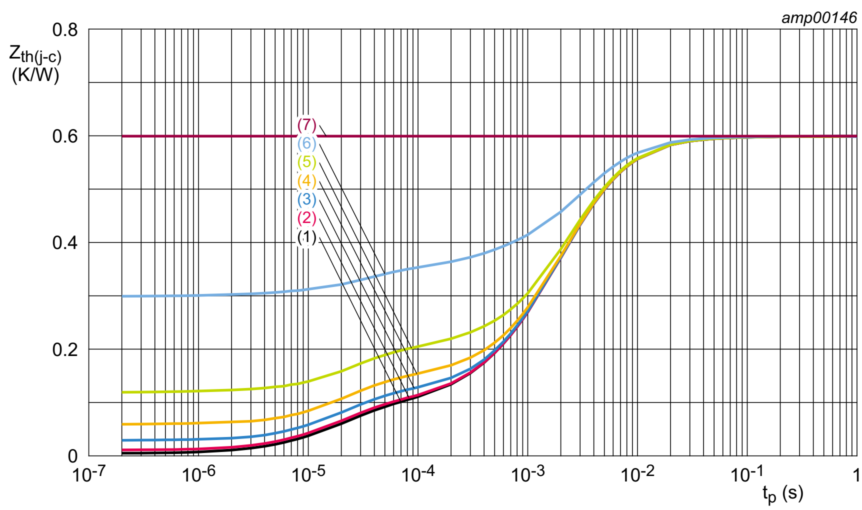
Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_j = 125 °C	[1][2]	0.6	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_j = 150 °C; t_p = 100 μs; δ = 20 %	[3]	0.21	K/W

[1] T_j is the junction temperature.

[2] $R_{th(j-c)}$ is measured under RF conditions.

[3] See Figure 1.



(1) δ = 1 %

(2) δ = 2 %

(3) δ = 5 %

(4) δ = 10 %

(5) δ = 20 %

(6) δ = 50 %

(7) δ = 100 % (DC)

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 500 μA	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 50 mA	1.25	1.9	2.25	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 20 mA	-	1.7	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA

Table 6. DC characteristics *...continued*

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	7.8	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 3.75 V; I_D = 1.75 A	-	0.6	-	Ω

Table 7. AC characteristics

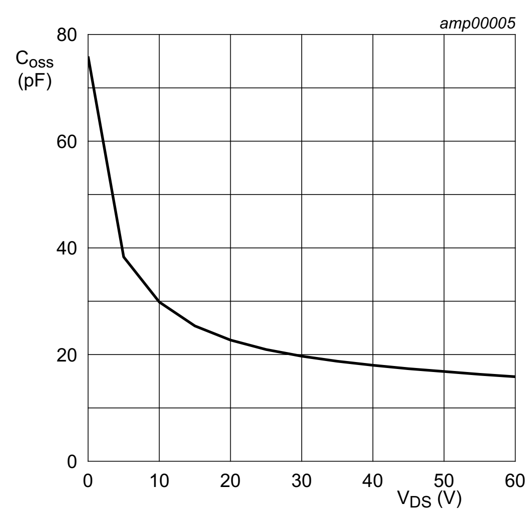
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	0.31	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	55.1	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	16.8	-	pF

Table 8. RF characteristics

Test signal: pulsed RF; t_p = 100 μs; δ = 20 %; f = 720 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 80 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 120 W	16.8	18	-	dB
RL_{in}	input return loss	P_L = 120 W	-	−20	-	dB
η_D	drain efficiency	P_L = 120 W	70	72	-	%



V_{GS} = 0 V; f = 1 MHz.

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

7. Test information

7.1 Ruggedness in class-AB operation

The BLP10H6120P and BLP10H6120PG are capable of withstanding a load mismatch corresponding to VSWR > 40 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 80 mA; P_L = 120 W pulsed; f = 720 MHz.

7.2 Impedance information

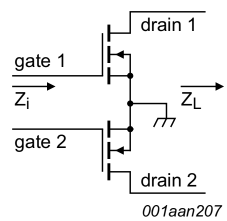


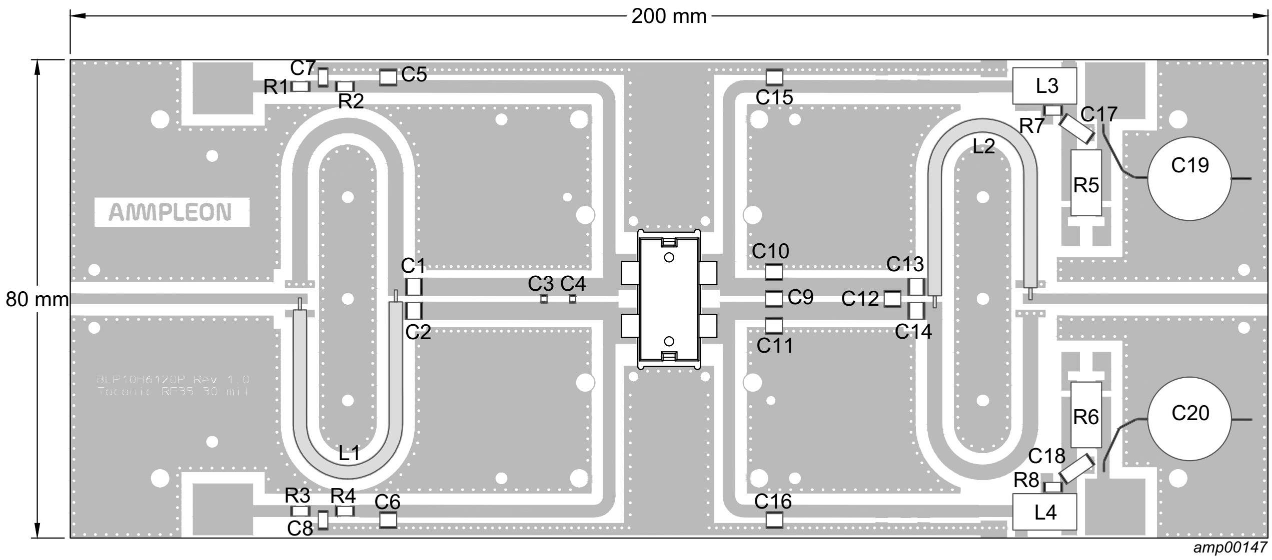
Fig 3. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 50 V and P_L = 120 W.

f	Z_i	Z_L
(MHz)	(Ω)	(Ω)
720	4.4 – j6.4	10 + j11.2

7.3 Test circuit



Printed-Circuit Board (PCB): RF-35; ε_r = 3.5 F/m; thickness = 0.765 mm; thickness copper plating = 35 μm.

See Table 10 for a list of components.

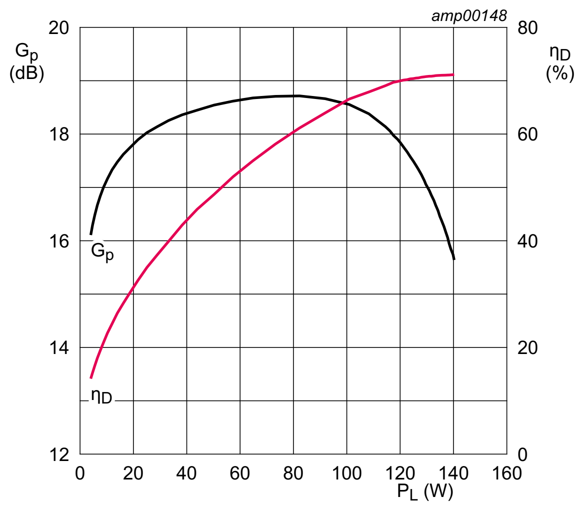
Fig 4. Component layout for class-AB production test circuit

Table 10. List of components

For test circuit see Figure 4.

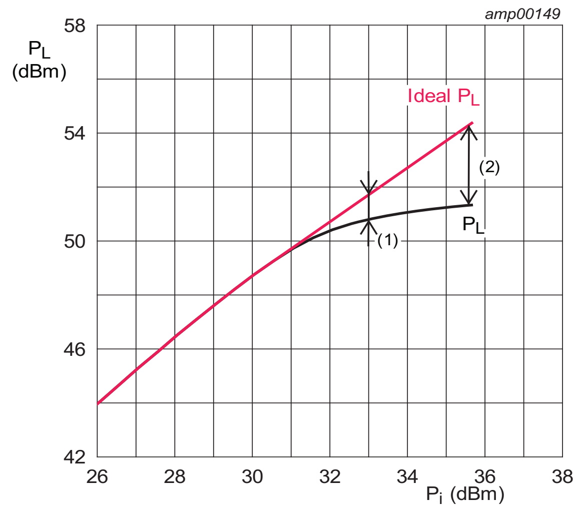
Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	15 pF	ATC 800B
C3	multilayer ceramic chip capacitor	4.3 pF	ATC 100A
C4	multilayer ceramic chip capacitor	9.1 pF	ATC 100A
C5, C6	multilayer ceramic chip capacitor	150 pF	ATC 100A
C7, C8	electrolytic capacitor	1 μF, 50 V	GRM32RR71H105KA01L
C9	multilayer ceramic chip capacitor	11 pF	ATC 800B
C10, C11	multilayer ceramic chip capacitor	10 pF	ATC 800B
C12	multilayer ceramic chip capacitor	6.2 pF	ATC 800B
C13, C14	multilayer ceramic chip capacitor	33 pF	ATC 800B
C15, C16	multilayer ceramic chip capacitor	150 pF	ATC 800B
C17, C18	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK: C5750X7R2A475KT/A
C19, C20	electrolytic capacitor	1000 μF, 63 V	Vishay
L1	coaxial balun	L = 64.8 mm	EZ_86_TP_M17
L2	coaxial balun	L = 64.8 mm	EZ_86_TP_M17
L3, L4	inductor	90 nH	132-9SMGL
R1, R2, R3, R4	resistor	4.7 Ω	SMD 1206
R5, R6	resistor	10 mΩ, 5 W	FCL4L110R010FER
R7, R8	resistor	7.5 Ω	SMD 1206

7.4 Graphical data



V_{DS} = 50 V; I_{Dq} = 80 mA; f = 720 MHz; t_p = 100 μs; δ = 20 %.

Fig 5. Power gain and drain efficiency as function of output power; typical values

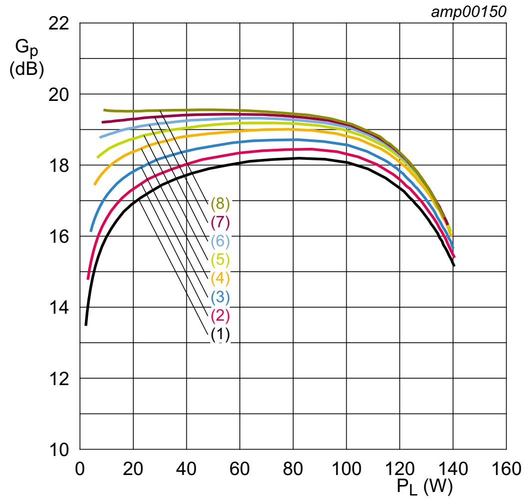


V_{DS} = 50 V; I_{Dq} = 80 mA; f = 720 MHz; t_p = 100 μs; δ = 20 %.

(1) $P_{L(1dB)}$ = 50.8 dBm (120 W) at P_i = 33 dBm

(2) $P_{L(3dB)}$ = 51.3 dBm (135.7 W) at P_i = 35.6 dBm

Fig 6. Output power as a function of input power; typical values



V_{DS} = 50 V; f = 720 MHz; t_p = 100 μs; δ = 20 %.

(1) I_{Dq} = 20 mA

(2) I_{Dq} = 40 mA

(3) I_{Dq} = 80 mA

(4) I_{Dq} = 160 mA

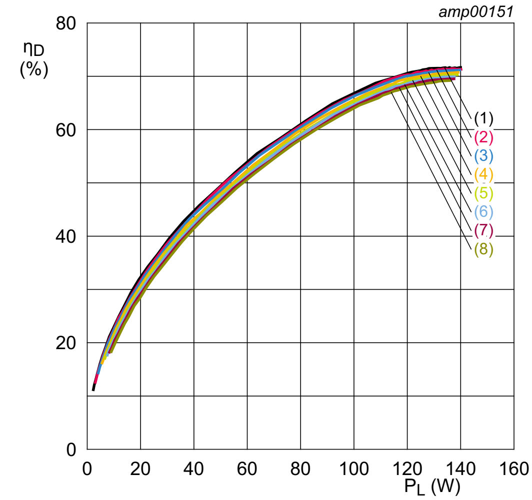
(5) I_{Dq} = 240 mA

(6) I_{Dq} = 320 mA

(7) I_{Dq} = 400 mA

(8) I_{Dq} = 480 mA

Fig 7. Power gain as a function of output power; typical values



V_{DS} = 50 V; f = 720 MHz; t_p = 100 μs; δ = 20 %.

(1) I_{Dq} = 20 mA

(2) I_{Dq} = 40 mA

(3) I_{Dq} = 80 mA

(4) I_{Dq} = 160 mA

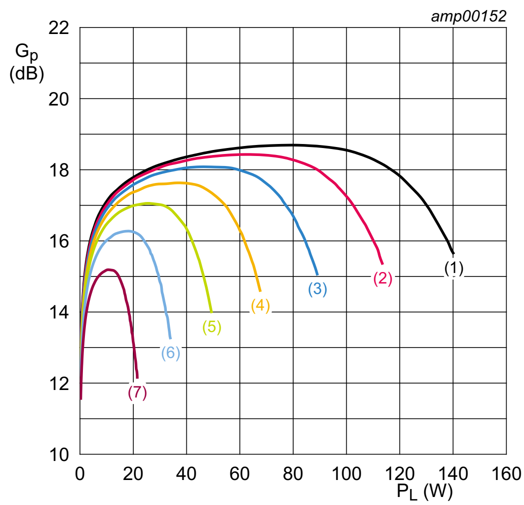
(5) I_{Dq} = 240 mA

(6) I_{Dq} = 320 mA

(7) I_{Dq} = 400 mA

(8) I_{Dq} = 480 mA

Fig 8. Drain efficiency as a function of output power; typical values



I_{Dq} = 80 mA; f = 720 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 50 V

(2) V_{DS} = 45 V

(3) V_{DS} = 40 V

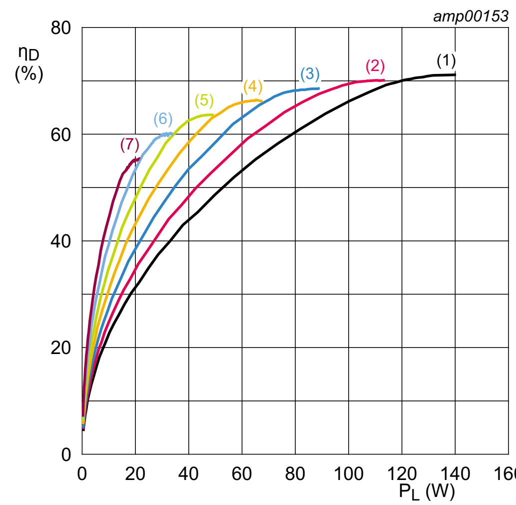
(4) V_{DS} = 35 V

(5) V_{DS} = 30 V

(6) V_{DS} = 25 V

(7) V_{DS} = 20 V

Fig 9. Power gain as a function of output power; typical values



I_{Dq} = 80 mA; f = 720 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 50 V

(2) V_{DS} = 45 V

(3) V_{DS} = 40 V

(4) V_{DS} = 35 V

(5) V_{DS} = 30 V

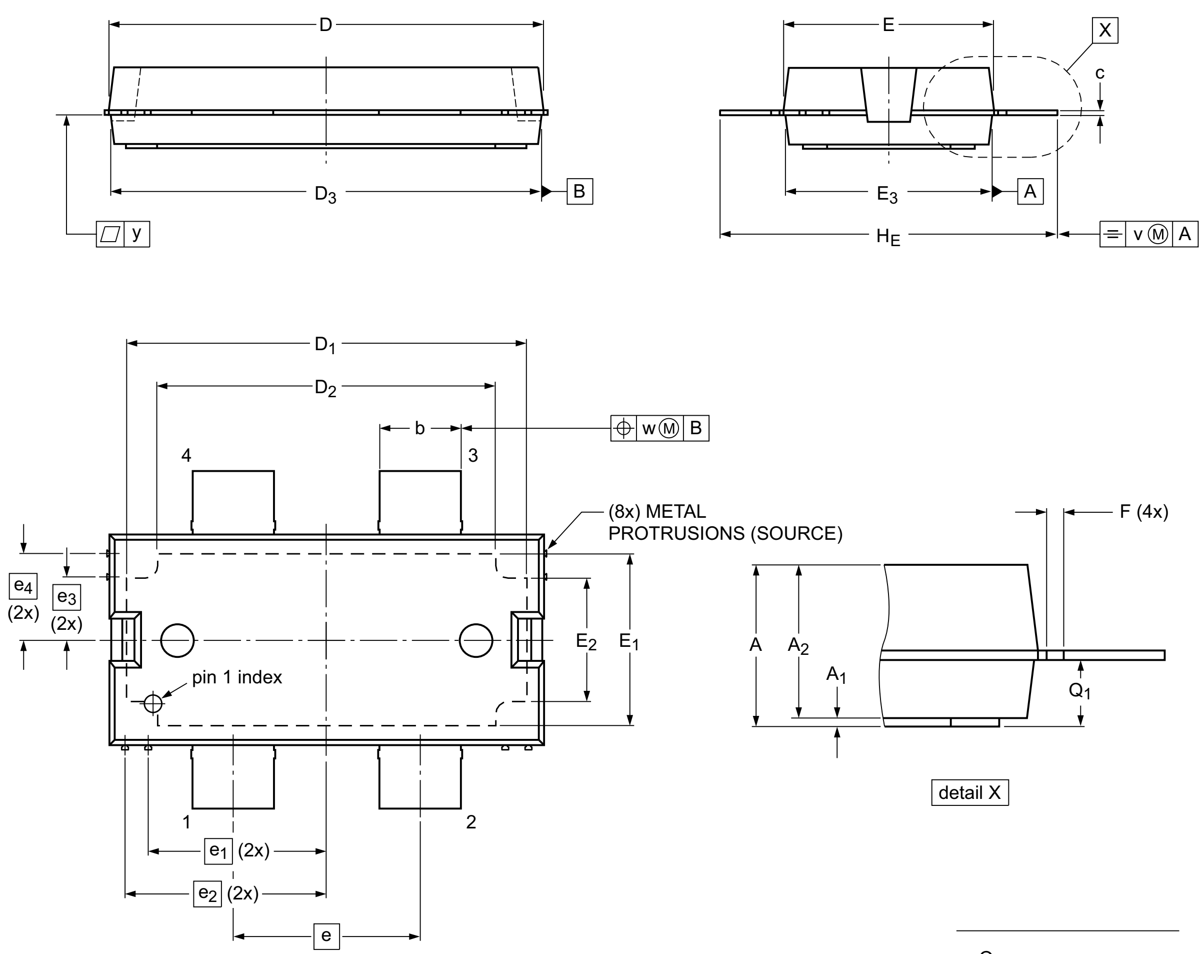
(6) V_{DS} = 25 V

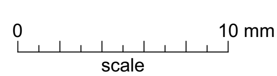
(7) V_{DS} = 20 V

Fig 10. Drain efficiency as a function of output power; typical values

8. Package outline

HSOP4F: plastic, heatsink small outline package; 4 leads(flat) **SOT1223-2**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	c	D(1)	D_1	D_2	D_3	E(1)	E_1	E_2	E_3	e	e_1	e_2	e_3	e_4	F	H_E	Q_1	v	w	y
	max	3.9	0.2	3.65	3.90	0.27	20.62	19.00	16.05	20.44	10.01	8.18	5.89	9.83							16.16	1.62			0.1
mm	nom		0.1	3.60	3.85	0.22	20.57	18.95	16.00	20.39	9.96	8.13	5.84	9.78	8.85	8.45	9.55	2.97	4.07	0.4	15.96	1.57	0.25	0.25	
	min		0	3.55	3.80	0.17	20.52	18.90	15.95	20.34	9.91	8.08	5.79	9.73							15.76	1.52			

Note

1. Package body dimensions “D and “E do not include mold and metal protrusions. Allowable protrusion is 0.25 mm per side.
2. Lead width dimension “b does not include dambar protrusions. Allowable dambar protrusion is 0.25 mm in total per lead.

sot1223-2_po

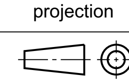
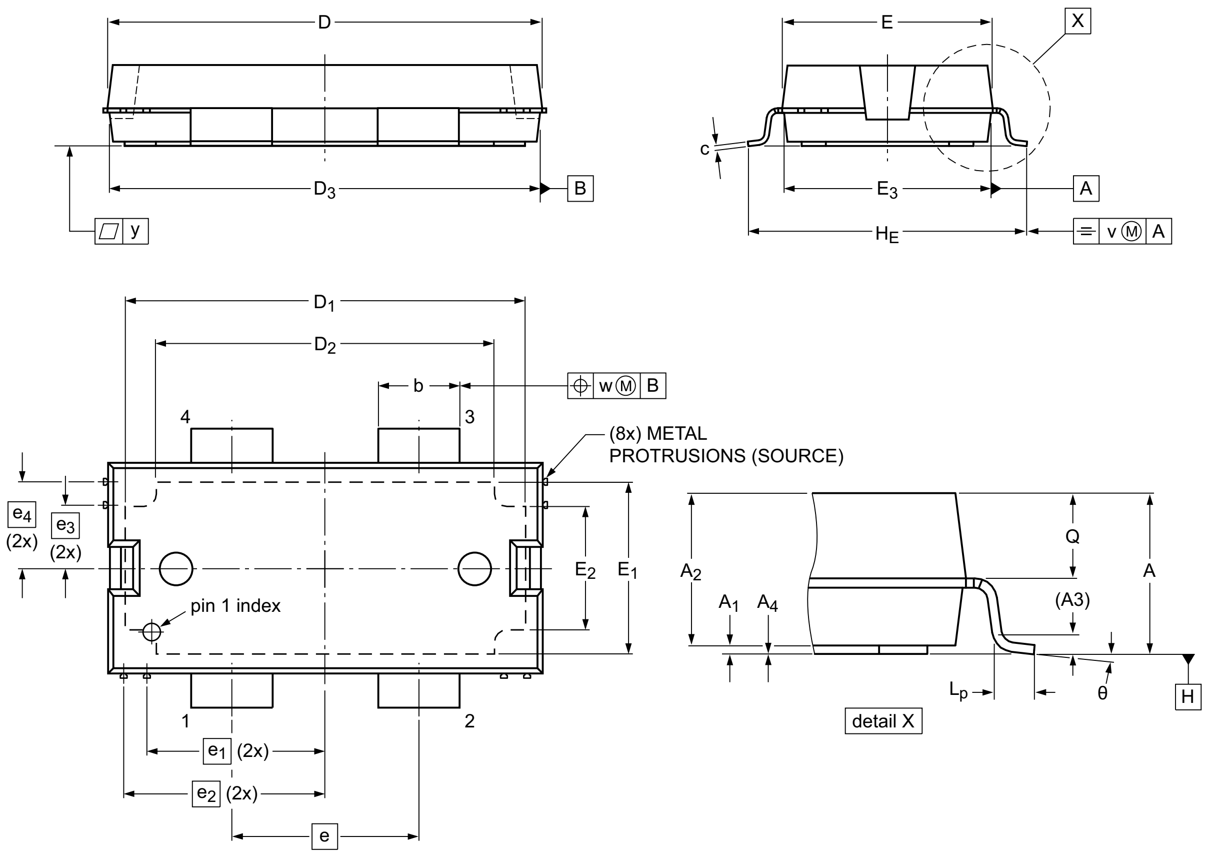
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1223-2						~~15-01-12~~ 15-06-04

Fig 11. Package outline SOT1223-2 (HSOP4F)

HSOP4: plastic, heatsink small outline package; 4 leads **SOT1224-2**



0 10 mm
scale

H_E	L_p	Q	v	w	y	θ
13.5	1.10	2.07			0.1	7°
13.2	0.95	2.02	0.25	0.25		3°
12.9	0.80	1.97				0°

Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	A_4	b	c	D(1)	D_1	D_2	D_3	E(1)	E_1	E_2	E_3	e	e_1	e_2	e_3	e_4
	max	3.9	0.2	3.65		0.06	3.90	0.27	20.62	19.00	16.05	20.44	10.01	8.18	5.89	9.83					
mm	nom		0.1	3.60	0.35	0	3.85	0.22	20.57	18.95	16.00	20.39	9.96	8.13	5.84	9.78	8.85	8.45	9.55	2.97	4.07
	min		0	3.55		-0.02	3.80	0.17	20.52	18.90	15.95	20.34	9.91	8.08	5.79	9.73					

Note

1. Package body dimensions “D and “E do not include mold and metal protrusions. Allowable protrusion is 0.25 mm per side.
2. Lead width dimension “b does not include dambar protrusions. Allowable dambar protrusion is 0.25 mm in total per lead.
3. Dimension A_4 is measured with respect to bottom of the heatsink DATUM H. Positive value means that the bottom of the heatsink is higher than the bottom of the lead.

sot1224-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1224-2						~~15-01-13~~ 15-06-04

Fig 12. Package outline SOT1224-2 (HSOP4)

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C1 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1C [2]

[1] CDM classification C1 is granted to any part that passes after exposure to an ESD pulse of 250 V, but fails after exposure to an ESD pulse of 500 V.

[2] HBM classification 1C is granted to any part that passes after exposure to an ESD pulse of 1000 V, but fails after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP10H6120P_BLP10H6120PG v.1	20161220	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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13. Contact information

For more information, please visit: **http://www.ampleon.com**

For sales office addresses, please visit: **http://www.ampleon.com/sales**

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