BLP7G07S-140P

Power LDMOS transistor

Rev. 5 — 8 January 2016

AMPLEON

Product data sheet

1. Product profile

1.1 General description

140 W LDMOS power transistor for base station applications at frequencies from 700 MHz to 1000 MHz.

Table 1. Typical performance

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	724 to 769	28	35	20.9	29.6	−36.3 [1]
	790 to 821	28	35	20.2	29.0	−35.5 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

1.2 Features and benefits

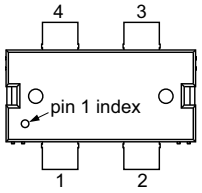
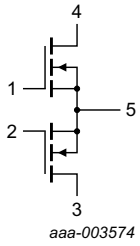
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (700 MHz to 1000 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 700 MHz to 1000 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	gate 1		
2	gate 2		
3	drain 2		
4	drain 1		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP7G07S-140P	HSOP4F	plastic, heatsink small outline package; 4 leads (flat)	SOT1223-2

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−0.5	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 35 W; V_{DS} = 28 V; I_{Dq} = 1200 mA	0.455	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 100 mA	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 600 mA	1.7	2.1	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	18	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 3.5 A	-	6.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 3.5 A	-	0.19	-	Ω

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1-64 DPCH; f_1 = 724 MHz; f_2 = 729 MHz; f_3 = 764 MHz; f_4 = 769 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1200 mA; T_{case} = 25 °C; unless otherwise specified; in a broadband class-AB production test circuit from 724 MHz to 821 MHz.

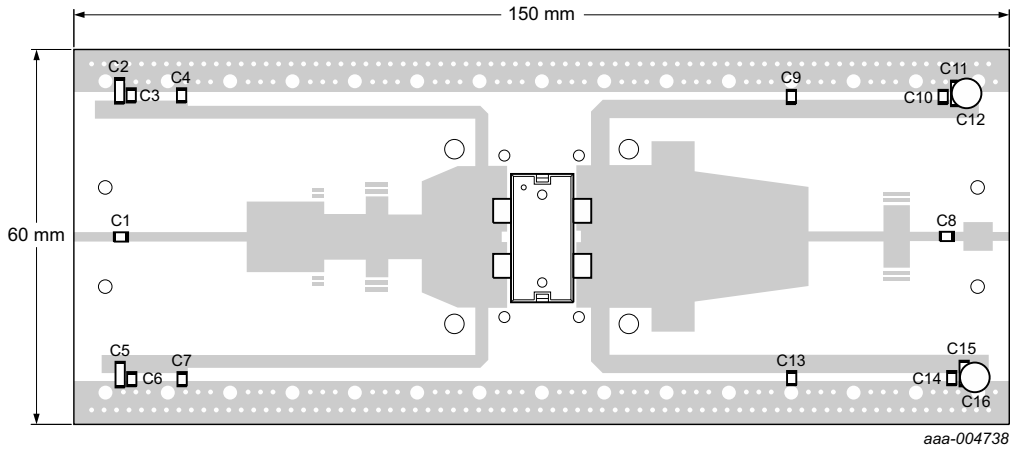
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 35 W	19.8	20.9	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 35 W	-	−14	−7.5	dB
η_D	drain efficiency	$P_{L(AV)}$ = 35 W	26.9	29.6	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 35 W	-	−36.3	−32.4	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLP7G07S-140P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 1200 mA; P_L = 140 W; f = 724 MHz to 821 MHz.

7.2 Test circuit information



See Table 8 for list of components.

Fig 1. Component layout

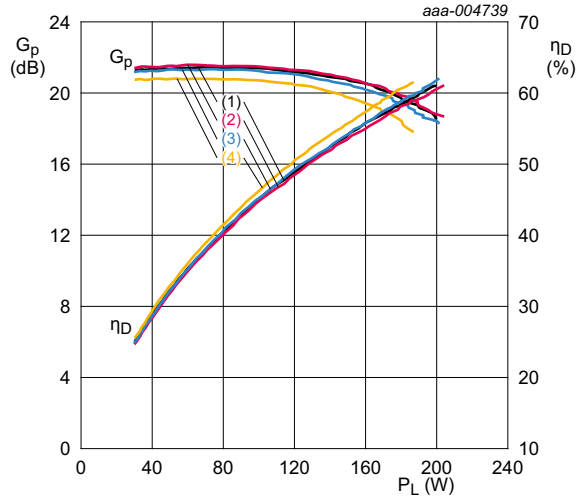
Table 8. List of components

See Figure 1 for component layout.

Component	Description	Value	Remarks
C1, C4, C7, C8, C9, C13	multilayer ceramic chip capacitor	82 pF	ATC800
C2, C5, C11, C15	multilayer ceramic chip capacitor	10 μF	TDK
C3, C6, C10, C14	multilayer ceramic chip capacitor	1 μF	Murata
C12, C16	electrolytic capacitor	470 μF, 63 V	

7.3 Graphical data

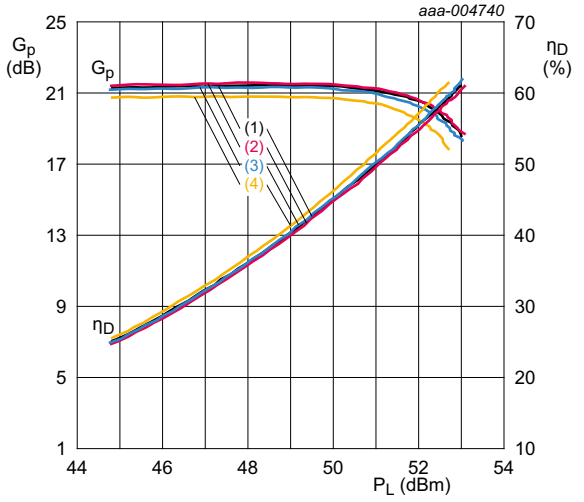
7.3.1 CW pulsed



V_{DS} = 28 V; I_{Dq} = 1200 mA; t_p = 10 μs; δ = 10 %.

(1) f = 724 MHz
(2) f = 769 MHz
(3) f = 790 MHz
(4) f = 821 MHz

Fig 2. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 1200 mA; t_p = 10 μs; δ = 10 %.

(1) f = 724 MHz
(2) f = 769 MHz
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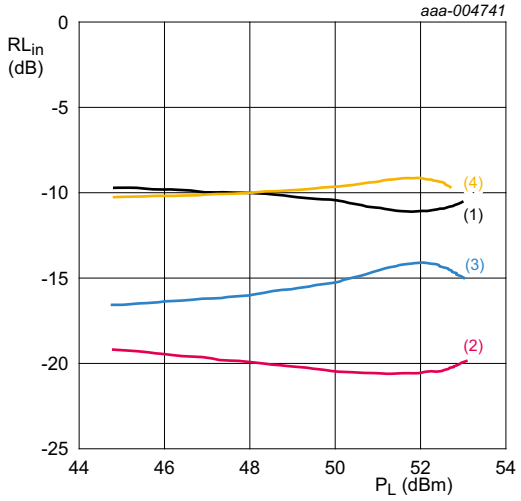
Fig 3. Power gain and drain efficiency as function of load power; typical values

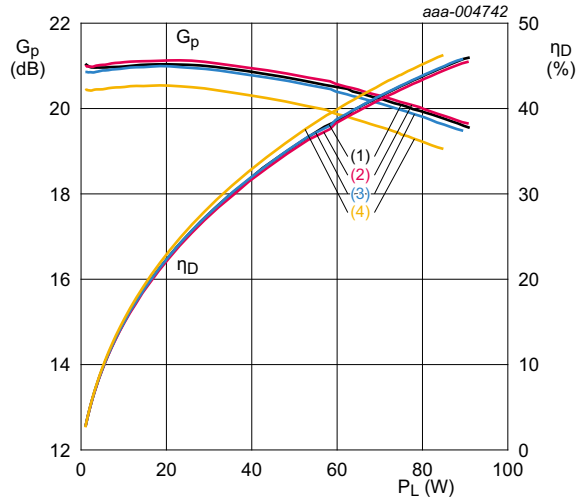


V_{DS} = 28 V; I_{Dq} = 1200 mA; t_p = 10 μs; δ = 10 %.

(1) f = 724 MHz
(2) f = 769 MHz
(3) f = 790 MHz
(4) f = 821 MHz

Fig 4. Input return loss as a function of load power; typical values

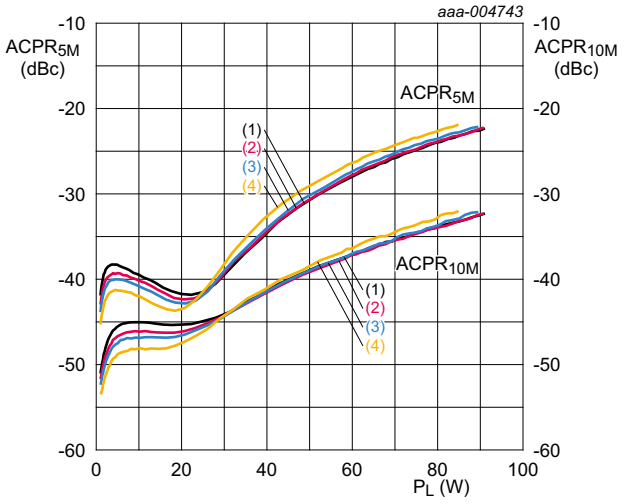
7.3.2 2-Carrier W-CDMA



V_{DS} = 28 V; I_{Dq} = 1200 mA.

(1) f = 726.5 MHz
(2) f = 766.5 MHz
(3) f = 793.5 MHz
(4) f = 818.5 MHz

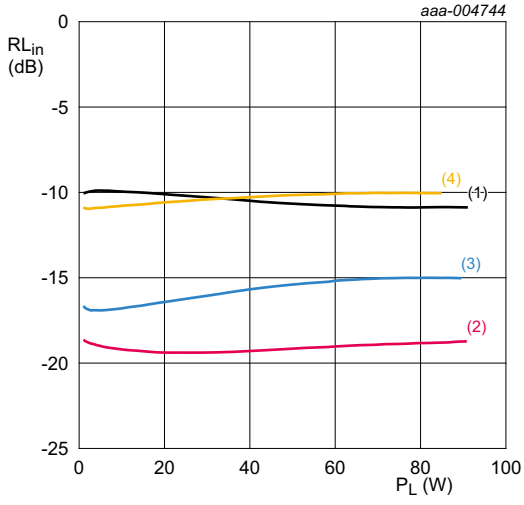
Fig 5. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 1200 mA.

(1) f = 726.5 MHz
(2) f = 766.5 MHz
(3) f = 793.5 MHz
(4) f = 818.5 MHz

Fig 6. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as function of load power; typical values



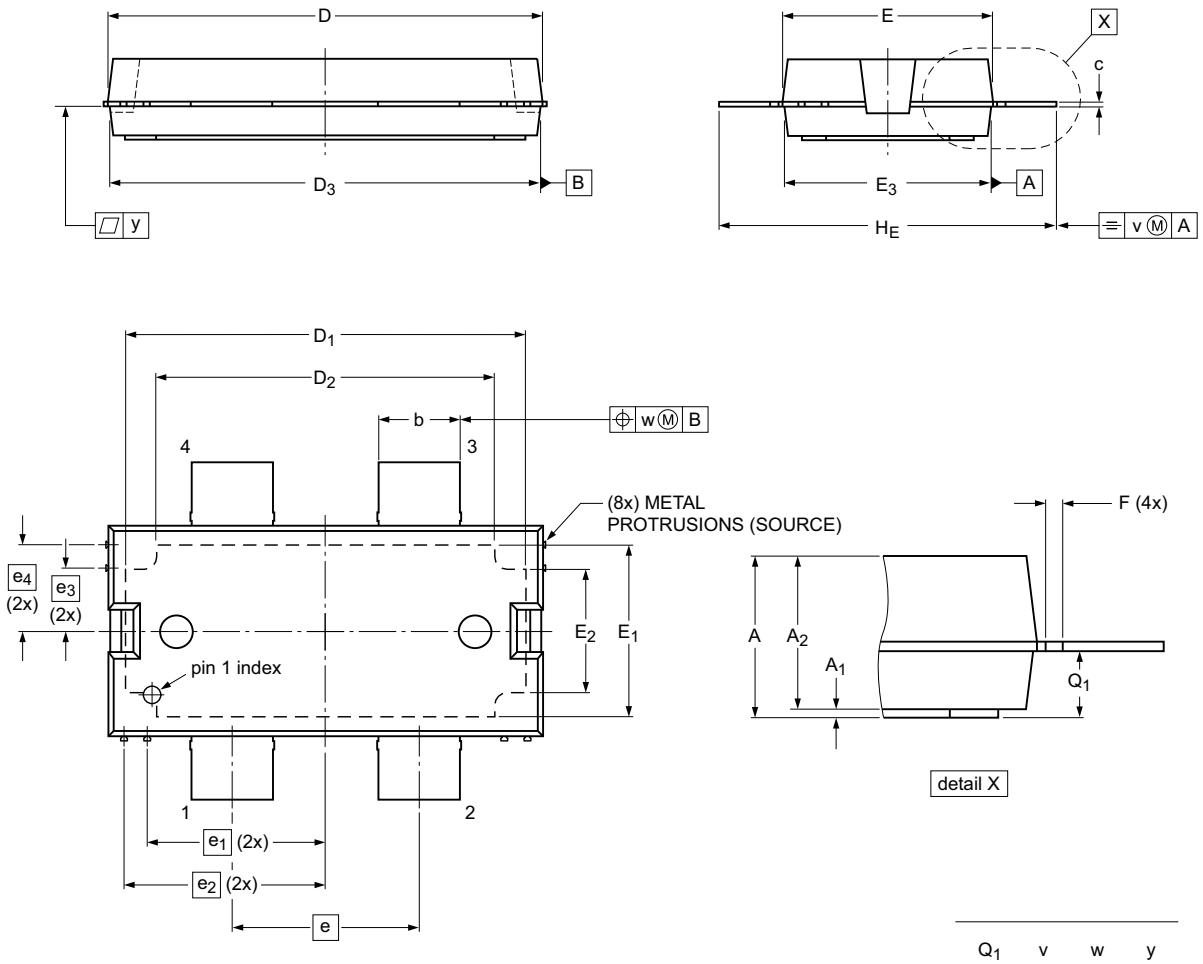
V_{DS} = 28 V; I_{Dq} = 1200 mA.

(1) f = 726.5 MHz
(2) f = 766.5 MHz
(3) f = 793.5 MHz
(4) f = 818.5 MHz

Fig 7. Input return loss as a function of load power; typical values

8. Package outline

HSOP4F: plastic, heatsink small outline package; 4 leads(flat) **SOT1223-2**



Q_1	v	w	y
1.62			0.1
1.57	0.25	0.25	
1.52			

Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	c	$D^{(1)}$	D_1	D_2	D_3	$E^{(1)}$	E_1	E_2	E_3	e	e_1	e_2	e_3	e_4	F	H_E
	max	3.9	0.2	3.65	3.90	0.27	20.62	19.00	16.05	20.44	10.01	8.18	5.89	9.83							16.16
mm	nom		0.1	3.60	3.85	0.22	20.57	18.95	16.00	20.39	9.96	8.13	5.84	9.78	8.85	8.45	9.55	2.97	4.07	0.4	15.96
	min		0	3.55	3.80	0.17	20.52	18.90	15.95	20.34	9.91	8.08	5.79	9.73							15.76

Note
1. Package body dimensions “D and “E do not include mold and metal protrusions. Allowable protrusion is 0.25 mm per side.
2. Lead width dimension “b does not include dambar protrusions. Allowable dambar protrusion is 0.25 mm in total per lead.

sot1223-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1223-2						~~15-01-12~~ 15-06-04

Fig 8. Package outline SOT1223-2 (HSOP4F)

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average Ratio
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP7G07S-140P v.5	20160108	Product data sheet	-	BLP7G07S-140P v.4
Modifications:	• Table 3 on page 2: table updated • Figure 8 on page 7: package outline changed from SOT1223-1 to SOT1223-2			
BLP7G07S-140P v.4	20150901	Product data sheet	-	BLP7G07S-140P v.3
BLP7G07S-140P v.3	20130329	Product data sheet	-	BLP7G07S-140P v.2
BLP7G07S-140P v.2	20121009	Objective data sheet	-	BLP7G07S-140P v.1
BLP7G07S-140P v.1	20120621	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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