BLP7G22-10

LDMOS driver transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

10W plastic LDMOS power transistor for base station applications at frequencies from 700 MHz to 2700 MHz.

Table 1. Application performance (multiple frequencies)

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 110 mA; in a class-AB application circuit.

Test signal	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	$ACPR_{5M}$ (dBc)
Pulsed CW	2700	110	28	2	14.5	26	-
1-carrier W-CDMA	748	110	28	0.7	27.5	13.5	–43 [1]
	748	110	28	2	27.5	25	–40
2-carrier W-CDMA	2140	110	28	0.7	17.4	13	–51
	2140	110	28	2	17.4	25	–40

[1] Test signal: 2-carrier W-CDMA; carrier spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on CCDF; RF performance at V_{DS} = 28 V; I_{Dq} = 110 mA.

1.2 Features and benefits

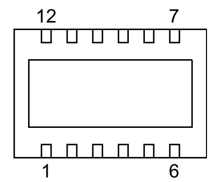
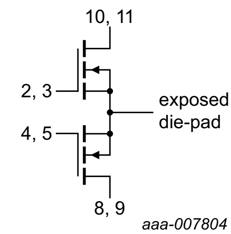
- High efficiency
- Excellent ruggedness
- Designed for broadband operation
- Excellent thermal stability
- High power gain
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- CDMA
- W-CDMA
- GSM EDGE
- MC-GSM
- LTE
- WiMAX

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol [1]
1, 6, 7, 12	n.c.	 Transparent top view	
2, 3, 4, 5	gate		
8, 9, 10, 11	drain		
exposed die-pad	source		

[1] To be used in single ended applications only.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP7G22-10	HVSON12	plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 6 × 4 × 0.85 mm	SOT1179-2

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	150	°C

5. Recommended operating conditions

See application note *AN11198* for more details.

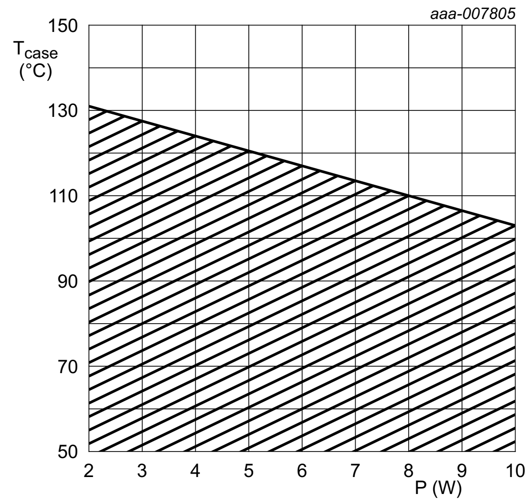


Fig 1. Recommended operating area; case temperature as a function of power dissipation

6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 70 °C; P_L = 2 W	3.2	K/W

7. Characteristics

Table 6. DC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.18 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 18 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	−1.4	-	+1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	3.2	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 18 mA	-	160	-	mS
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V; I_D = 630 mA	-	1000	-	mΩ

Table 7. RF characteristics

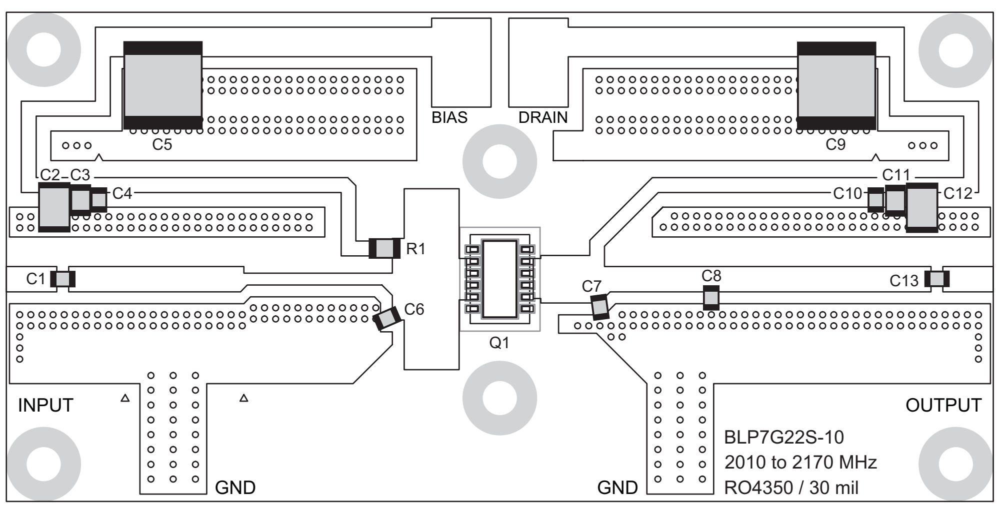
Test signal: 1-tone pulsed; t_p = 50 μs; δ = 10 %; f = 2140 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 110 mA; T_{case} = 25 °C; unless otherwise specified, in a production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 2 W	15	16	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 2 W	20	23	-	%
$P_{L(1dB)}$	output power at 1 dB gain compression		11	-	-	W
RL_{in}	input return loss	$P_{L(AV)}$ = 2 W	-	−16	−12	dB

8. Application information

8.1 Frequency band 2110 MHz to 2170 MHz

8.1.1 Application circuit



The used Printed-Circuit Board (PCB) material is Rogers RO4350; thickness = 0.762 mm; ε_r = 3.5; thickness copper plating is 35 μm.

See Table 8 for list of components.

Fig 2. Component layout

Table 8. List of components

See Figure 2 for component layout.

The used Printed-Circuit Board (PCB) material is Rogers RO4350; thickness = 0.762 mm; ε_r = 3.5; thickness copper plating is 35 μm.

Component	Description	Value	Remarks
C1, C4, C10, C13	multilayer ceramic chip capacitor	22 pF	[1]
C2, C12	multilayer ceramic chip capacitor	1 μF	[2]
C3, C11	multilayer ceramic chip capacitor	100 nF	[3]
C5, C9	multilayer ceramic chip capacitor	10 μF; 50 V	[4]
C6	multilayer ceramic chip capacitor	2.8 pF	[1]

Table 8. List of components *...continued*

See Figure 2 for component layout.
The used Printed-Circuit Board (PCB) material is Rogers RO4350; thickness = 0.762 mm; ε_r = 3.5; thickness copper plating is 35 μm.

Component	Description	Value	Remarks
C7	multilayer ceramic chip capacitor	3.9 pF	[1]
C8	multilayer ceramic chip capacitor	1.7 pF	[1]
R1	chip resistor	10 Ω	SMD 0805; 1 % tolerance

[1] American Technical Ceramics type 100A or capacitor of same quality.

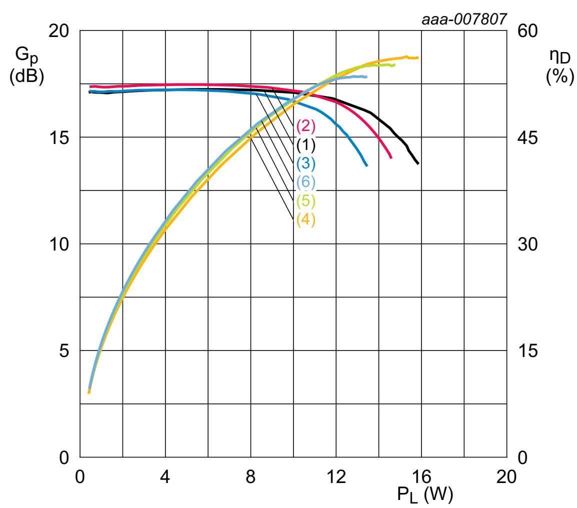
[2] Murata GRM31MR71H105KA88L or capacitor of same quality.

[3] Murata GRM21BR71H104KA01L or capacitor of same quality.

[4] Murata GRM32ER71H106KA88L or capacitor of same quality.

8.1.2 Graphs

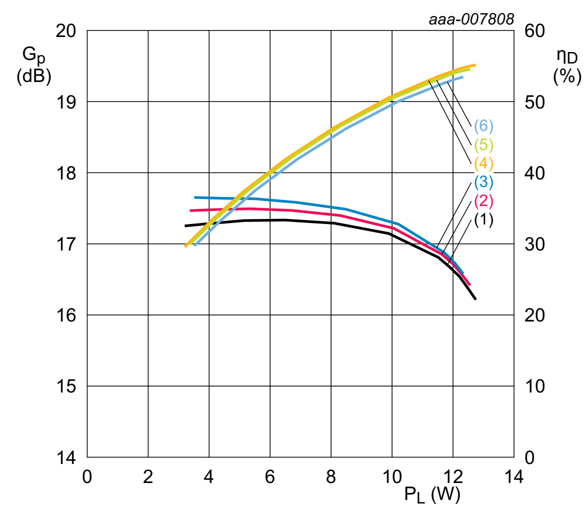
8.1.2.1 Pulsed CW



V_{DS} = 28 V; I_{Dq} = 110 mA; T_{case} = 25 °C; δ = 10 %; t_p = 20 μs.

(1) G_p at f = 2110 MHz
(2) G_p at f = 2140 MHz
(3) G_p at f = 2170 MHz
(4) η_D at f = 2110 MHz
(5) η_D at f = 2140 MHz
(6) η_D at f = 2170 MHz

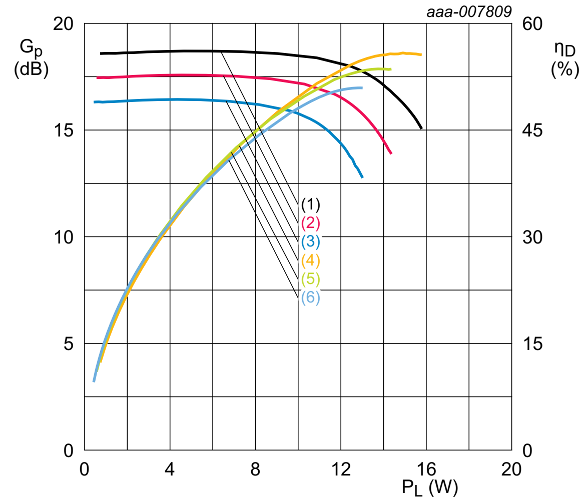
Fig 3. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; f = 2140 MHz; T_{case} = 25 °C; δ = 10 %; t_p = 20 μs.

(1) G_p at I_{Dq} = 90 mA
(2) G_p at I_{Dq} = 110 mA
(3) G_p at I_{Dq} = 130 mA
(4) η_D at I_{Dq} = 90 mA
(5) η_D at I_{Dq} = 110 mA
(6) η_D at I_{Dq} = 130 mA

Fig 4. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 110 mA; f = 2140 MHz; δ = 10 %; t_p = 20 μs.

(1) G_p at T_{case} = –37 °C

(2) G_p at T_{case} = 25 °C

(3) G_p at T_{case} = 85 °C

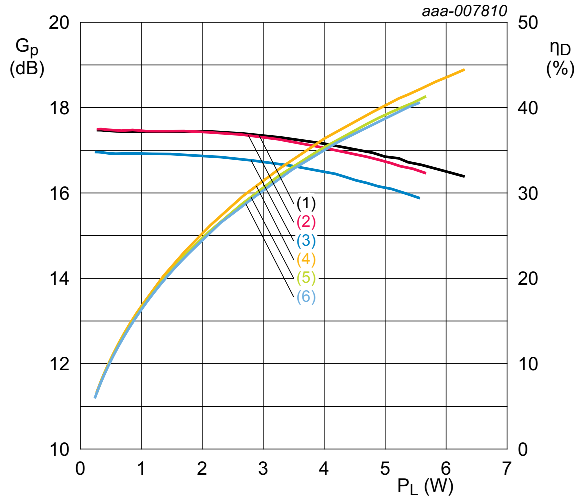
(4) η_D at T_{case} = –37 °C

(5) η_D at T_{case} = 25 °C

(6) η_D at T_{case} = 85 °C

Fig 5. Power gain and drain efficiency as function of load power; typical values

8.1.2.2 2-Carrier W-CDMA



V_{DS} = 28 V; I_{Dq} = 110 mA; T_{case} = 25 °C; carrier spacing = 5 MHz; 46 % clipping; PAR = 8.4 dB at 0.01 % probability on CCDF.

(1) G_p at f = 2110 MHz

(2) G_p at f = 2140 MHz

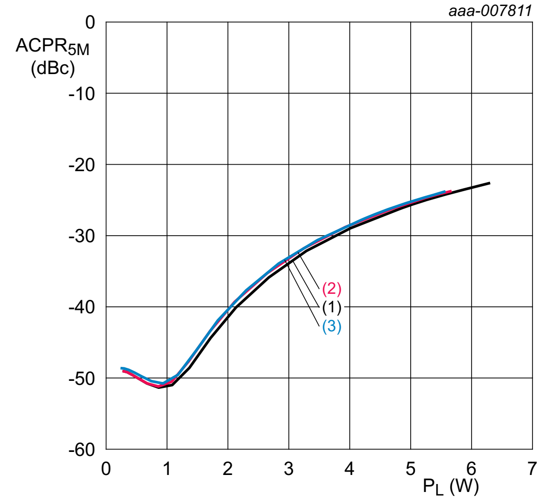
(3) G_p at f = 2170 MHz

(4) η_D at f = 2110 MHz

(5) η_D at f = 2140 MHz

(6) η_D at f = 2170 MHz

Fig 6. Power gain and drain efficiency as function of load power; typical values



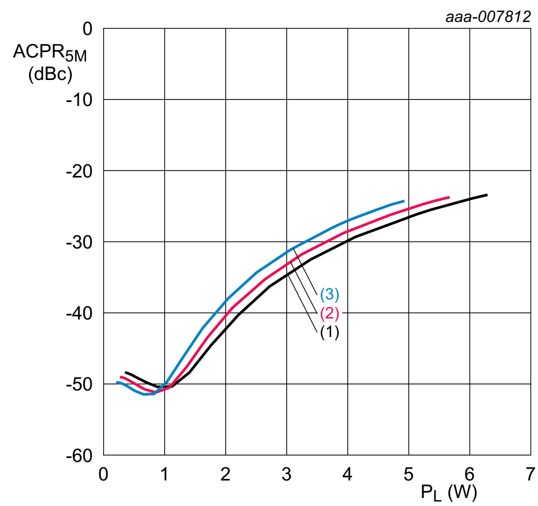
V_{DS} = 28 V; I_{Dq} = 110 mA; T_{case} = 25 °C; carrier spacing = 5 MHz; 46 % clipping; PAR = 8.4 dB at 0.01 % probability on CCDF.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 7. Adjacent channel power ratio (5 MHz) as a function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 110 mA; f = 2140 MHz; carrier spacing = 5 MHz; 46 % clipping; PAR = 8.4 dB at 0.01 % probability on CCDF.

(1) T_{case} = −37 °C

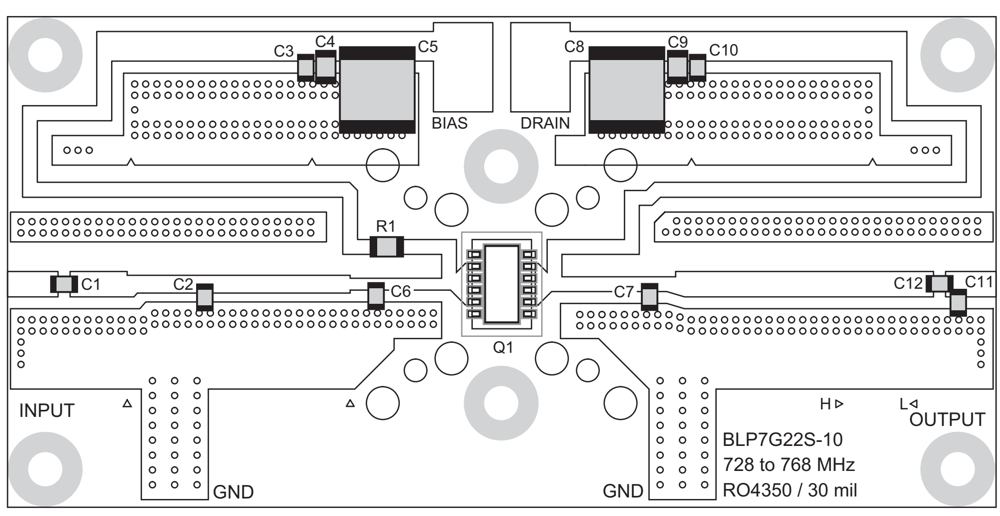
(2) T_{case} = 25 °C

(3) T_{case} = 85 °C

Fig 8. Adjacent channel power ratio (5 MHz) as a function of load power; typical values

8.2 Frequency band 728 MHz to 768 MHz

8.2.1 Application circuit



The used Printed-Circuit Board (PCB) material is Rogers RO4350; thickness = 0.762 mm; ε_r = 3.5; thickness copper plating is 35 μm.

See Table 9 for list of components.

Fig 9. Component layout

Table 9. List of components

See Figure 9 for component layout.

The used Printed-Circuit Board (PCB) material is Rogers RO4350; thickness = 0.762 mm; ε_r = 3.5; thickness copper plating is 35 μm.

Component	Description	Value		Remarks
C1, C12	multilayer ceramic chip capacitor	68 pF	[1]	
C2	multilayer ceramic chip capacitor	10 pF	[1]	
C3, C10	multilayer ceramic chip capacitor	100 pF	[1]	
C4, C9	multilayer ceramic chip capacitor	100 nF	[2]	
C5, C8	multilayer ceramic chip capacitor	10 μF; 50 V	[3]	
C6	multilayer ceramic chip capacitor	36 pF	[1]	
C7	multilayer ceramic chip capacitor	9.1 pF	[1]	
C11	multilayer ceramic chip capacitor	7.5 pF	[1]	
R1	chip resistor	5.1 Ω		SMD 0805; 1 % tolerance

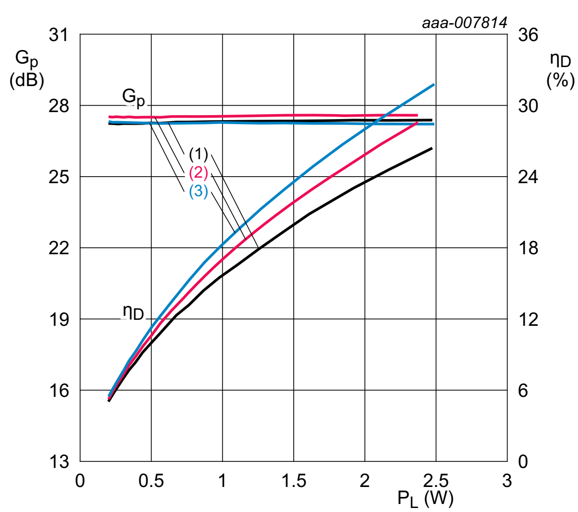
[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] Murata GRM21BR71H104KA01L or capacitor of same quality.

[3] Murata GRM32ER71H106KA88L or capacitor of same quality.

8.2.2 Graphs

8.2.2.1 2-Carrier W-CDMA



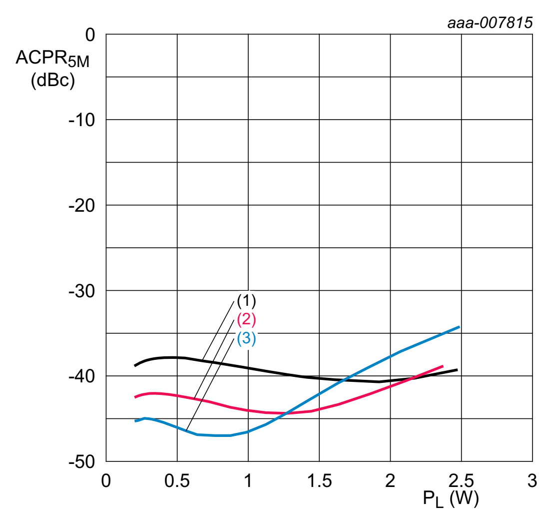
V_{DS} = 28 V; I_{Dq} = 110 mA; T_{case} = 25 °C; carrier spacing = 5 MHz; 46 % clipping; PAR = 8.4 dB at 0.01 % probability on CCDF.

(1) f = 728 MHz

(2) f = 748 MHz

(3) f = 768 MHz

Fig 10. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 110 mA; T_{case} = 25 °C; carrier spacing = 5 MHz; 46 % clipping; PAR = 8.4 dB at 0.01 % probability on CCDF.

(1) f = 728 MHz

(2) f = 748 MHz

(3) f = 768 MHz

Fig 11. Adjacent channel power ratio (5 MHz) as a function of load power; typical values

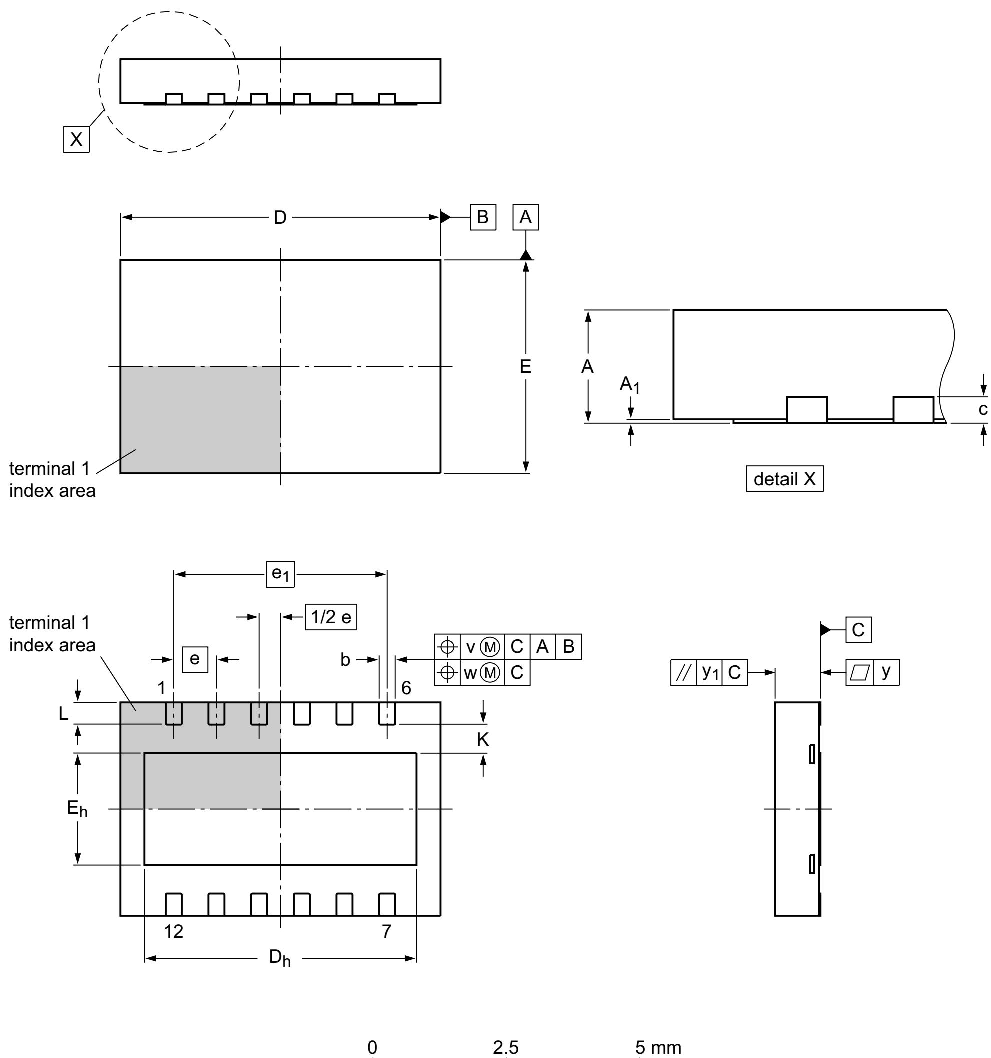
9. Test information

9.1 Ruggedness in class-AB operation

The BLP7G22-10 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 110 mA; P_L = 10 W; frequency from 700 MHz to 2700 MHz.

10. Package outline

HVSON12: plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 4 x 6 x 0.85 mm **SOT1179-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	K	L	v	w	y	y_1
	max	1.00	0.05	0.35		6.1	5.2	4.1	2.2				0.5				
mm	nom	0.85	0.03	0.30	0.2	6.0	5.1	4.0	2.1	0.8	4		0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.25		5.9	5.0	3.9	2.0			0.5	0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1179-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1179-2	- - -	MO-229	- - -			~~13-02-26~~ 13-07-16

Fig 12. Package outline SOT1179-2 (HVSON12)

11. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
EDGE	Enhanced Data rates for GSM Evolution
ESD	ElectroStatic Discharge
GSM	Global System for Mobile Communication
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LTE	Long Term Evolution
MC-GSM	Multi Carrier GSM
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP7G22-10#3	20150901	Product data sheet		BLP7G22-10 v.2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLP7G22-10 v.2	20130530	Product data sheet	-	BLP7G22-10 v.1
BLP7G22-10 v.1	20120213	Objective data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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15. Contact information

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For sales office addresses, please visit: http://www.ampleon.com/sales

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