BLS6G3135-120; BLS6G3135S-120

LDMOS S-Band radar power transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

120 W LDMOS power transistor intended for radar applications in the 3.1 GHz to 3.5 GHz range.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 300 μs; δ = 10 %; I_{Dq} = 100 mA; in a class-AB production test circuit.

Mode of operation	f (GHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
pulsed RF	3.1 to 3.5	32	120	11	43	20	6

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

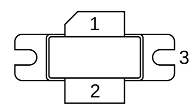
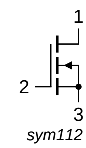
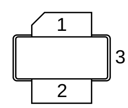
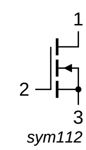
- Typical pulsed RF performance at a frequency of 3.1 GHz to 3.5 GHz, a supply voltage of 32 V, an I_{Dq} of 100 mA, a t_p of up to 300 μs with δ of 10 %:
  - Output power = 120 W
  - Gain = 11 dB
  - Efficiency = 43 %
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (3.1 GHz to 3.5 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- S-Band power amplifiers for radar applications in the 3.1 GHz to 3.5 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
BLS6G3135-120 (SOT502A)			
1	drain		
2	gate		
3	source [1]		
BLS6G3135S-120 (SOT502B)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS6G3135-120	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLS6G3135S-120	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	60	V
V_{GS}	gate-source voltage	−0.5	+13	V
I_D	drain current	-	7.2	A
T_{stg}	storage temperature	−65	+150	°C
T_j	junction temperature	-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$Z_{th(j-mb)}$	transient thermal impedance from junction to mounting base	T_{case} = 85 °C; P_L = 120 W			
		t_p = 300 μs; δ = 10 %	0.29	0.40	K/W
		t_p = 100 μs; δ = 20 %	0.30	0.41	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.5 mA	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 180 mA	1.4	1.8	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	5	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	27	33	-	A
I_{GSS}	gate leakage current	V_{GS} = 8.3 V; V_{DS} = 0 V	-	-	450	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 9 A	-	13	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 6.3 A	-	0.085	0.160	Ω

7. Application information

Table 7. Application information

Mode of operation: pulsed RF; t_p = 300 μs; δ = 10 %; RF performance at V_{DS} = 32 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		-	120	-	W
V_{CC}	supply voltage	P_L = 120 W	-	-	32	V
G_p	power gain	P_L = 120 W	9.5	11	-	dB
IRL	input return loss	P_L = 120 W	6	10	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression	P_L = 120 W	-	130	-	W
η_D	drain efficiency	P_L = 120 W	39	43	-	%
t_r	rise time	P_L = 120 W	-	20	50	ns
t_f	fall time	P_L = 120 W	-	6	50	ns

Table 8. Typical impedance

f GHz	Z_S Ω	Z_L Ω
3.1	2.7 – j5.4	5.9 – j5.9
3.2	3.3 – j4.7	4.5 – j6.2
3.3	4.2 – j4.4	3.5 – j6.0
3.4	5.2 – j4.8	2.7 – j5.6
3.5	5.7 – j6.2	2.0 – j5.2

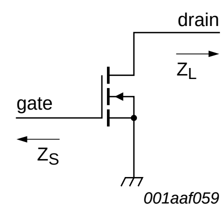
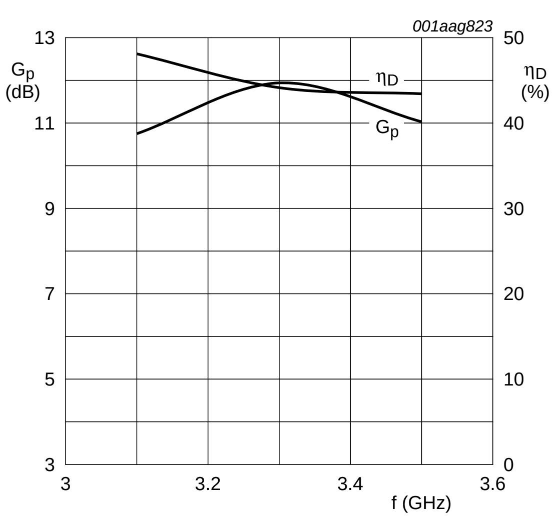


Fig 1. Definition of transistor impedance

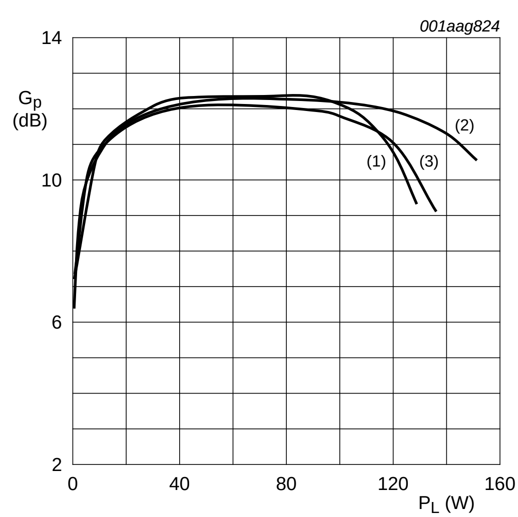
7.1 Ruggedness in class-AB operation

The BLS6G3135-120 and BLS6G3135S-120 are capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 100 mA; P_L = 120 W; t_p = 300 μs; δ = 10 %.



V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 300 μs; δ = 10 %; P_L = 120 W.

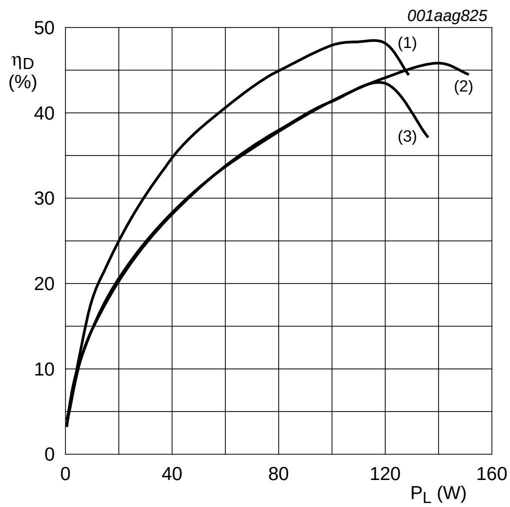
Fig 2. Power gain and drain efficiency as functions of frequency; typical values



(1) f = 3.1 GHz
(2) f = 3.3 GHz
(3) f = 3.5 GHz

V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 300 μs; δ = 10 %.

Fig 3. Power gain as a function of load power; typical values



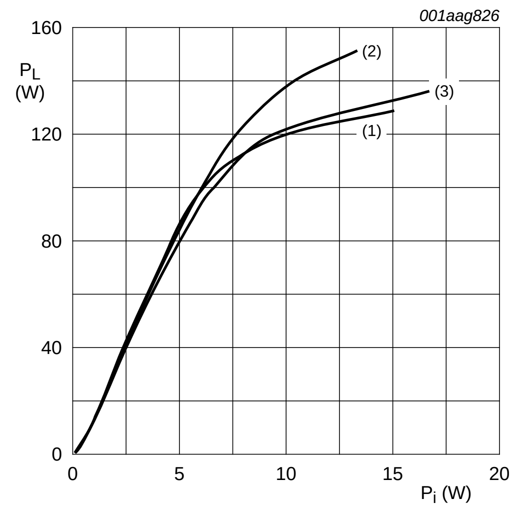
(1) f = 3.1 GHz

(2) f = 3.3 GHz

(3) f = 3.5 GHz

V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 300 μs; δ = 10 %.

Fig 4. Drain efficiency as a function of load power; typical values



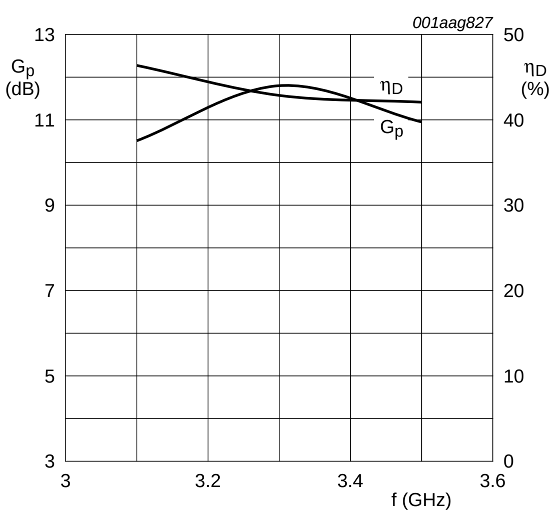
(1) f = 3.1 GHz

(2) f = 3.3 GHz

(3) f = 3.5 GHz

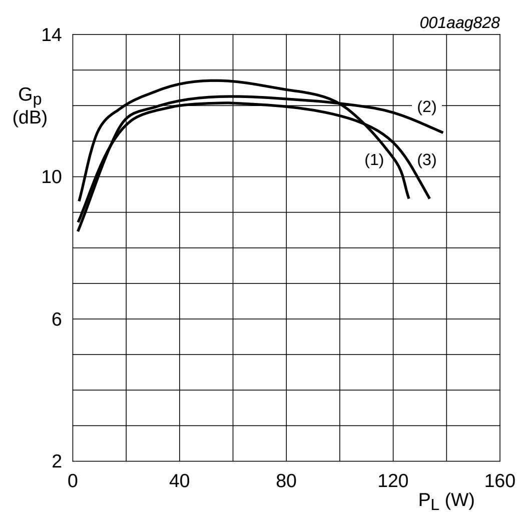
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 300 μs; δ = 10 %.

Fig 5. Load power as a function of input power; typical values



V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 100 μs; δ = 20 %;
P_L = 120 W.

Fig 6. Power gain and drain efficiency as functions of frequency; typical values



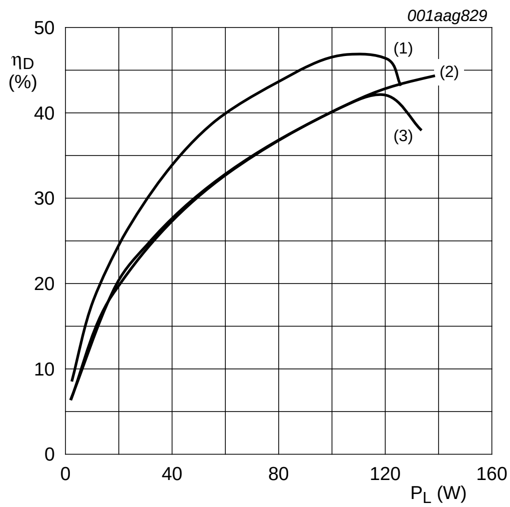
(1) f = 3.1 GHz

(2) f = 3.3 GHz

(3) f = 3.5 GHz

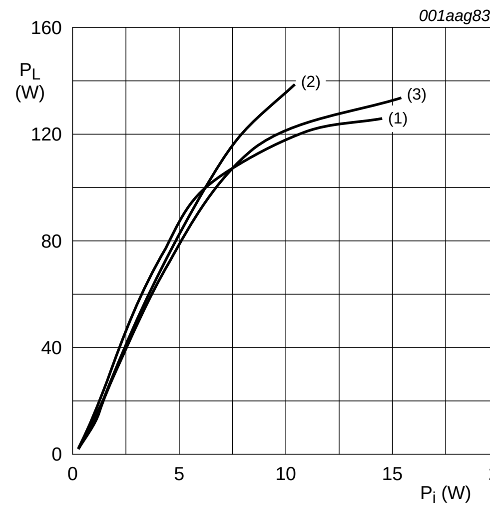
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 100 μs; δ = 20 %.

Fig 7. Power gain as a function of load power; typical values



(1) f = 3.1 GHz
(2) f = 3.3 GHz
(3) f = 3.5 GHz
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 100 μs; δ = 20 %.

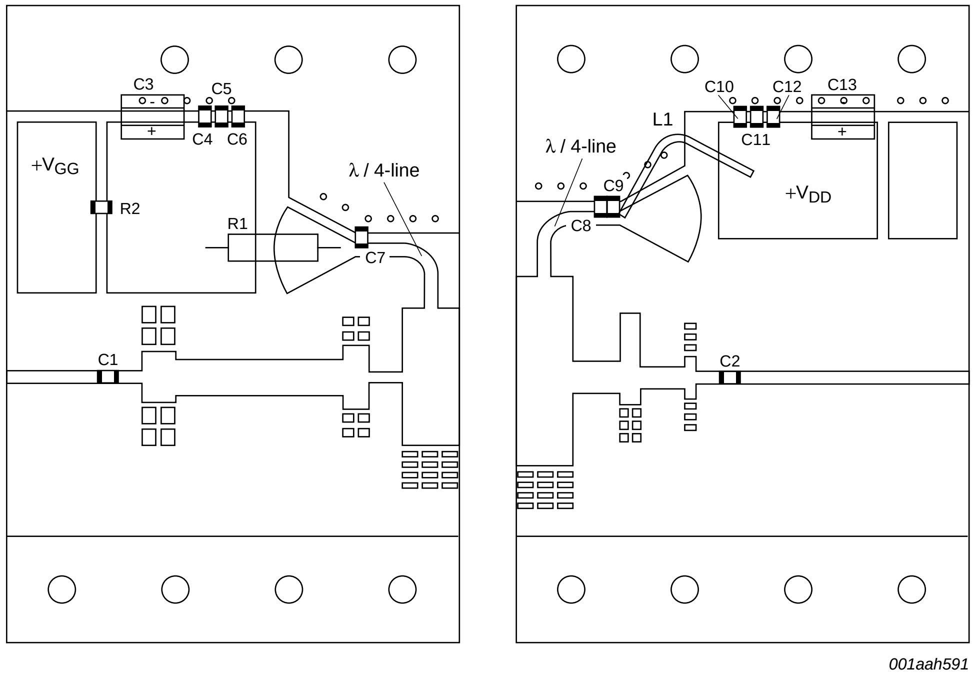
Fig 8. Drain efficiency as a function of load power; typical values



(1) f = 3.1 GHz
(2) f = 3.3 GHz
(3) f = 3.5 GHz
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 100 μs; δ = 20 %.

Fig 9. Load power as a function of input power; typical values

8. Test information



Striplines are on a double copper-clad Rogers Duroid 6006 Printed-Circuit Board (PCB) with ε_r = 6.2 and thickness = 0.64 mm.

See Table 9 for list of components.

Fig 10. Component layout for 3.1 GHz to 3.5 GHz MHz test circuit

Table 9. List of components (see Figure 10)

To ensure good power supply of the device, adding an electrolytical capacitor close to the supply connection of the circuit may be required. The actual capacitor value may differ depending on the pulse format, the quality of the power supply and the length of the connecting wires to the power supply. In general a value of 470 μF will be sufficient.

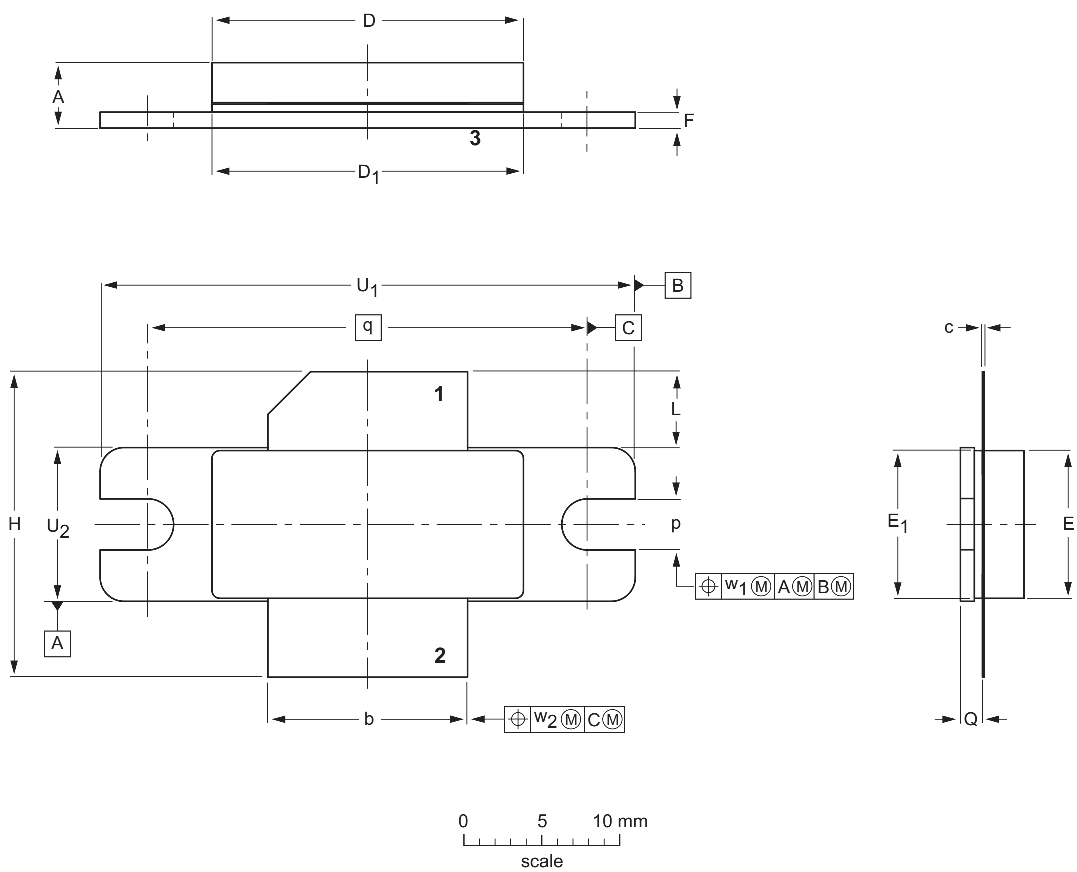
Component	Description	Value	Remarks
C1, C2, C4, C5, C6, C7, C8, C9, C11	multilayer ceramic chip capacitor	24 pF	[1]
C3	electrolytic capacitor	20 μF; 20 V	
C10	multilayer ceramic chip capacitor	33 pF	[1]
C12	multilayer ceramic chip capacitor	1 nF	[2]
C13	electrolytic capacitor	100 μF; 63 V	
L1	copper wire	-	
R1	resistor	49.9 Ω	
R2	SMD resistor	49.9 Ω	

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 700A or capacitor of same quality.

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



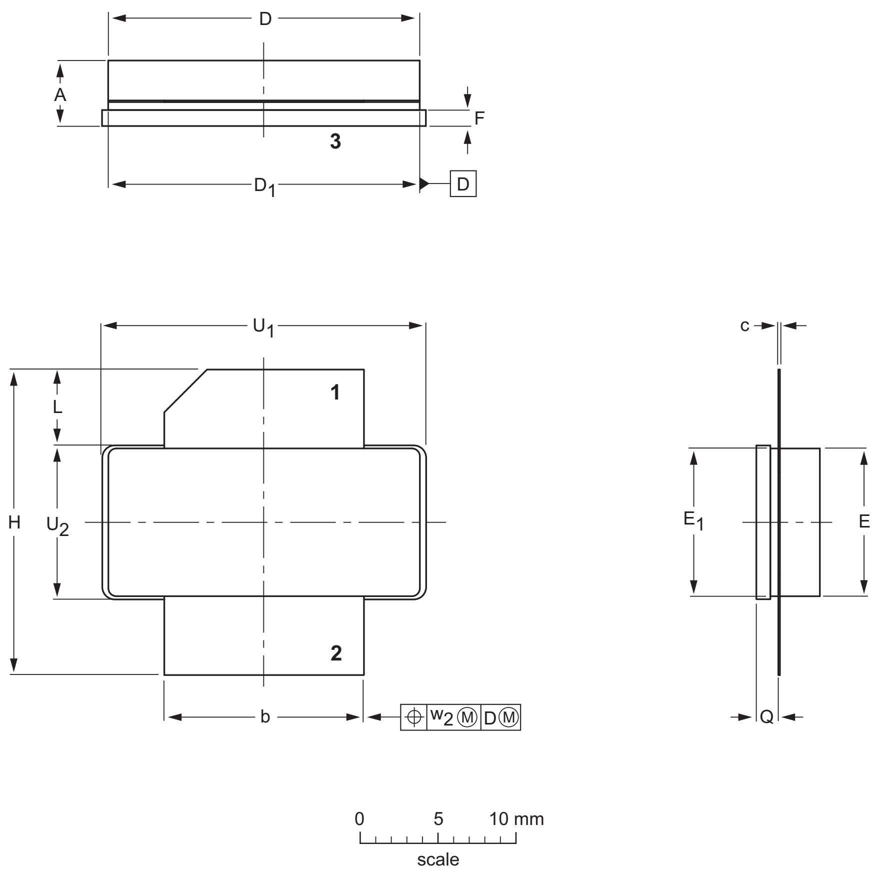
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

Fig 11. Package outline SOT502A

Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

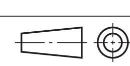
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 12. Package outline SOT502B

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Lateral Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
S-Band	Short wave Band
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS6G3135-120_6G3135S-120#3	20150901	Product data sheet		BLS6G3135-120_6G3135S-120#2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLS6G3135-120_6G3135S-120#2	20080529	Product data sheet	-	BLS6G3135-120_6G3135S-120#1
BLS6G3135-120_6G3135S-120#1	20070814	Preliminary data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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