

# BLS7G2729L-350P; BLS7G2729LS-350P

LDMOS S-band radar power transistor

Rev. 5 — 16 May 2014

Product data sheet

## 1. Product profile

### 1.1 General description

350 W LDMOS power transistor for S-band radar applications in the frequency range from 2.7 GHz to 2.9 GHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ;  $I_{Dq} = 200\text{ mA}$ ; in a class-AB production test circuit.

Test signal	f	V <sub>DS</sub>	P <sub>L</sub>	G <sub>p</sub>	$\eta_D$	t <sub>r</sub>	t <sub>f</sub>
	(GHz)	(V)	(W)	(dB)	(%)	(ns)	(ns)
pulsed RF	2.7 to 2.9	32	350	13	50	8	5

### 1.2 Features and benefits

- High efficiency
- Excellent ruggedness
- Designed for S-band operation (2.7 GHz to 2.9 GHz)
- Excellent thermal stability
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- S-band radar applications in the frequent range 2.7 GHz to 2.9 GHz



## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLS7G2729L-350P (SOT539A)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source <a href="#">[1]</a>		
<b>BLS7G2729LS-350P (SOT539B)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS7G2729L-350P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLS7G2729LS-350P	-	earless flanged balanced ceramic package; 4 leads	SOT539B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
$V_{DS}$	drain-source voltage	-	65	V
$V_{GS}$	gate-source voltage	-0.5	+11	V
$T_{stg}$	storage temperature	-65	+150	°C
$T_j$	junction temperature <a href="#">[1]</a>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the on-line MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-mb)}$	transient thermal impedance from junction to mounting base	$T_{case} = 85\text{ °C}; P_L = 350\text{ W}$		
		$t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.07	K/W
		$t_p = 200\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.09	K/W
		$t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.10	K/W
		$t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.09	K/W

## 6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.2\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 220\text{ mA}$	1.5	1.9	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	39	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$G_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 11.0\text{ A}$	-	16.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 7.7\text{ A}$	-	0.065	-	$\Omega$

Table 7. RF characteristics

Test signal: pulsed RF;  $t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ ; RF performance at  $V_{DS} = 32\text{ V}; I_{Dq} = 200\text{ mA}; T_{case} = 25\text{ °C}$ ; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 350\text{ W}$	11	13	-	dB
$RL_{in}$	input return loss	$P_L = 350\text{ W}$	-	-10	-	dB
$\eta_D$	drain efficiency	$P_L = 350\text{ W}$	46	50	-	%
$P_{droop(pulse)}$	pulse droop power	$P_L = 350\text{ W}$	-	0	0.5	dB
$t_r$	rise time	$P_L = 350\text{ W}$	-	8	50	ns
$t_f$	fall time	$P_L = 350\text{ W}$	-	5	50	ns

**7. Test information**

**7.1 Ruggedness in class-AB operation**

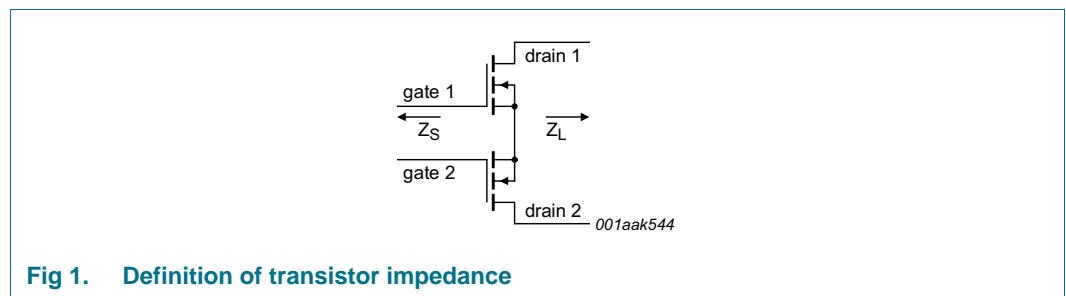
The BLS7G2729L-350P and BLS7G2729LS-350P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 200\text{ mA}$ ;  $P_L = 350\text{ W}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ .

**7.2 Impedance information**

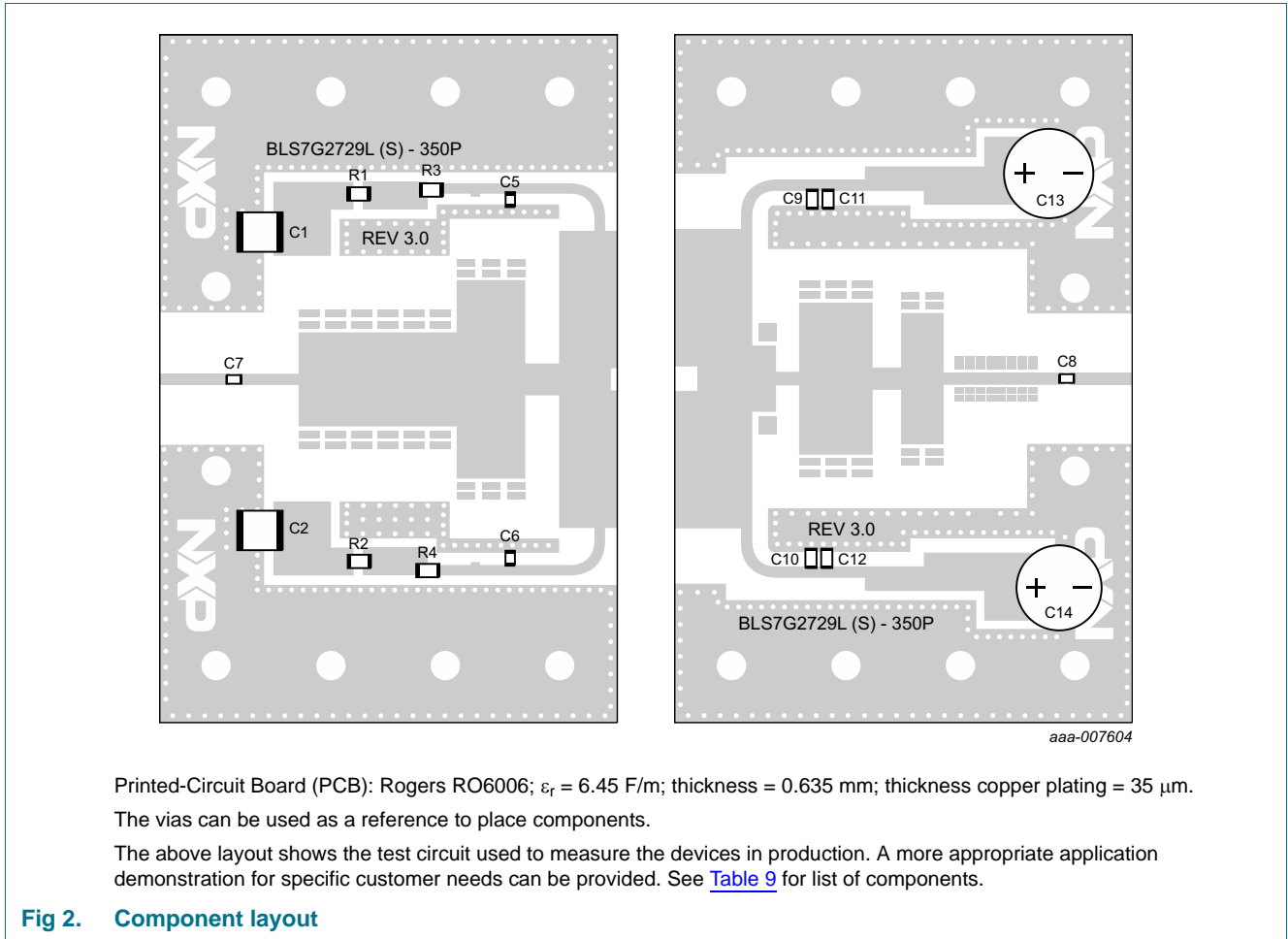
**Table 8. Typical impedance**

f	$Z_S$ [1]	$Z_L$ [1]
GHz	$\Omega$	$\Omega$
2.7	2.8 – j8.7	1.8 – j5.1
2.8	3.9 – j8.2	2.1 – j5.4
2.9	4.8 – j9.3	1.5 – j5.7

[1] Impedances are taken at a single halve of the push-pull transistor



**7.3 Test circuit information**



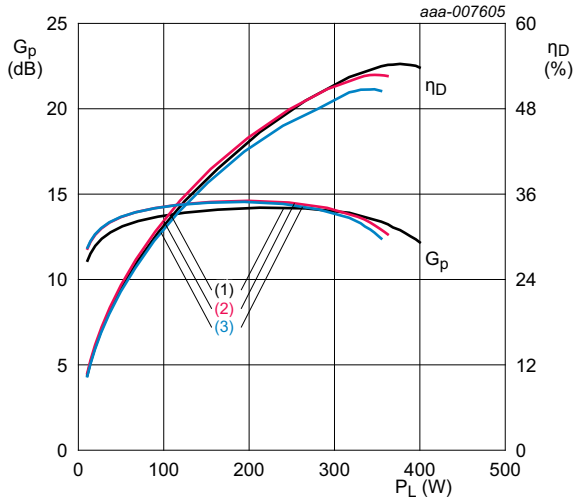
Printed-Circuit Board (PCB): Rogers RO6006;  $\epsilon_r = 6.45$  F/m; thickness = 0.635 mm; thickness copper plating = 35  $\mu\text{m}$ .  
 The vias can be used as a reference to place components.  
 The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be provided. See [Table 9](#) for list of components.

**Fig 2. Component layout**

**Table 9. List of components**  
 See [Figure 2](#) for component layout.

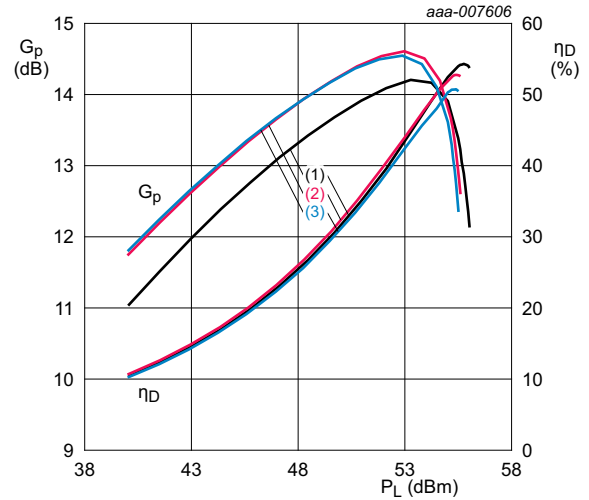
Component	Description	Value	Remarks
C1, C2	SMD capacitor	4.7 $\mu\text{F}$ , 50 V	
C5, C6	multilayer ceramic chip capacitor	12 pF	ATC800A
C7, C8	multilayer ceramic chip capacitor	20 pF	ATC800A
C9, C10	multilayer ceramic chip capacitor	12 pF	ATC800A
C11, C12	multilayer ceramic chip capacitor	1 nF	ATC700A
C13, C14	electrolytic capacitor	220 $\mu\text{F}$ , 63 V	
R1, R2	SMD resistor	9.1 $\Omega$	SMD 0805
R3, R4	SMD resistor	8 $\Omega$	SMD 0805

**7.4 Graphical data**



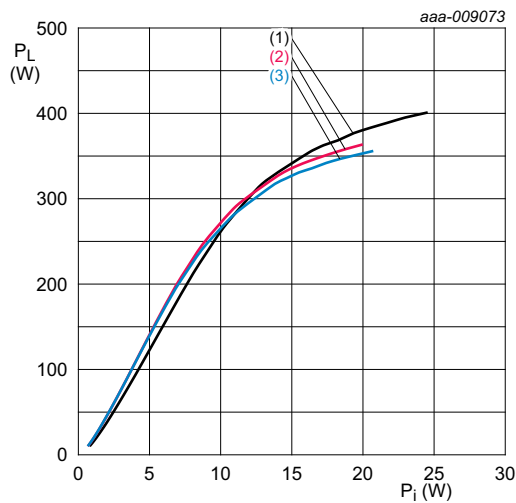
$V_{DS} = 32\text{ V}; I_{Dq} = 200\text{ mA}.$   
 (1)  $f = 2.7\text{ GHz}$   
 (2)  $f = 2.8\text{ GHz}$   
 (3)  $f = 2.9\text{ GHz}$

**Fig 3. Power gain and drain efficiency as function of output power; typical values**



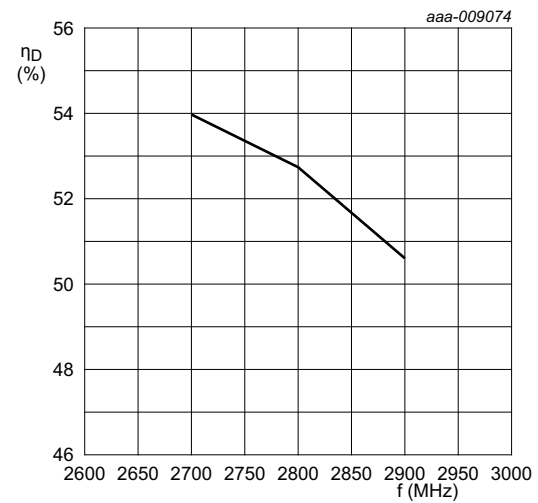
$V_{DS} = 32\text{ V}; I_{Dq} = 200\text{ mA}.$   
 (1)  $f = 2.7\text{ GHz}$   
 (2)  $f = 2.8\text{ GHz}$   
 (3)  $f = 2.9\text{ GHz}$

**Fig 4. Power gain and drain efficiency as function of output power; typical values**



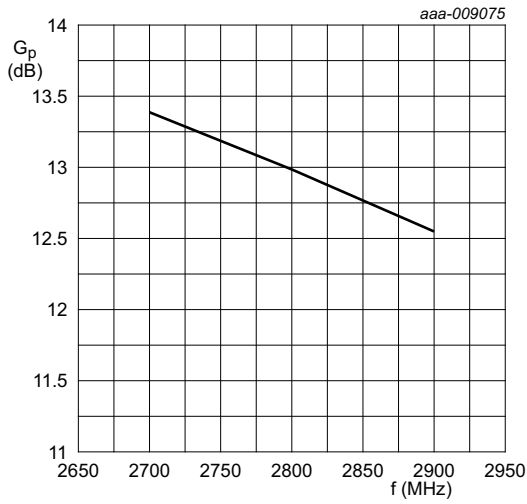
$V_{DS} = 32\text{ V}; I_{Dq} = 200\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }%.$   
 (1)  $f = 2.7\text{ GHz}$   
 (2)  $f = 2.8\text{ GHz}$   
 (3)  $f = 2.9\text{ GHz}$

**Fig 5. Output power as a function of input power; typical values**



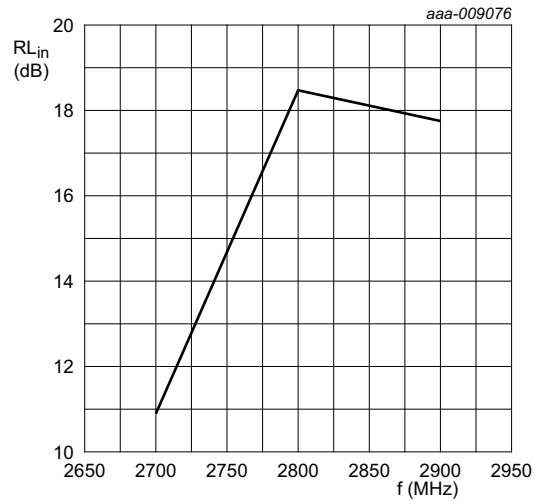
$V_{DS} = 32\text{ V}; I_{Dq} = 200\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }%; P_L = 350\text{ W}.$

**Fig 6. Drain efficiency as a function of frequency; typical values**



$V_{DS} = 32\text{ V}$ ;  $I_{Dq} = 200\text{ mA}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ;  
 $P_L = 350\text{ W}$ .

**Fig 7. Power gain as a function of frequency; typical values**



$V_{DS} = 32\text{ V}$ ;  $I_{Dq} = 200\text{ mA}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ;  
 $P_L = 350\text{ W}$ .

**Fig 8. Input return loss as a function of frequency; typical values**

**8. Package outline**

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

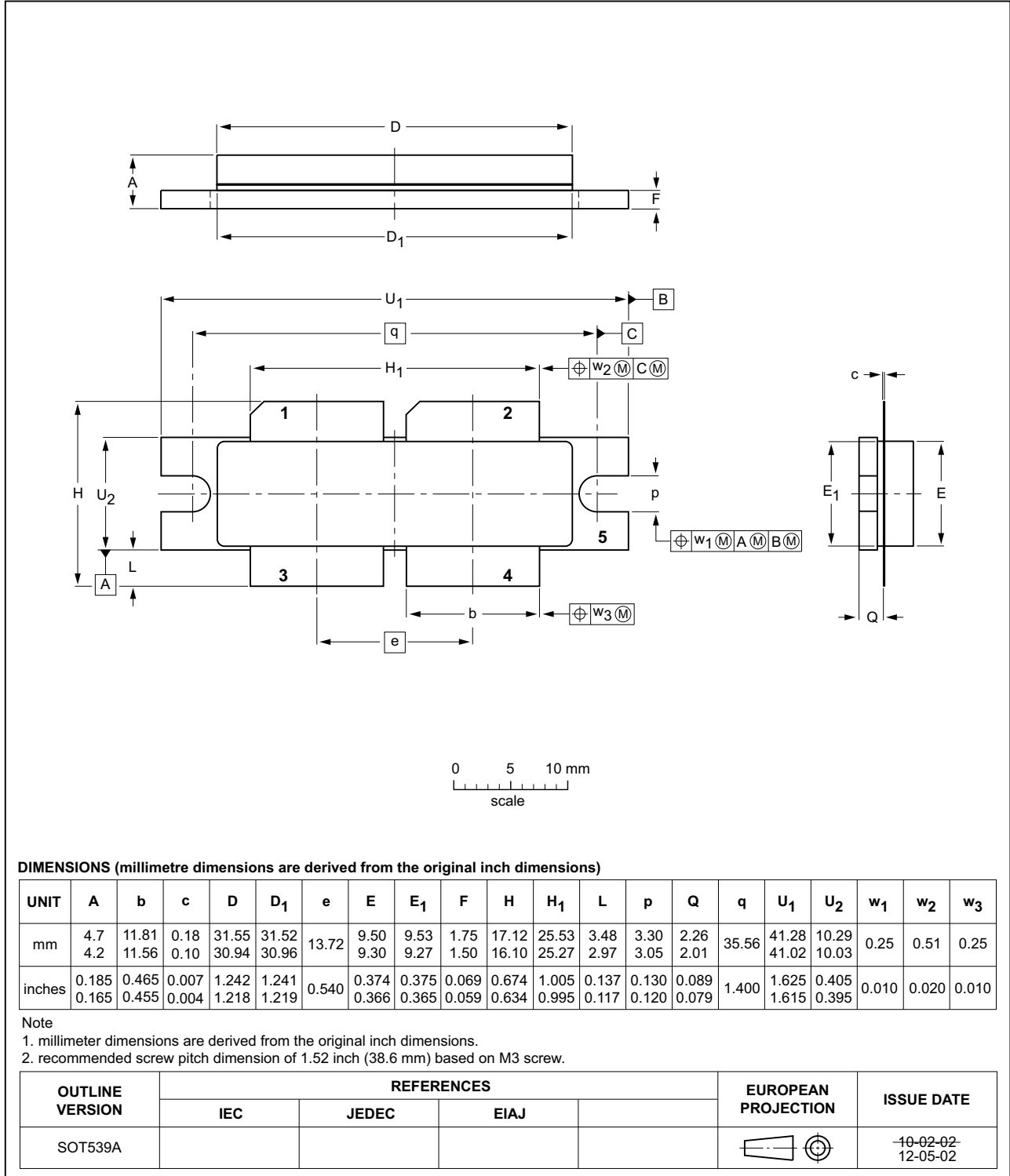


Fig 9. Package outline SOT539A



Earless flanged balanced ceramic package; 4 leads

SOT539B

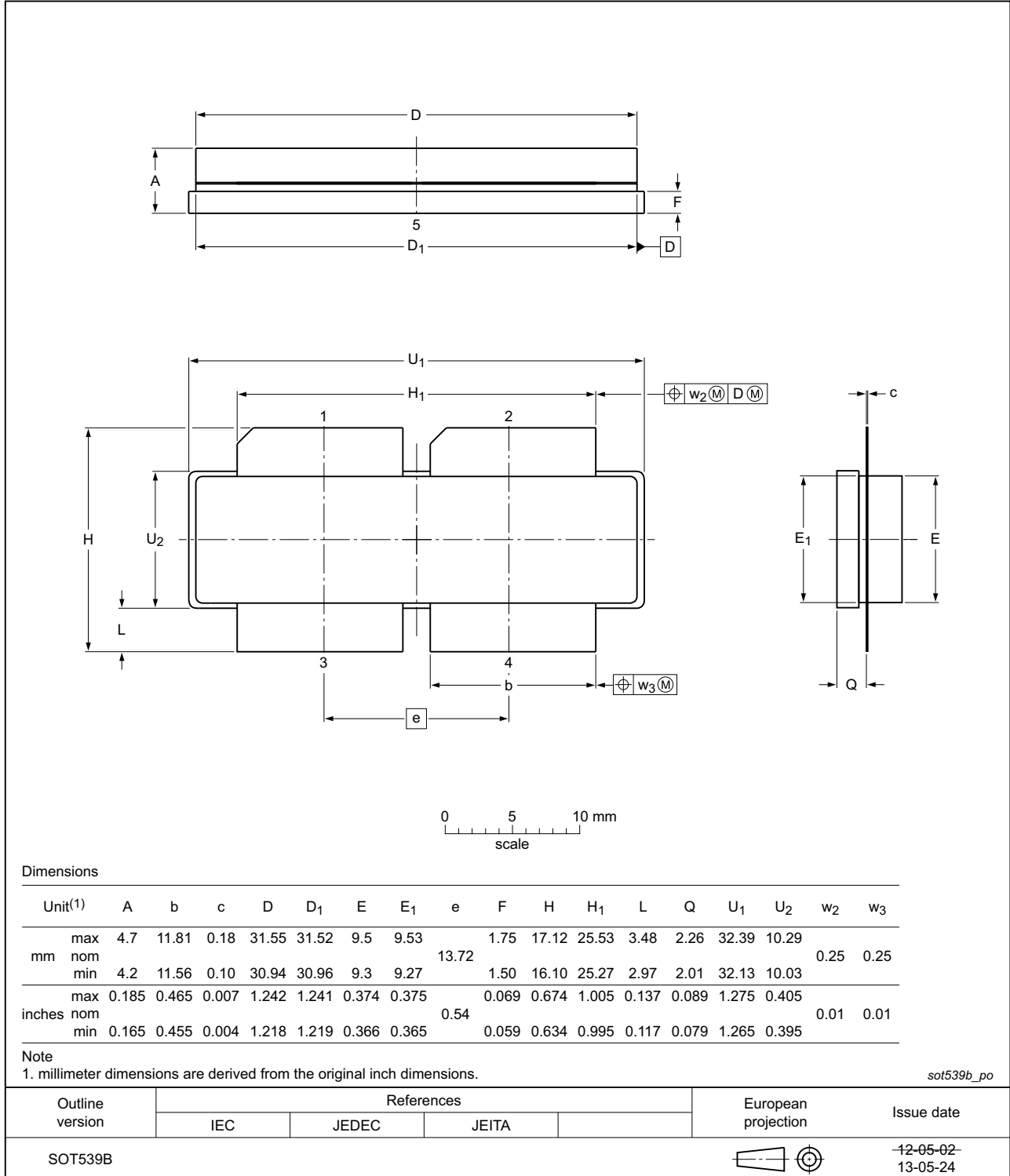


Fig 10. Package outline SOT539B

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
S-band	Short wave Band
SMD	Surface-Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS7G2729L-350P_LS-350P v.5	20140516	Product data sheet	-	BLS7G2729L-350P_LS-350P v.4
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Figure 3 on page 6</a>: figure has been corrected.</li> </ul>			
BLS7G2729L-350P_LS-350P v.4	20130923	Product data sheet	-	BLS7G2729L-350P_LS-350P v.3
BLS7G2729L-350P_LS-350P v.3	20130712	Objective data sheet	-	BLS7G2729L-350P_LS-350P v.2
BLS7G2729L-350P_LS-350P v.2	20130506	Objective data sheet	-	BLS7G2729L-350P_LS-350P v.1
BLS7G2729L-350P_LS-350P v.1	20110524	Objective data sheet	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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