BLS8G2731L-400P; BLS8G2731LS-400P

LDMOS S-band radar power transistor

AMPLEON

Rev. 2 — 1 September 2015

Product data sheet

1. Product profile

1.1 General description

400 W LDMOS power transistor for S-band radar applications in the frequency range from 2.7 GHz to 3.1 GHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 50 µs; δ = 2 %; I_{Dq} = 200 mA; in a class-AB demo test circuit.

Test signal	f	V_{DS}	$P_{L(1dB)}$	G_p [1]	η_D [1]	$P_{L(2dB)}$	G_p [2]	η_D [2]
	(GHz)	(V)	(W)	(dB)	(%)	(W)	(dB)	(%)
pulsed RF	2.7 to 2.9	32	540	11	45	610	10	46
	2.9 to 3.1	32	490	12	47	550	11	49
	2.7 to 3.1	32	530	12	45	590	11	47

[1] at 1 dB gain compression.

[2] at 2 dB gain compression.

1.2 Features and benefits

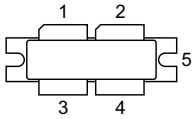
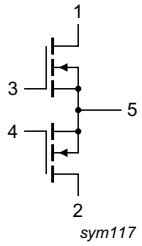
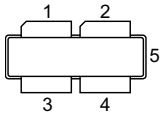
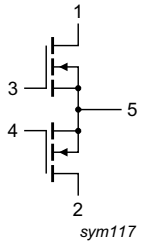
- High efficiency
- Excellent ruggedness
- Designed for S-band operation
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- S-band radar applications in the frequent range 2.7 GHz to 3.1 GHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLS8G2731L-400P (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLS8G2731LS-400P (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS8G2731L-400P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLS8G2731LS-400P	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	65	V
V_{GS}	gate-source voltage	–6	+11	V
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature [1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-mb)}$	transient thermal impedance from junction to mounting base	T_{case} = 85 °C; P_L = 400 W		
		t_p = 100 μs; δ = 10 %	0.067	K/W
		t_p = 200 μs; δ = 10 %	0.083	K/W
		t_p = 300 μs; δ = 10 %	0.091	K/W
		t_p = 100 μs; δ = 20 %	0.082	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	51	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 15.0 A	-	21	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 10.5 A	-	0.058	-	Ω

Table 7. RF characteristics

Test signal: pulsed RF; f = 3.1 GHz; t_p = 300 μs; δ = 10 %; RF performance at V_{DS} = 32 V; I_{Dq} = 200 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB narrow band production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 400 W	10.3	13	-	dB
η_D	drain efficiency	P_L = 400 W	43	47	-	%
RL_{in}	input return loss	P_L = 400 W	-	−8	-	dB
$P_{droop(pulse)}$	pulse droop power	P_L = 400 W	-	0	0.5	dB
t_r	rise time	P_L = 400 W	-	5	50	ns
t_f	fall time	P_L = 400 W	-	5	50	ns
$P_{L(2dB)}$	output power at 2 dB gain compression		400	-	-	W

7. Test information

7.1 Ruggedness in class-AB operation

The BLS8G2731L-400P and BLS8G2731LS-400P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 200 mA; P_L = 400 W; t_p = 300 μs; δ = 10 %.

7.2 Impedance information

Table 8. Typical impedance

f	Z_S[1]	Z_L[1]
(GHz)	(Ω)	(Ω)
2.7	1.0 – 7.0j	1.8 – 4.9j
2.9	1.5 – 8.5j	2.5 – 5.2j
3.1	4.0 – 9.0j	3.6 – 4.7j

[1] Impedances are taken at a single halve of the push-pull transistor

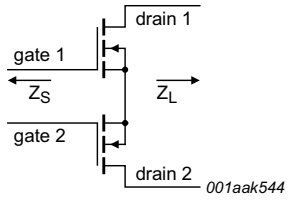
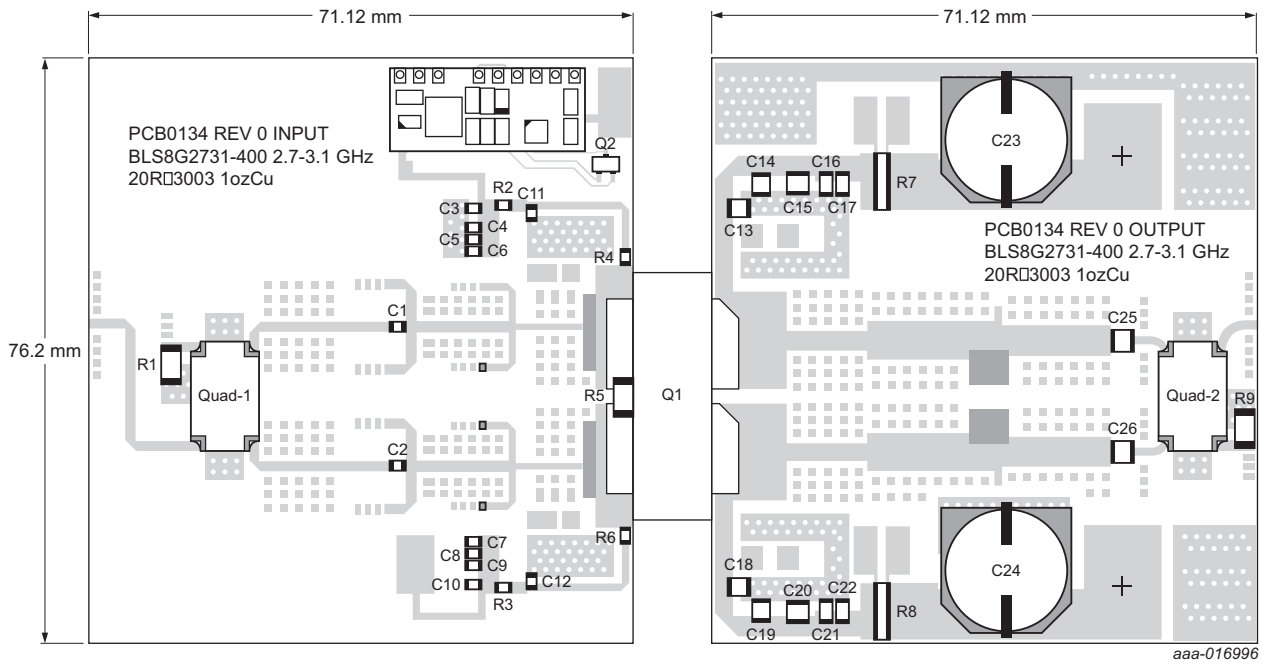


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO3003; thickness = 0.508 mm.

See Table 9 for a list of components.

Fig 2. Component layout for class-AB production test circuit

Table 9. List of components

For test circuit see Figure 2.

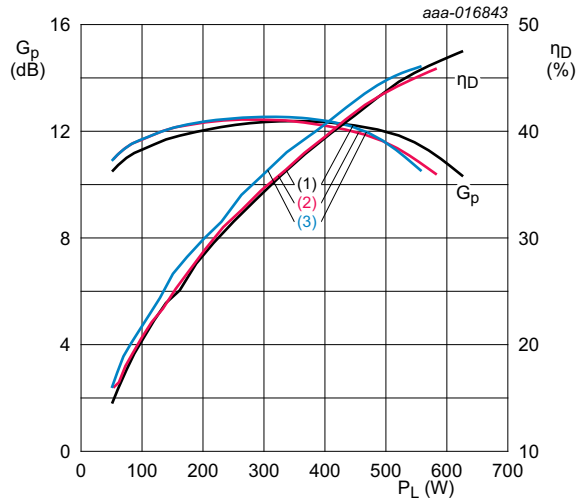
Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	5.6 pF	ATC: ATC600F5R6
C3, C10	multilayer ceramic chip capacitor	220 pF, 50 V	Murata: GRM2165C1H221JA01D
C4, C9	multilayer ceramic chip capacitor	10 nF, 50 V	Murata: GRM216R71H103KA01D
C5, C8	multilayer ceramic chip capacitor	100 nF, 50 V	Murata: GRM21BR71H104KA01L
C6, C7	multilayer ceramic chip capacitor	10 μF, 10 V	Murata: GRM21BR61A106KE19L
C11, C12	multilayer ceramic chip capacitor	15 pF	ATC: ATC600F150
C13, C14, C18, C19, C25, C26	multilayer ceramic chip capacitor	22 pF	Passive Plus: 1111N220GW501
C15, C20	electrolytic capacitor	560 pF	Passive Plus: 1111N561GW501
C16, C21	multilayer ceramic chip capacitor	0.01 μF, 250 V	Murata: GRM31B7U2E103JW31L
C17,C22	multilayer ceramic chip capacitor	0.1 μF, 250 V	Murata: GRM32DR72E104KW01L
C23, C24	electrolytic capacitor	470 μF, 63 V	Panasonic: EEV-TG1J471M
R1, R9	resistor	50 Ω	EMC: SMT2010TALN
R2, R3	shunt resistor	9.1 Ω	Vishay Dale: CRCW08059R10FKEA
R4, R6	shunt resistor	5.1 Ω	Vishay Dale: CRCW08055R10FKEA
R5	shunt resistor	510 Ω	Vishay Dale: CRCW2010510RFKEFHP
R7, R8	resistor	0.01 Ω	Susumu: RL7520WT-R010-F

Table 9. List of components *...continued*

For test circuit see Figure 2.

Component	Description	Value	Remarks
Q1	transistor	-	Ampleon: BLS8G2731LS-400P
Q2	transistor	-	NXP: MMBT2222A
Quad-1, Quad-2	90 degree hybrid coupler	-	Innovative Power Products: IPP-7075

7.4 Graphical data



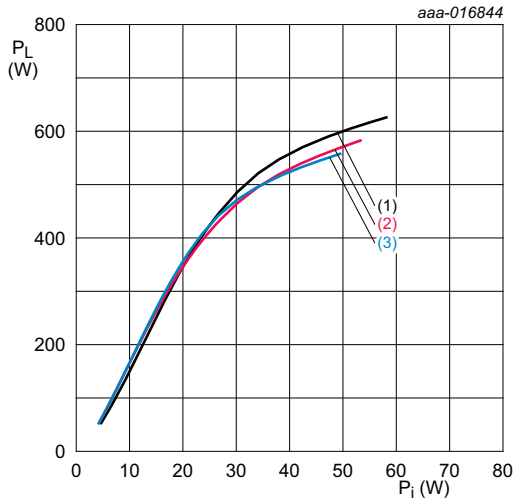
V_{DS} = 32 V; I_{Dq} = 200 mA; t_p = 100 μs; δ = 2 %.

(1) f = 2700 MHz

(2) f = 2900 MHz

(3) f = 3100 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



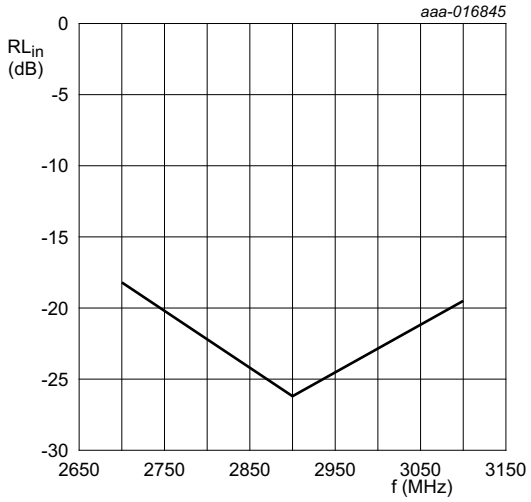
V_{DS} = 32 V; I_{Dq} = 200 mA; t_p = 100 μs; δ = 2 %.

(1) f = 2700 MHz

(2) f = 2900 MHz

(3) f = 3100 MHz

Fig 4. Output power as a function of input power; typical values

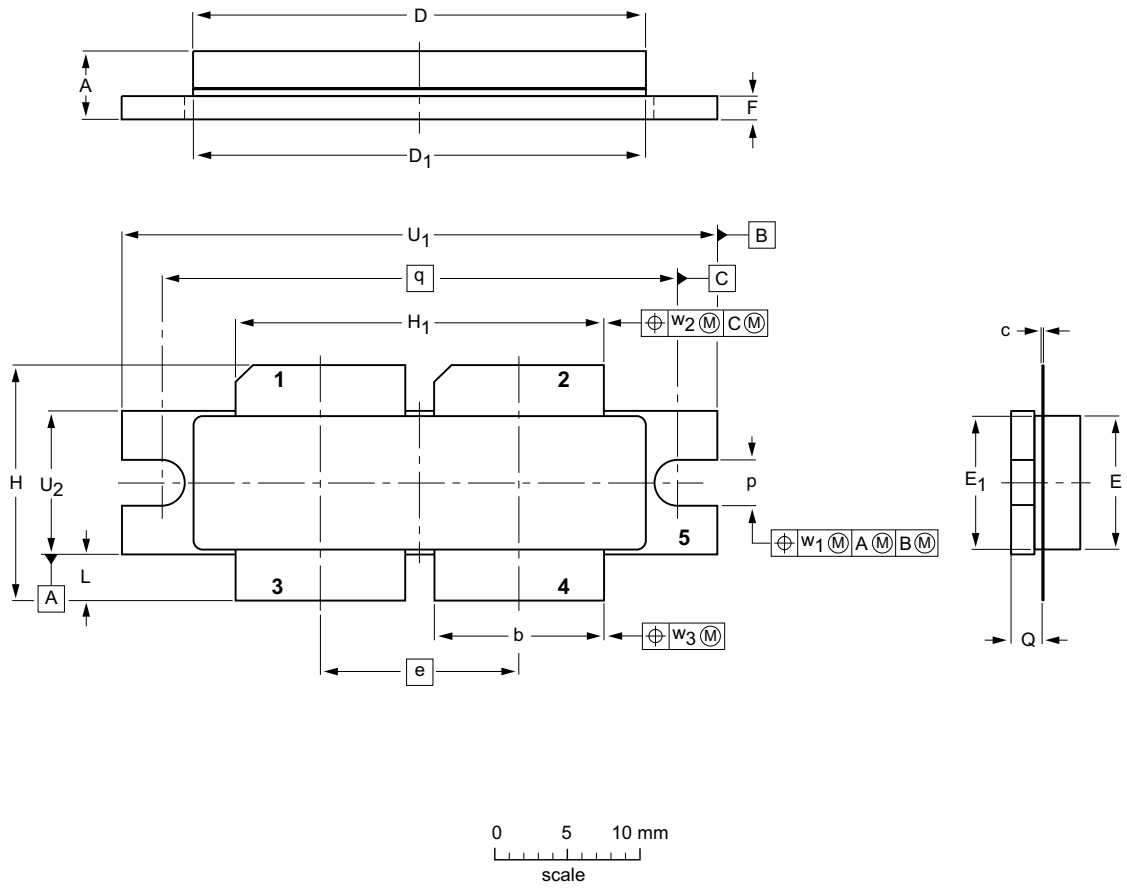


V_{DS} = 32 V; I_{Dq} = 200 mA; P_i = 10 dBm.

Fig 5. Input return loss as a function of frequency; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

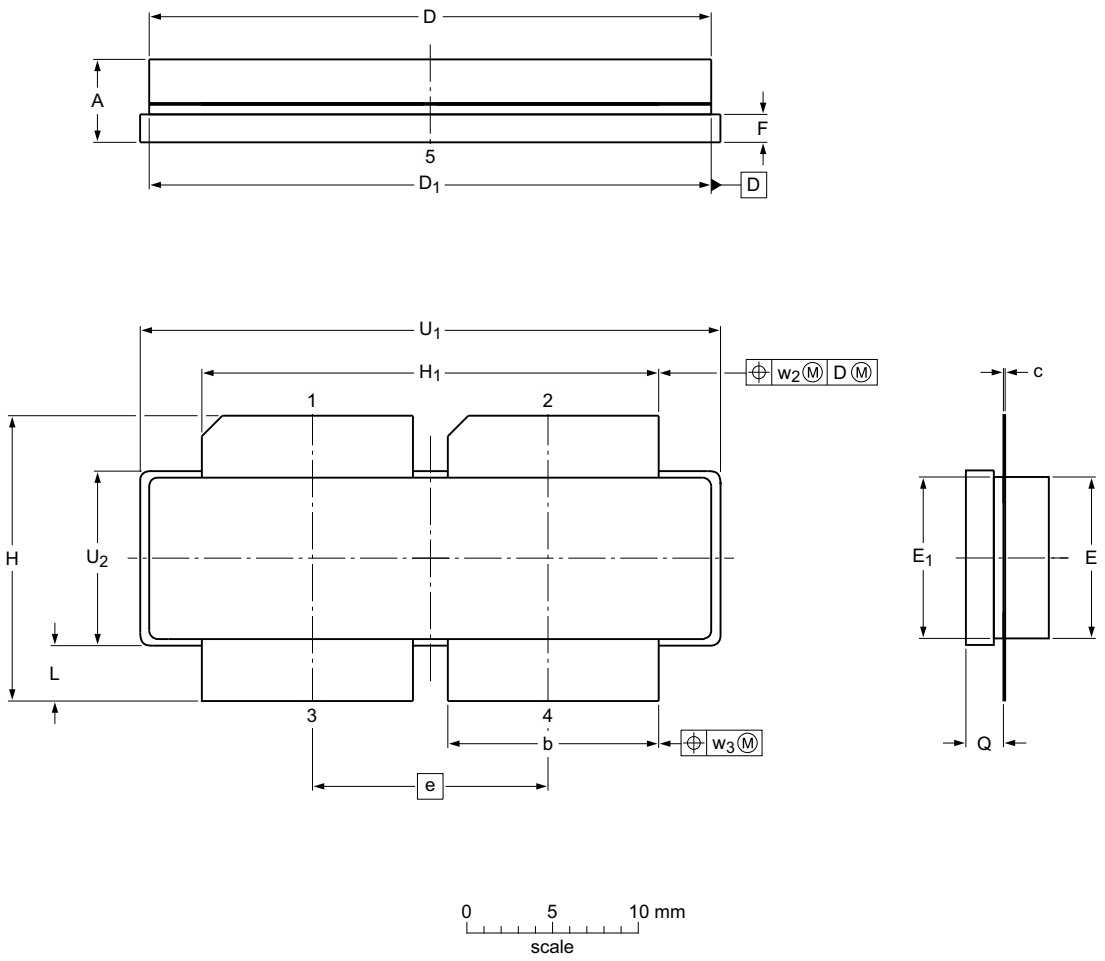
UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 6. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53	13.72	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	nom																	
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375	0.54	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	nom																	
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 7. Package outline SOT539B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
S-band	Short wave Band
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS8G2731L-400P_LS-400P#2	20150901	Product data sheet		BLS8G2731L-400P_LS-400P v.1
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLS8G2731L-400P_LS-400P v.1	20150526	Product data sheet	-	-

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12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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