

DATA SHEET

BLV92 UHF power transistor

Product specification

March 1993

UHF power transistor

BLV92

DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily intended for use in mobile radio transmitters in the 900 MHz communications band.

FEATURES

- multi-base structure and emitter-ballasting resistors for an optimum temperature profile
- internal input matching to achieve an optimum wideband capability and high power gain
- gold metallization ensures excellent reliability.

The transistor has a 6-lead flange envelope with a ceramic cap (SOT-171). All leads are isolated from the flange.

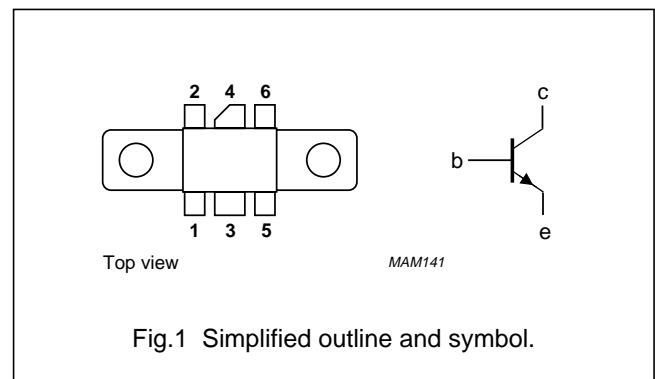
QUICK REFERENCE DATA

R.F. performance at $T_h = 25\text{ }^\circ\text{C}$ in a common-emitter class-B test circuit

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η_c %
narrow band; c.w.	12,5	900	4	> 7,5	> 50
	9,6	900	3	typ. 7,3	typ. 56

PINNING - SOT171A

PIN	SYMBOL	DESCRIPTION
1	e	emitter
2	e	emitter
3	b	base
4	c	collector
5	e	emitter
6	e	emitter



WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)

peak value

V_{CBOM} max. 36 V

Collector-emitter voltage (open base)

V_{CEO} max. 16 V

Emitter-base voltage (open collector)

V_{EBO} max. 3 V

Collector current

d.c. or average

I_C max. 0,8 A

(peak value); $f > 1$ MHz

I_{CM} max. 2,4 A

Total power dissipation

at $T_{mb} = 94$ °C

$P_{tot(dc)}$ max. 9 W

at $T_{mb} = 94$ °C; $f > 1$ MHz

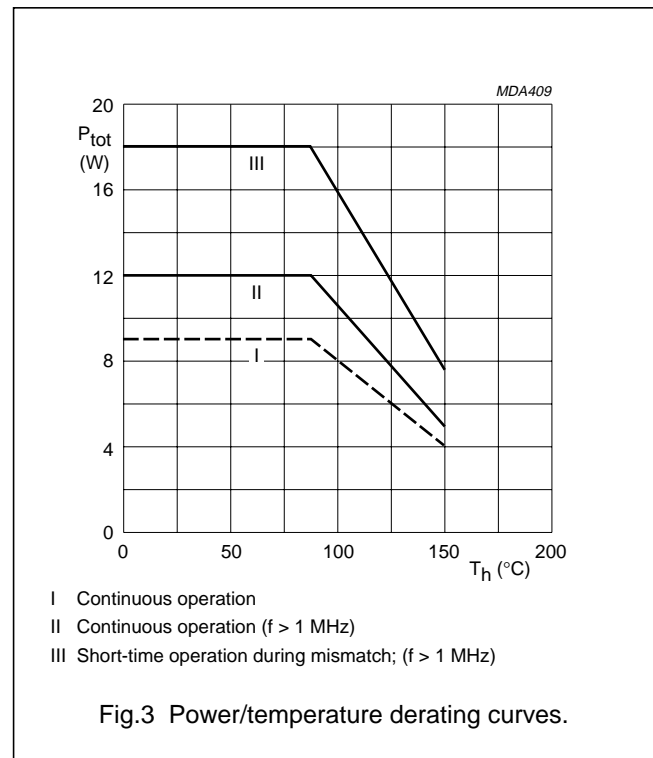
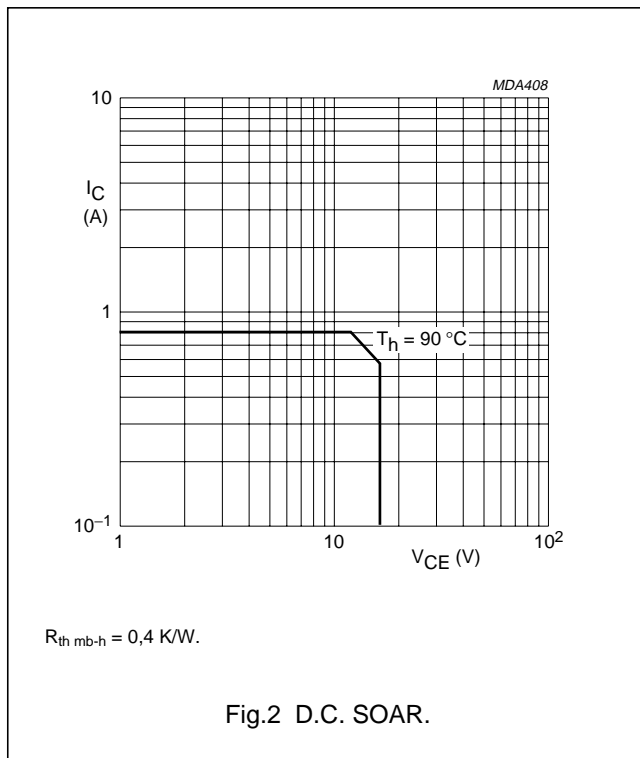
$P_{tot(rf)}$ max. 12 W

Storage temperature

T_{stg} -65 to + 150 °C

Operating junction temperature

T_j max. 200 °C



THERMAL RESISTANCE

Dissipation = 6 W; $T_{mb} = 128$ °C

From junction to mounting base

(d.c. dissipation)

$R_{th\ j-mb(dc)}$ max. 12 K/W

(r.f. dissipation)

$R_{th\ j-mb(rf)}$ max. 9 K/W

From mounting base to heatsink

$R_{th\ mb-h}$ max. 0,4 K/W

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CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Collector-base breakdown voltage, open emitter; $I_C = 10\text{ mA}$

Collector-emitter breakdown voltage, open base; $I_C = 20\text{ mA}$

Emitter-base breakdown voltage, open collector; $I_E = 1\text{ mA}$

Collector cut-off current, $V_{BE} = 0$; $V_{CE} = 16\text{ V}$

Second breakdown energy, $L = 25\text{ mH}$; $f = 50\text{ Hz}$; $R_{BE} = 10\text{ }\Omega$

D.C. current gain, $I_C = 0,6\text{ A}$; $V_{CE} = 10\text{ V}$

Transition frequency at $f = 500\text{ MHz}^{(1)}$, $-I_E = 0,6\text{ A}$; $V_{CB} = 12,5\text{ V}$

Collector capacitance at $f = 1\text{ MHz}$, $I_E = i_e = 0$; $V_{CB} = 12,5\text{ V}$

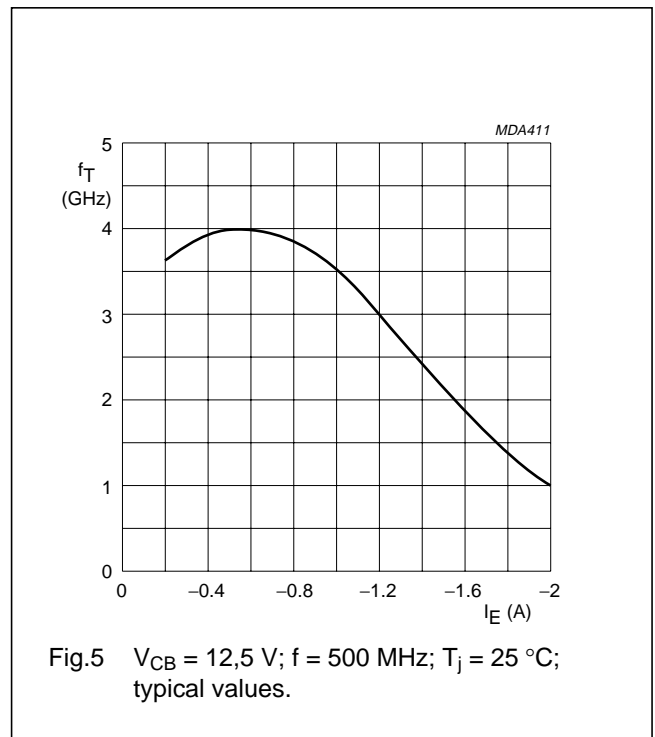
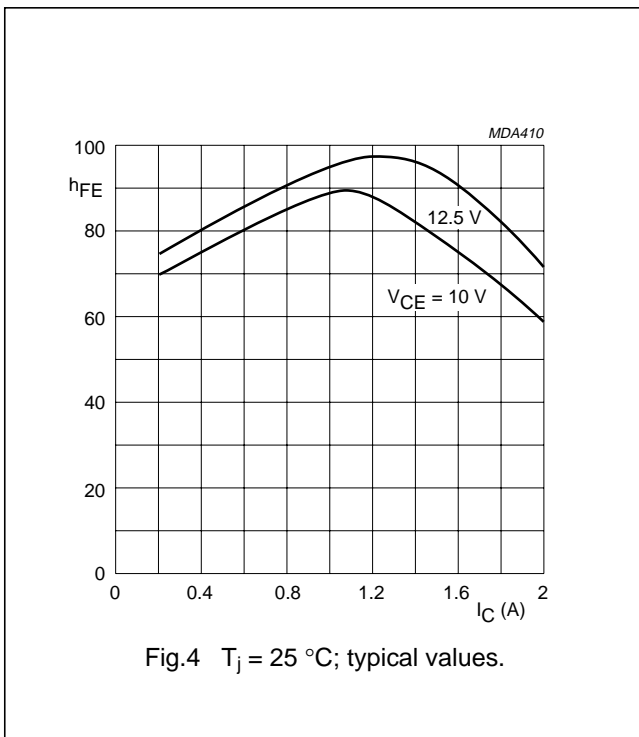
Feed-back capacitance at $f = 1\text{ MHz}$, $I_C = 0$; $V_{CE} = 12,5\text{ V}$

Collector-flange capacitance

$V_{(BR)CBO}$	>	36 V
$V_{(BR)CEO}$	>	16 V
$V_{(BR)EBO}$	>	3 V
I_{CES}	<	5 mA
E_{SBR}	>	1 mJ
h_{FE}	>	25
f_T	typ.	4 GHz
C_c	typ.	8 pF
C_{re}	typ.	5 pF
C_{cf}	typ.	2 pF

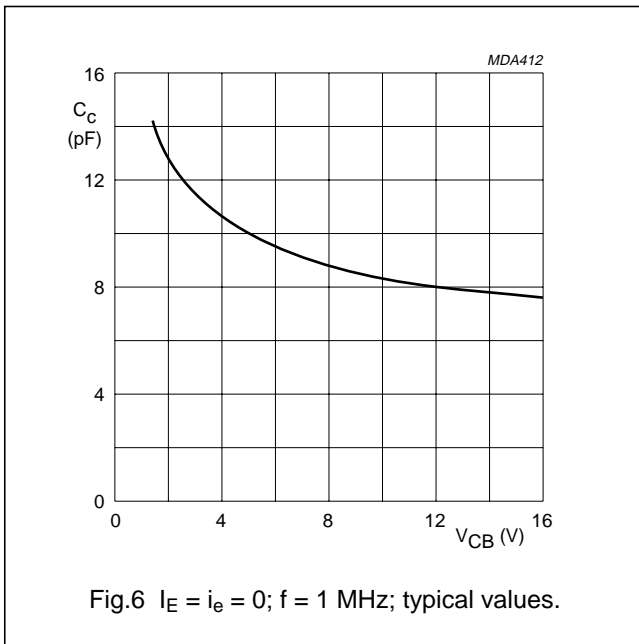
Note

1. Measured under pulse conditions: $t_p = 50\text{ }\mu\text{s}$; $\delta < 1\%$.



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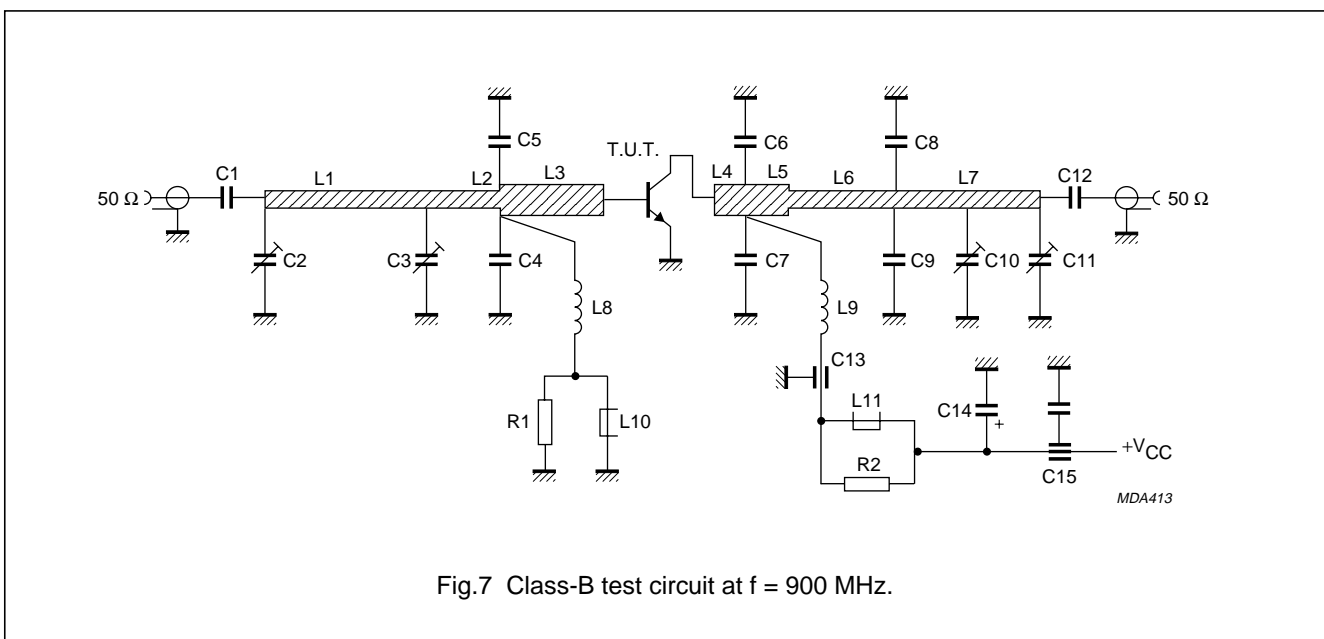
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APPLICATION INFORMATION

R.F. performance in c.w. operation (common-emitter circuit; class-B): f = 900 MHz; T_h = 25 °C.

MODE OF OPERATION	V _{CE} V	P _L W	P _S W	G _P dB	I _C A	η _c %
narrow band; c.w.	12,5	4	< 0,71 typ. 0,57	> 7,5 typ. 8,5	< 0,64 typ. 0,56	> 50 typ. 57
	9,6	3	typ. 0,56	typ. 7,3	typ. 0,56	typ. 56



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List of components:

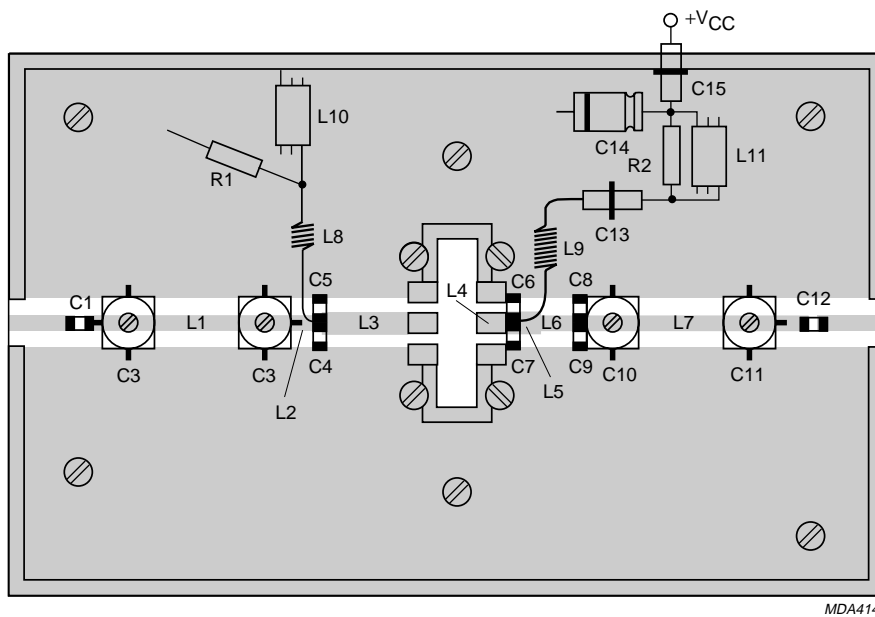
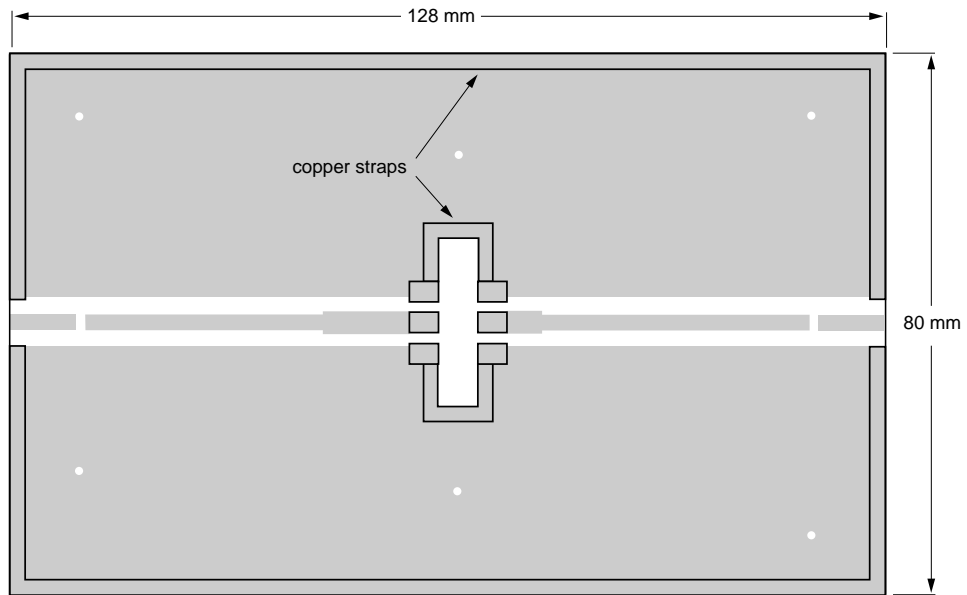
- C1 = C12 = 33 pF multilayer ceramic chip capacitor
 - C2 = C3 = C10 = C11 = 1,4 to 5,5 pF film dielectric trimmer (cat. no. 2222 809 09001)
 - C4 = C5 = 3,9 pF multilayer ceramic chip capacitor⁽¹⁾
 - C6 = C7 = C8 = C9 = 6,2 pF multilayer ceramic chip capacitor⁽¹⁾
 - C13 = 10 pF ceramic feed-through capacitor
 - C14 = 6,8 μ F (63 V) electrolytic capacitor
 - C15 = 330 pF ceramic feed-through capacitor
 - L1 = 50 Ω stripline (29,5 mm \times 2,4 mm)
 - L2 = 50 Ω stripline (5,5 mm \times 2,4 mm)
 - L3 = 42,7 Ω stripline (16,8 mm \times 3,0 mm)
 - L4 = 42,7 Ω stripline (7,5 mm \times 3,0 mm)
 - L5 = 42,7 Ω stripline (2,0 mm \times 3,0 mm)
 - L6 = 50 Ω stripline (8,5 mm \times 2,4 mm)
 - L7 = 50 Ω stripline (28,0 mm \times 2,4 mm)
 - L8 = 60 nH; 4 turns closely wound enamelled Cu-wire (0,4 mm); int. dia. 3 mm; leads 2 \times 5 mm
 - L9 = 45 nH; 4 turns enamelled Cu-wire (1,0 mm); length 6 mm; int. dia. 4 mm; leads 2 \times 5 mm
 - L10 = L11 = Ferroxcube wideband h.f. choke, grade 3B (cat. no. 4312 020 36642)
 - R1 = R2 = 10 $\Omega \pm 10\%$; 0,25 W, metal film resistor
- L1 to L7 are striplines on a double Cu-clad printed circuit board with P.T.F.E. fibre-glass dielectric ($\epsilon_r = 2,2$); thickness $\frac{1}{32}$ inch.

Note

1. American Technical Ceramics capacitors type 100A or capacitor of same quality.

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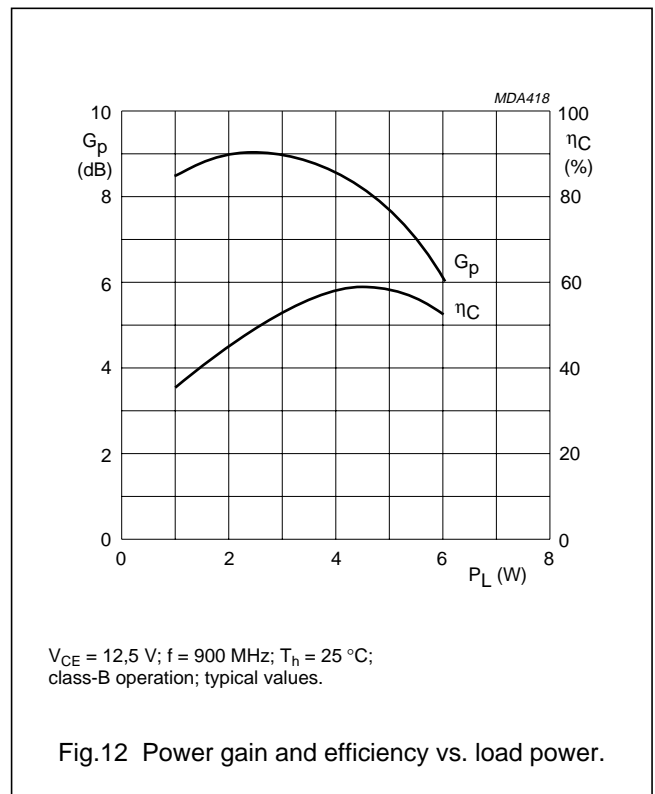
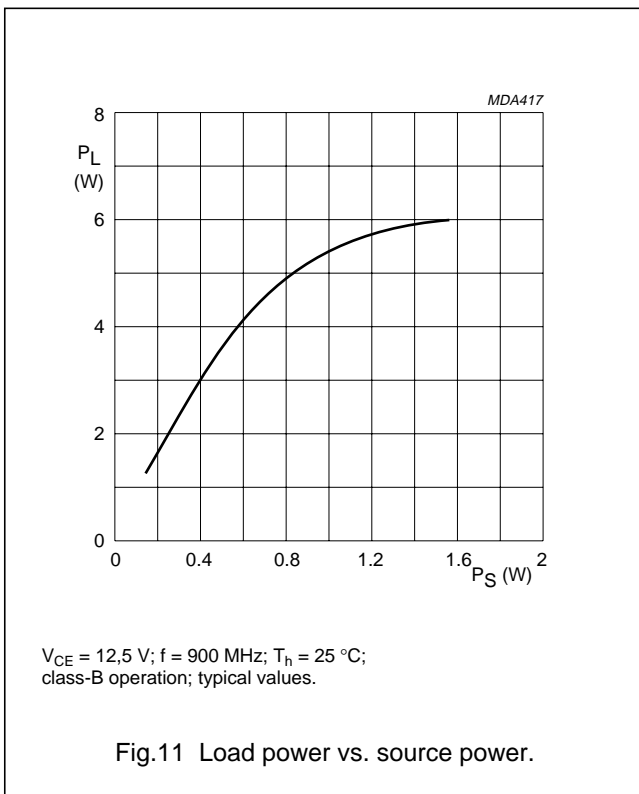
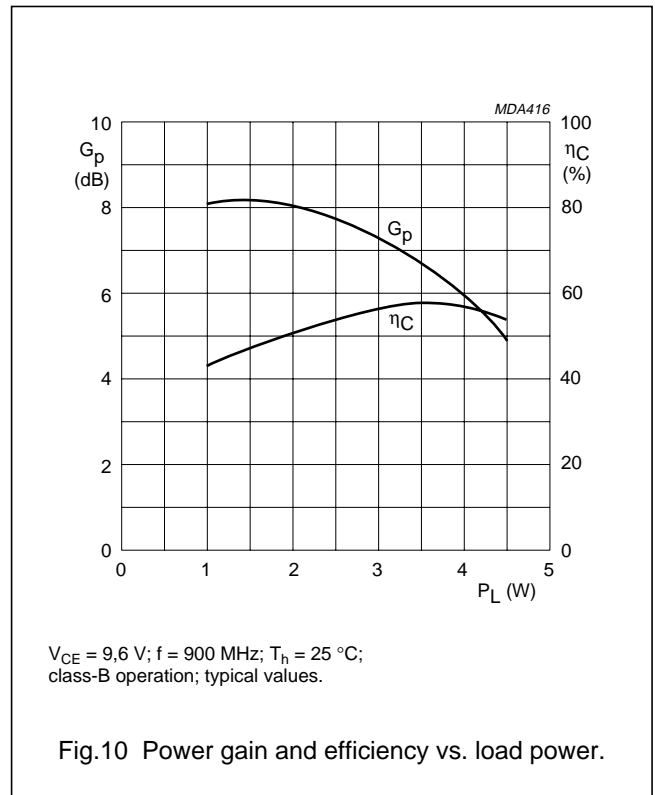
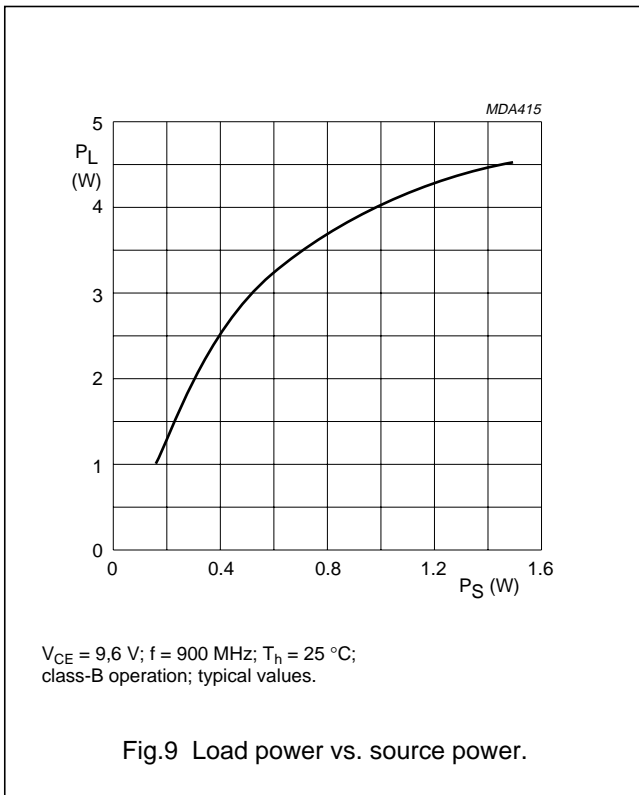
MDA414

The circuit and the components are on one side of the P.T.F.E. fibre-glass board; the other side is unetched copper serving as ground plane. Earth connections are made by fixing screws and copper straps around the board and under the emitters to provide a direct contact between the copper on the component side and the ground plane.

Fig.8 Printed circuit board and component lay-out for 900 MHz class-B test circuit.

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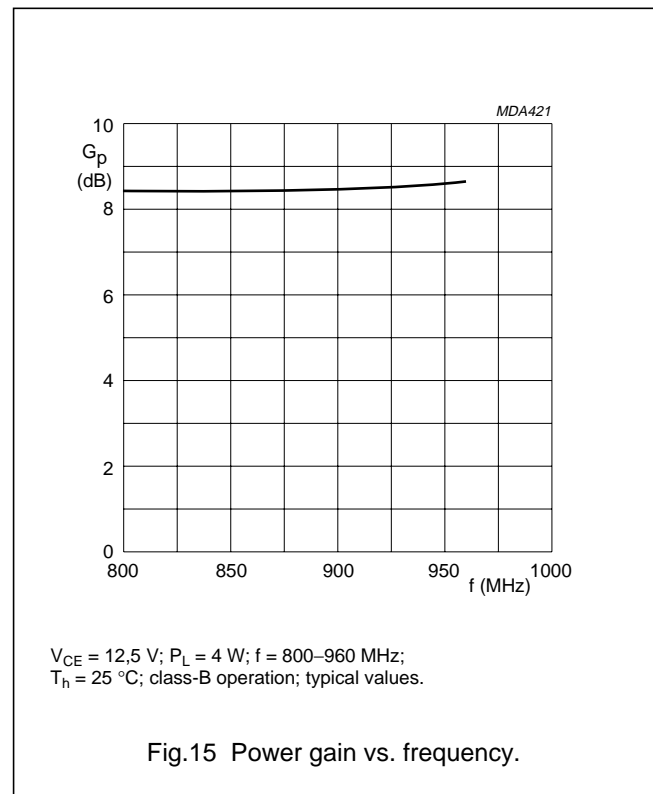
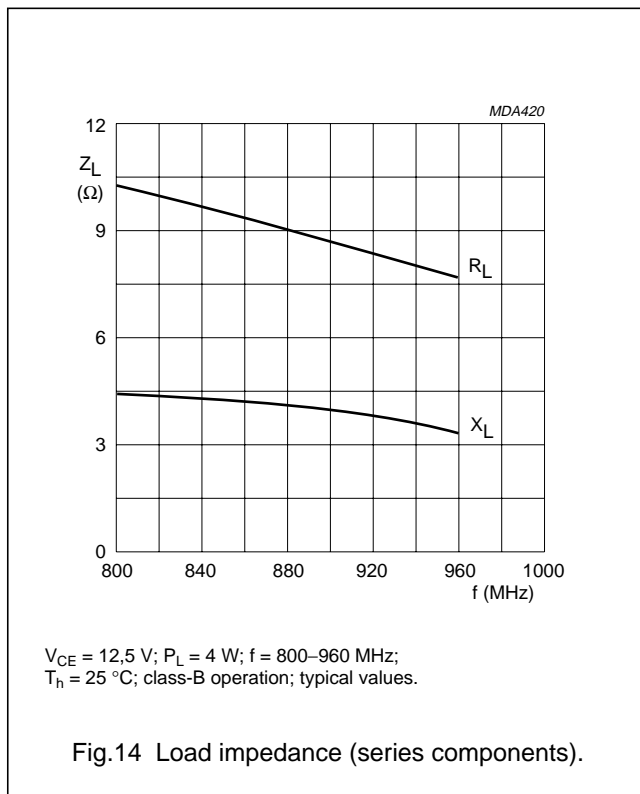
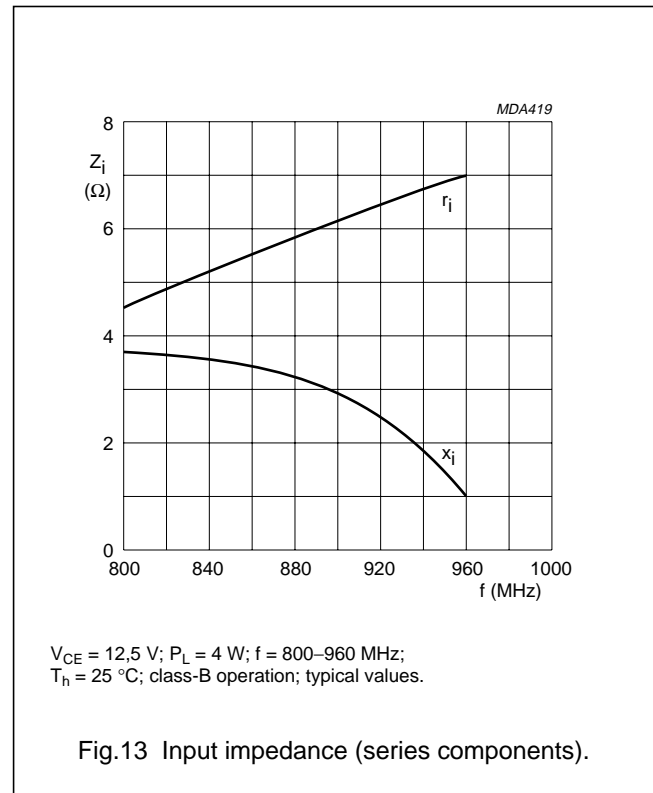


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RUGGEDNESS

The device is capable of withstanding a full load mismatch (VSWR = 50; all phases) at rated load power up to a supply voltage of 15,5 V and at $T_h = 25\text{ }^\circ\text{C}$.



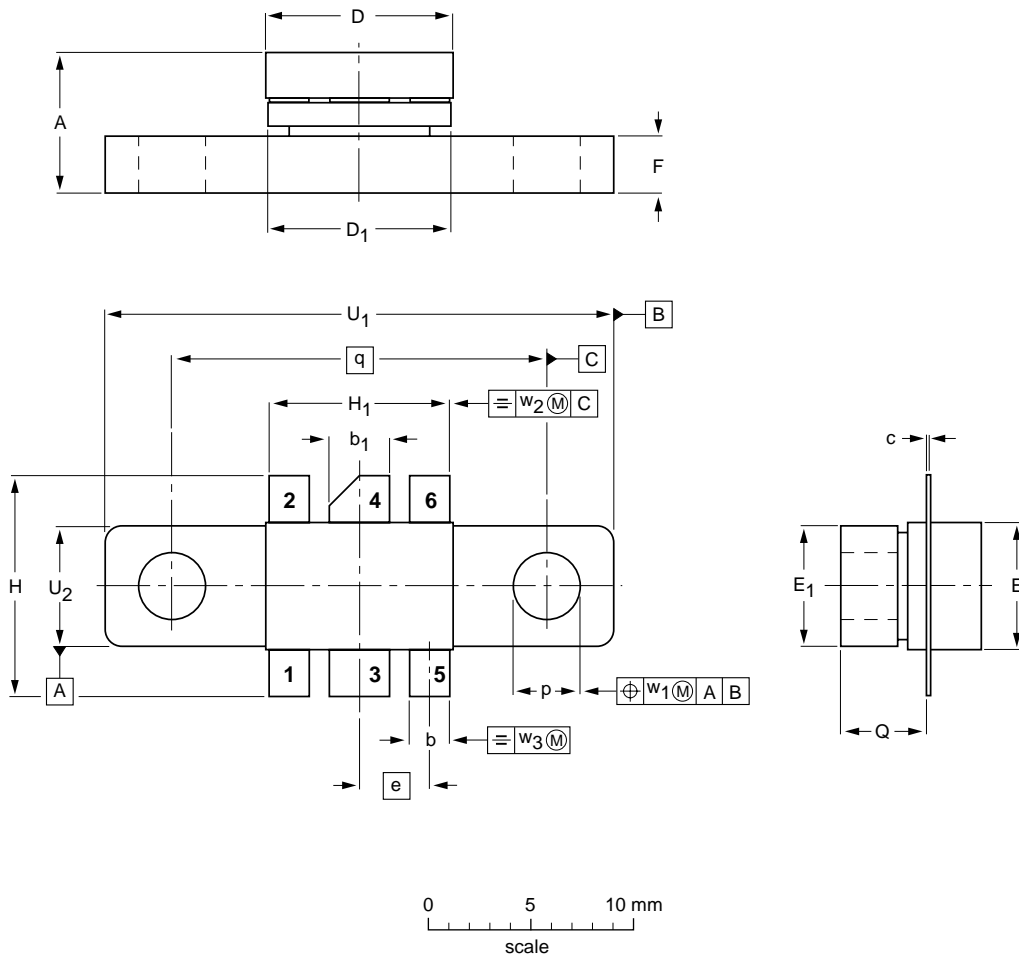
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PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 6 leads

SOT171A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b ₁	c	D	D ₁	E	E ₁	e	F	H	H ₁	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	6.81 6.07	2.15 1.85	3.20 2.89	0.16 0.07	9.25 9.04	9.30 8.99	5.95 5.74	6.00 5.70	3.58	3.05 2.54	11.31 10.54	9.27 9.01	3.43 3.17	4.32 4.11	18.42	24.90 24.63	6.00 5.70	0.51	1.02	0.26
inches	0.268 0.239	0.085 0.073	0.126 0.114	0.006 0.003	0.364 0.356	0.366 0.354	0.234 0.226	0.236 0.224	0.140	0.120 0.100	0.445 0.415	0.365 0.355	0.135 0.125	0.170 0.162	0.725	0.980 0.970	0.236 0.224	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT171A						97-06-28

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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