

IPS Alpha Technology, Ltd.

Date: July.13,2006

TECHNICAL DATA

BM066A001A

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DESCRIPTION

The following specifications are applied to the following Super-TFT module.

Note : Inverter for back light unit is built in this module.

Product Name : BM066A001A

General Specifications

Effective Display Area	: (H)575.769×(V)323.712	(mm)
Number of Pixels	: (H)1,366×(V)768	(pixels)
Pixel Pitch	: (H)0.4215×(V)0.4215	(mm)
Color Pixel Arrangement	: R+G+B Vertical Stripe	
Display Mode	: Transmissive Mode Normally Black Mode	
Top Polarizer Type	: Anti-Glare	
Number of Colors	: 16,777,216	(colors)
Viewing Angle Range	: Super Wide Version (Horizontal & Vertical : 170°, CR ≥ 10)	
Input Signal	: 1-channel LVDS (LVDS:Low Voltage Differential Signaling)	
Back Light	: 7pcs. of CCFL (Type:U-Shape)	
External Dimensions	: (H)626.0×(V)373.0×(t)47.5	(mm)
Weight	: 5,100g typ.	

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	°C	1),5),6)
Humidity	2)		2)		%RH	1)
Vibration	—	4.9(0.5G)	—	14.7 (1.5G)	m/s ²	3)
Shock	—	29.4(3G)	—	294 (30G)	m/s ²	4)
Corrosive Gas	Not Acceptable		Not Acceptable		—	
Illumination at LCD Surface	—	50,000	—	50,000	lx	

Note 1) Temperature and Humidity should be applied to the glass surface of a Super-TFT module, not to the system installed with a module.

The temperature at the center of rear surface should be less than 70°C on the condition of operating. The brightness of a CCFL tends to drop at low temperature. Besides, the life-time becomes shorter at low temperature.

2) $T_a \leq 40^\circ\text{C}$ ······Relative humidity should be less than 85%RH max. Dew is prohibited.

$T_a > 40^\circ\text{C}$ ······Relative humidity should be lower than the moisture of the 85%RH at 40°C.

3) Frequency of the vibration is between 15Hz and 100Hz. (Remove the resonance point)

4) Pulse width of the shock is 10 ms.

5) Long operation under low temperature may cause some portion of display area to be reddish for several minutes after turning on the product.

However, it does not affect the characteristics and reliability of the product.

1.2 Electrical Absolute Maximum Ratings

(1) Super-TFT Module

$V_{SS} = 0\text{ V}$

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	0	13.2	V	
Input Voltage for logic	V_I	-0.3	3.6	V	1)
Electrostatic Durability	V_{ESD0}	±100		V	2),3)
	V_{EDS1}	±8		kV	2),4)

Note 1) It is applied to pixel data signal and clock signal.

2) Discharge Coefficient : 200pF-250Ω, Environmental : 25°C-70%RH

3) It is applied to I/F connector pins.

4) It is applied to the surface of a metallic bezel and a LCD panel.

(2) Back-light Inverter

$V_{SS} = 0\text{ V}$

ITEM	SYMBOL	Min.	Max.	Unit	Note
Input Voltage	V_{in}	-1.0	28.0	V	
ON/OFF Control Input Voltage	ON/OFF	-1.0	5.5	V	
Brightness Control Voltage	BRT	-1.0	5.5	V	

2. INITIAL OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted. The optical characteristics should be measured in a dark room or equivalent state.

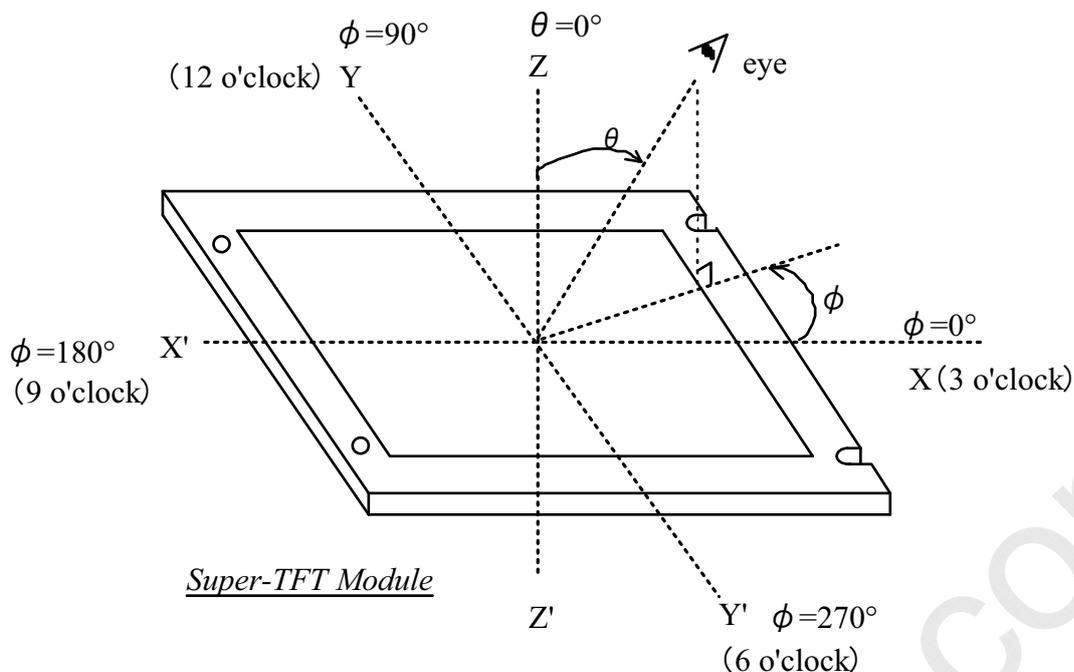
Measuring equipment: CS-1000A, or equivalent

Ambient Temperature =25°C、VDD=12.0V、f V=60Hz、

Vin=24V、BRT=3.15V

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast Ratio		CR		400	750	—	—	2)
Response Time	Rise	ton		—	9	20	ms	3)
	Fall	toff		—	7	20	ms	3)
Brightness of white		Bwh		350	450	—	cd/m ²	
Brightness uniformity		Buni		—	—	30	%	4)
Color Chromaticity (CIE)	Red	χ	$\theta=0^\circ$ 1)	0.62	0.65	0.68	—	[Gray scale =255]
		y		0.30	0.33	0.36		
	Green	χ		0.26	0.29	0.32		
		y		0.58	0.61	0.64		
	Blue	χ		0.12	0.15	0.18		
		y		0.04	0.07	0.10		
	White	χ		0.242	0.272	0.302		
		y		0.248	0.278	0.308		
Variation of Color Position (CIE)	Red	$\Delta \chi$	$\theta=+50^\circ$ $\varphi=0^\circ, 90^\circ$ $80^\circ, 270^\circ$ 1)	—	—	0.04	—	5) [Gray scale =255]
		Δy		—	—	0.04		
	Green	$\Delta \chi$		—	—	0.04		
		Δy		—	—	0.04		
	Blue	$\Delta \chi$		—	—	0.04		
		Δy		—	—	0.04		
	White	$\Delta \chi$		—	—	0.04		
		Δy		—	—	0.04		
Contrast Ratio at 85°		CR85°		10	—	—	—	Estimated Value

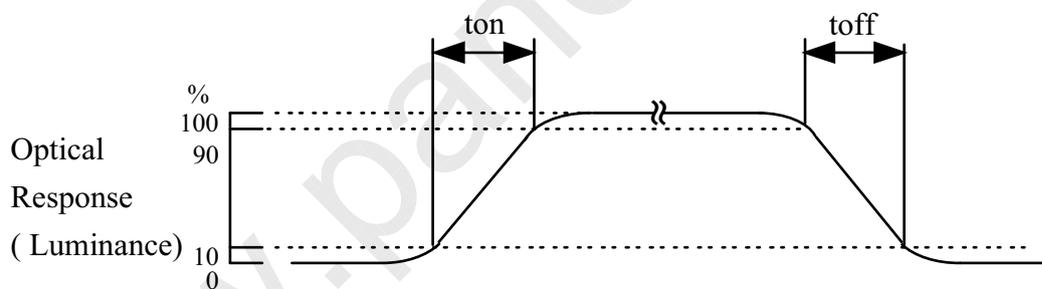
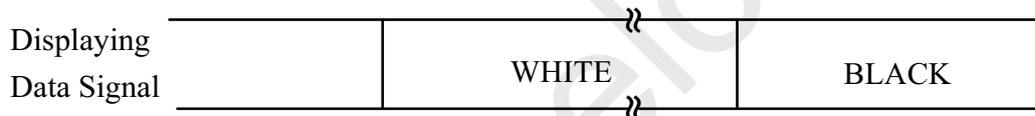
Note 1) Definition of Viewing Angle



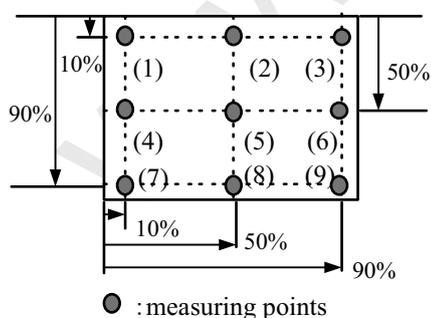
2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformity



Display pattern is white (255 level). The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

$$Buni = \frac{|B_{max \text{ or } B_{min}} - B_{ave}|}{B_{ave}} \times 100$$

where, B_{max} = Maximum brightness

B_{min} = Minimum brightness

$$B_{ave} = \text{Average brightness} = \frac{\sum_{k=1}^9 (B(k))}{9}$$

5) Variation of color position on CIE is defined as difference between colors at $\theta=0^\circ$ and at $\theta=50^\circ$ & $\phi=0^\circ, 90^\circ, 180^\circ, 270^\circ$.

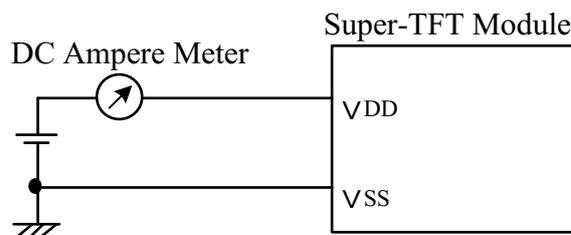
3. ELECTRICAL CHARACTERISTICS

3.1 TFT-LCD Module

 $T_a=25^{\circ}\text{C}$, $V_{ss}=0\text{V}$

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	11.4	12.0	12.6	V	
Power Supply Current	I_{DD}	—	0.4	0.6	A	1),2)
Ripple Voltage of Power Supply	V_{DDR}	—	—	0.15	V	

Note 1) DC current at $f_v=60.0\text{Hz}$, $f_{\text{CLK}}=82\text{MHz}$, $V_{DD}=12.0\text{V}$ and Display pattern is Horizontal stripe.



- 2) Current fuse is built in a module. Current capacity of power supply for VDD should be larger than 4A, so that the fuse can be opened at the trouble of power supply.

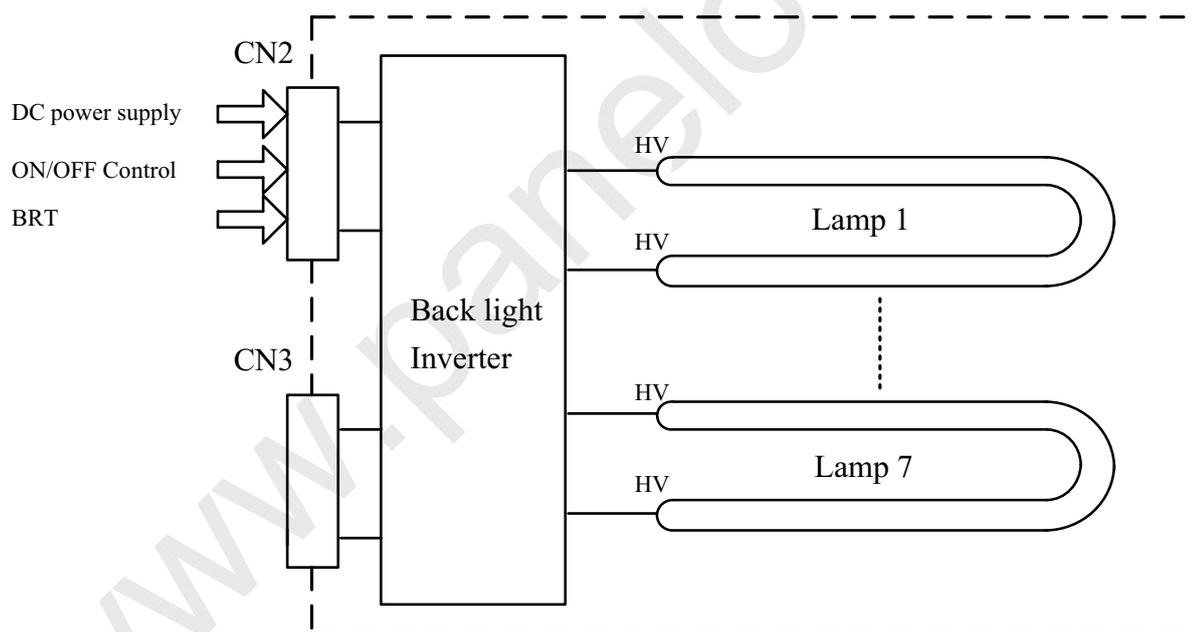
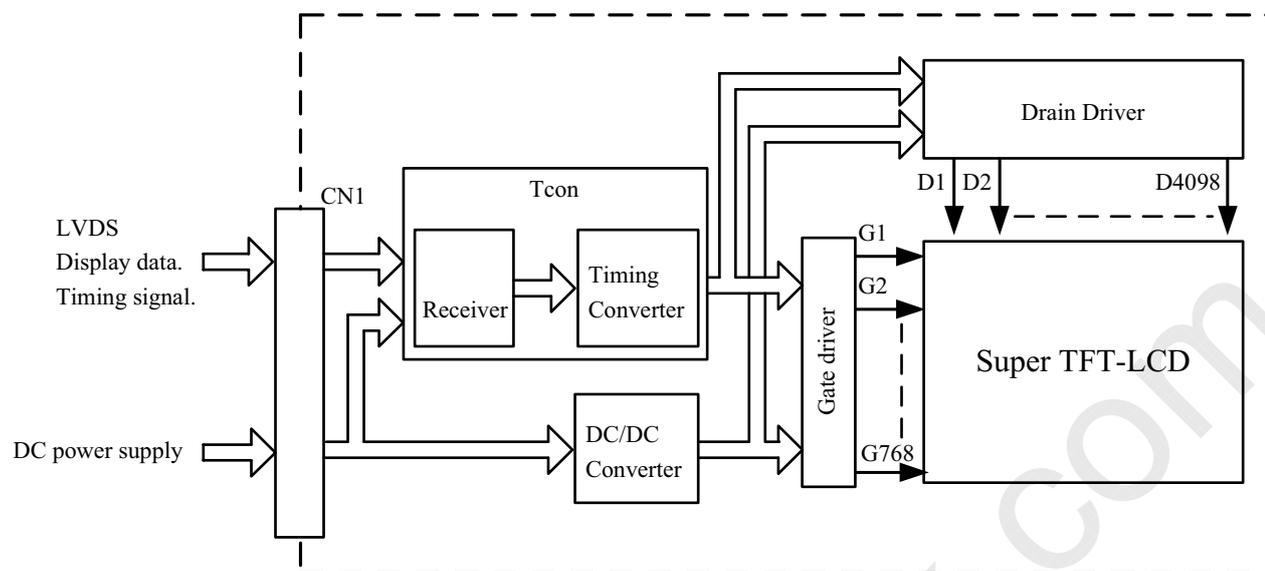
3.2 Back Light

ITEM	Symbol	VALUE			Unit	Notes
		Min	Typ	Max		
Input Voltage	VBL	21.6	24.0	26.4	V	
Input Current	IBL	—	2.84	3.4	A	$V_{in}=24.0\text{V}$, $BRT=3.15\text{V}$ 1)
ON/OFF Control Input Voltage	ON	2.0	—	5.5	V	
	OFF	-0.3	—	0.8	V	
Brightness Control Input Voltage	Min. Brightness	—	0	—	V	
	Max. Brightness	3.0	3.15	3.3	V	
PWM Duty	Min. Brightness	20	—	—	%	$V_{in}=24.0\text{V}$, $BRT=0\text{V}$
	Max. Brightness	—	—	100	%	$V_{in}=24.0\text{V}$, $BRT=3.15\text{V}$
Output current	IL	5.0	6.0	7.0	mArms	$V_{in}=24.0\text{V}$, $BRT=3.15\text{V}$
Open Output Voltage	V_{open}	1700	1800	1900	V_{rms}	
Output Frequency	fL	48	50	52	kHz	

- 1) This characteristics should be applied putting on the lamp about 30 minutes later with ambient temperature. ($T_a=25 \pm 2^{\circ}\text{C}$)

4. BLOCK DIAGRAM

(1) Super-TFT Module



5. INTERFACE PIN ASSIGNMENT

5.1 TFT-LCD MODULE

CN1 : HIROSE FX15S-41S-0.5SH

(Matching connector :HIROSE FX15S-41P-C)

Pin No.	Symbol	Description	Note
1	VDD	Power Supply (typ.+12V)	1)
2	VDD		
3	VDD		
4	VDD		
5	VDD		
6	VDD		
7	VSS	GND(0V)	2)
8	VSS		
9	VSS		
10	VSS		
11	VSS		
12	VSS		
13	Rx0-	Pixel Data	3)
14	Rx0+		
15	VSS	GND(0V)	2)
16	Rx1-	Pixel Data	3)
17	Rx1+		
18	VSS	GND(0V)	2)
19	Rx2-	Pixel Data	3)
20	Rx2+		
21	VSS	GND(0V)	2)
22	CLK-	Pixel Clock	3)
23	CLK+		
24	VSS	GND(0V)	2)
25	Rx3-	Pixel Clock	3)
26	Rx3+		
27	VSS	GND(0V)	2)
28	IC	Internally Connected , Keep Open	
29	IC	Internally Connected , Keep Open	
30	IC	Internally Connected , Keep Open	
31	IC	Internally Connected , Keep Open	
32	IC	Internally Connected , Keep Open	
33	IC	Internally Connected , Keep Open	
34	IC	Internally Connected , Keep Open	
35	IC	Internally Connected , Keep Open	
36	IC	Internally Connected , Keep Open	
37	IC	Internally Connected , Keep Open	
38	IC	Internally Connected , Keep Open	
39	IC	Internally Connected , Keep Open	
40	IC	Internally Connected , Keep Open	
41	IC	Internally Connected , Keep Open	

- Notes
- 1) All VDD pins shall be connected to +12.0V(Typ.).
 - 2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.
 - 3) Rx n+ and Rx n- (n=0,1,2,3) should be wired by twist-pairs or side-by-side FPC patterns, respectively.

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5.2 BACK-LIGHT UNIT**CN2 : JST S14B-PH-SM4-TB**

(Matching connector : JST PHR-14)

Pin No.	SYMBOL	Description	Note
1	VIN	Power supply(Typ. 24.0V)	1)
2	VIN		
3	VIN		
4	VIN		
5	VIN		
6	VSS	GND(0V)	2)
7	VSS		
8	VSS		
9	VSS		
10	VSS		
11	NC	NC	
12	ON/OFF	High:Lamp ON, Low:Lamp OFF	3)
13	BRT	High : Max. Brightness , Low : Min. Brightness	4)
14	NC	NC	

Notes 1) All VIN pins shall be connected to +24.0V(Typ.).

2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.

3) High level:2.2~5.5V, Low level:-0.3~0.8V

4) High level : 3.15V , Low level : 0V

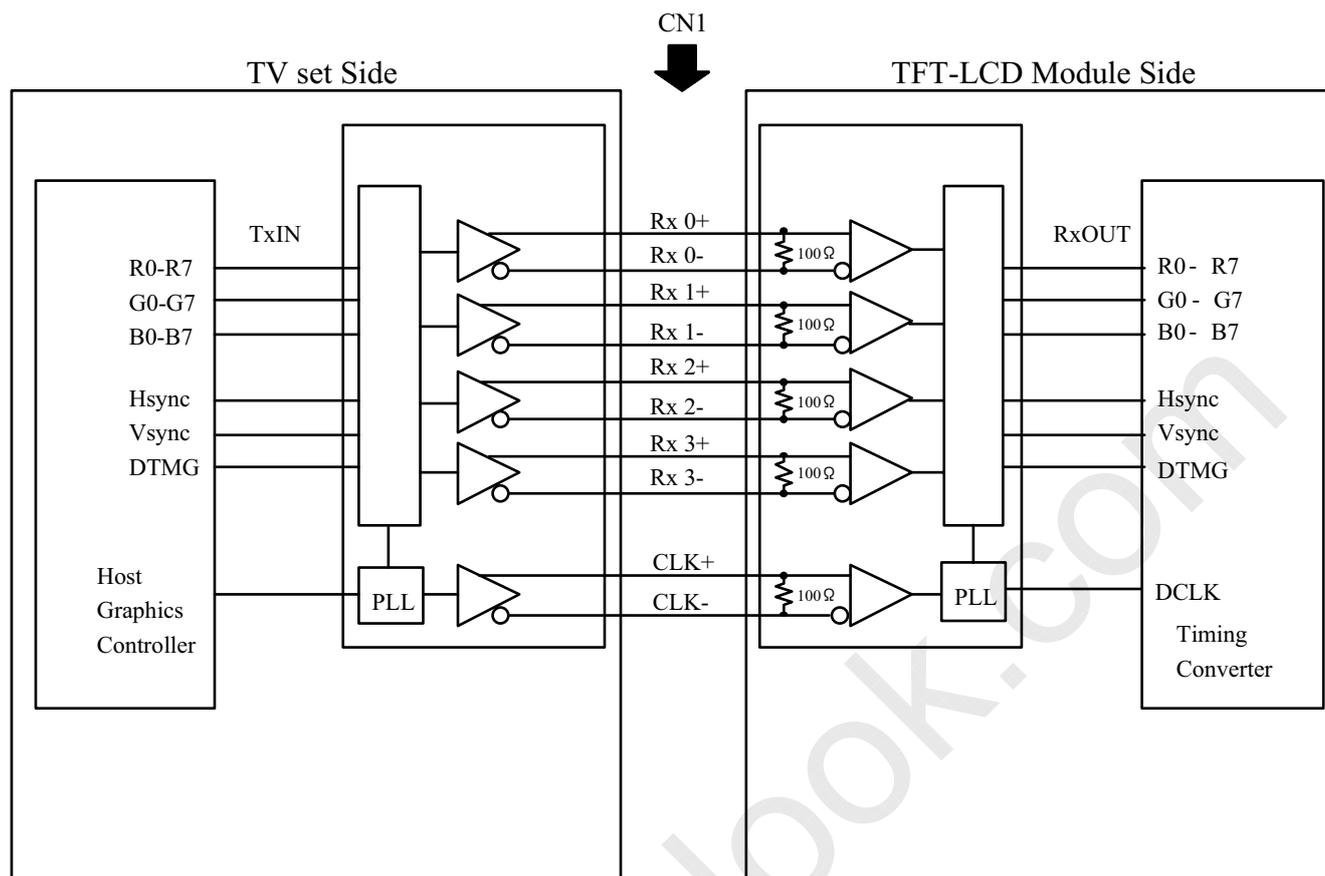
CN3 : JST S10B-PH-SM4-TB

(Matching connector : JST PHR-10)

Pin No.	SYMBOL	Description	Note
1	NC		1)
2	NC		
3	NC		
4	NC		
5	NC		
6	NC		
7	NC		
8	NC		
9	NC		
10	NC		

Note 1) CN3 is not used.

5.3 BLOCK DIAGRAM OF INTERFACE



R0~R7 : Pixel R Data
 G0~G7 : Pixel G Data
 B0~B7 : Pixel B Data
 HSYNC : Horizontal synchronization signal
 VSYNC : Vertical synchronization signal
 DTMG : Display timing signal

- Notes
- 1) The system must have the transmitter to drive the module.
 - 2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.4 LVDS INTERFACE

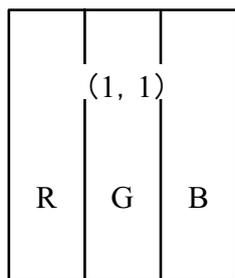
	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT		
		PIN	INPUT	PC	TFT-LCD	PIN	OUTPUT			
24bit	R2	51	Tx IN0	TA OUT0+	Rx 0+	27	Rx OUT0	R2		
	R3	52	Tx IN1			29	Rx OUT1	R3		
	R4	54	Tx IN2			30	Rx OUT2	R4		
	R5	55	Tx IN3			32	Rx OUT3	R5		
	R6	56	Tx IN4			33	Rx OUT4	R6		
	R7	3	Tx IN6			TA OUT0-	Rx 0-	35	Rx OUT6	R7
	G2	4	Tx IN7					37	Rx OUT7	G2
	G3	6	Tx IN8	38	Rx OUT8			G3		
	G4	7	Tx IN9	39	Rx OUT9			G4		
	G5	11	Tx IN12	TA OUT1+	Rx 1+			43	Rx OUT12	G5
	G6	12	Tx IN13					45	Rx OUT13	G6
	G7	14	Tx IN14					46	Rx OUT14	G7
	B2	15	Tx IN15			TA OUT1-	Rx 1-	47	Rx OUT15	B2
	B3	19	Tx IN18					51	Rx OUT18	B3
	B4	20	Tx IN19					53	Rx OUT19	B4
	B5	22	Tx IN20					TA OUT2+	Rx 2+	54
	B6	23	Tx IN21	55	Rx OUT21					B6
	B7	24	Tx IN22	1	Rx OUT22					B7
	HSYNC	27	Tx IN24	3	Rx OUT24					HSYNC
	VSYNC	28	Tx IN25	TA OUT2-	Rx 2-	5	Rx OUT25			VSYNC
	DTMG	30	Tx IN26			6	Rx OUT26			DTMG
	R0	50	Tx IN27			7	Rx OUT27			R0
	R1	2	Tx IN5			TA OUT3+	Rx 3+	34	Rx OUT5	R1
	G0	8	Tx IN10					41	Rx OUT10	G0
	G1	10	Tx IN11					42	Rx OUT11	G1
B0	16	Tx IN16	TA OUT3-					Rx 3-	49	Rx OUT16
B1	18	Tx IN17		50	Rx OUT17				B1	
RSVD 1)	25	Tx IN23		2	Rx OUT23				not connect	
DCLK	31	TxCLK IN		TxCLK OUT+	RxCLK IN+				26	RxCLK OUT
				TxCLK OUT-	RxCLK IN-					

R0~R7 : Pixel R Data (7;MSB, 0;LSB)
 G0~G7 : Pixel G Data (7;MSB, 0;LSB)
 B0~B7 : Pixel B Data (7;MSB, 0;LSB)
 HSYNC : Horizontal synchronization signal
 VSYNC : Vertical synchronization signal
 DTMG : Display timing signal

Notes 1) RSVD(reserved) pins on the transmitter shall be "H" or "L".

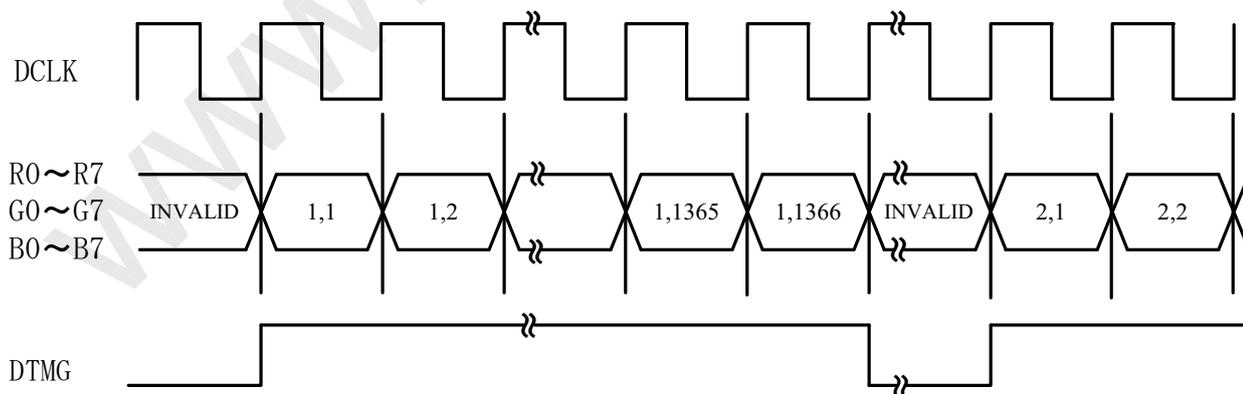
5.5 CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE

Display data of adjacent one pixel is latched during one cycle of DCLK.



pixel : R0~R7 :R data
 G0~G7 :G data
 B0~B7 :B data

1, 1	1, 2	1, 3	-----	1, 1366
2, 1	2, 2	2, 3	-----	2, 1366
3, 1	3, 2	3, 3	-----	3, 1366
768, 1	768, 2	768, 3	-----	768, 1366



5.6 RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color	Input	Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB				LSB				MSB				LSB				MSB				LSB			
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

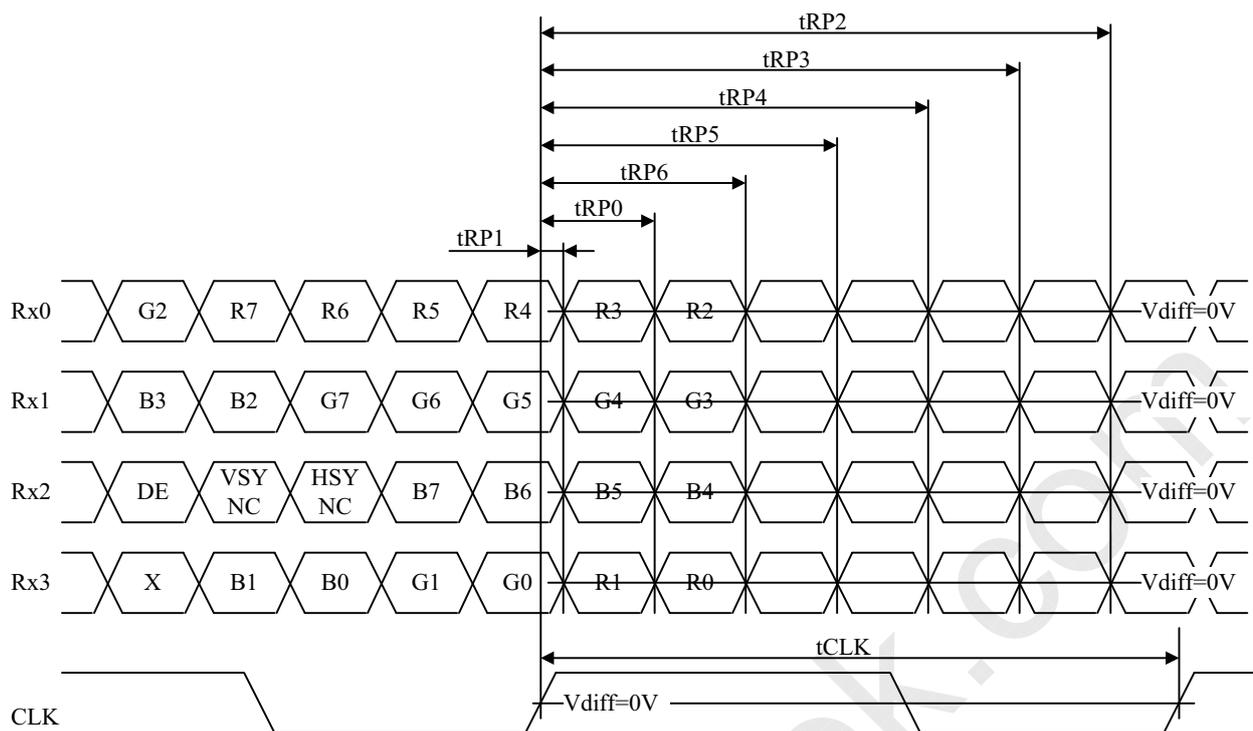
Notes 1) Definition of gray scale:

Color(n).....Number in parenthesis indicates gray scale level. Larger n corresponds to brighter level.

2) Data: 1:High, 0:Low

6. INTERFACE TIMING

6.1 LVDS RECEIVER TIMING



Rx0 = (Rx0+) - (Rx0-)

Rx1 = (Rx1+) - (Rx1-)

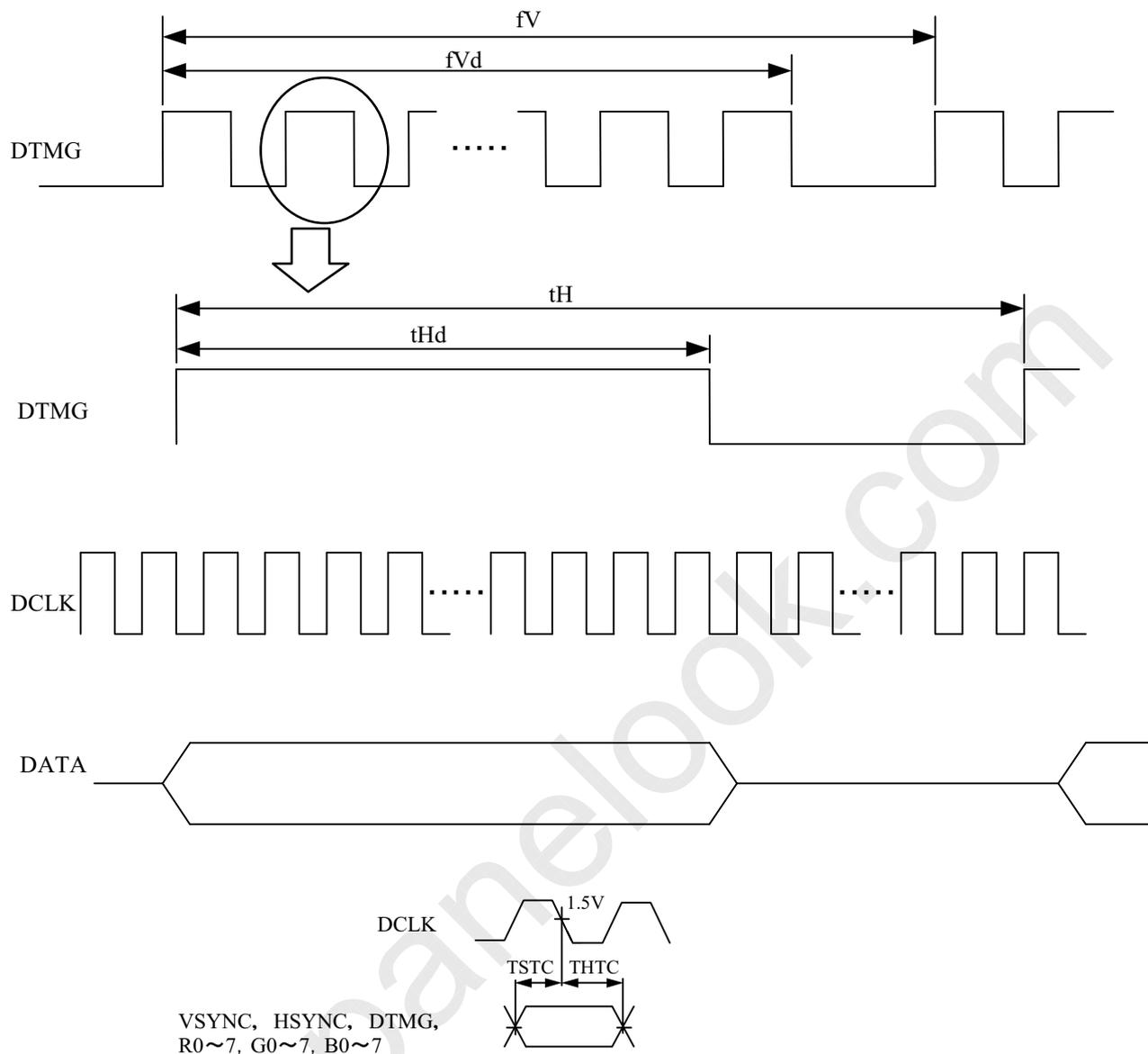
Rx2 = (Rx2+) - (Rx2-)

Rx3 = (Rx3+) - (Rx3-)

CLK = (CLK+) - (CLK-)

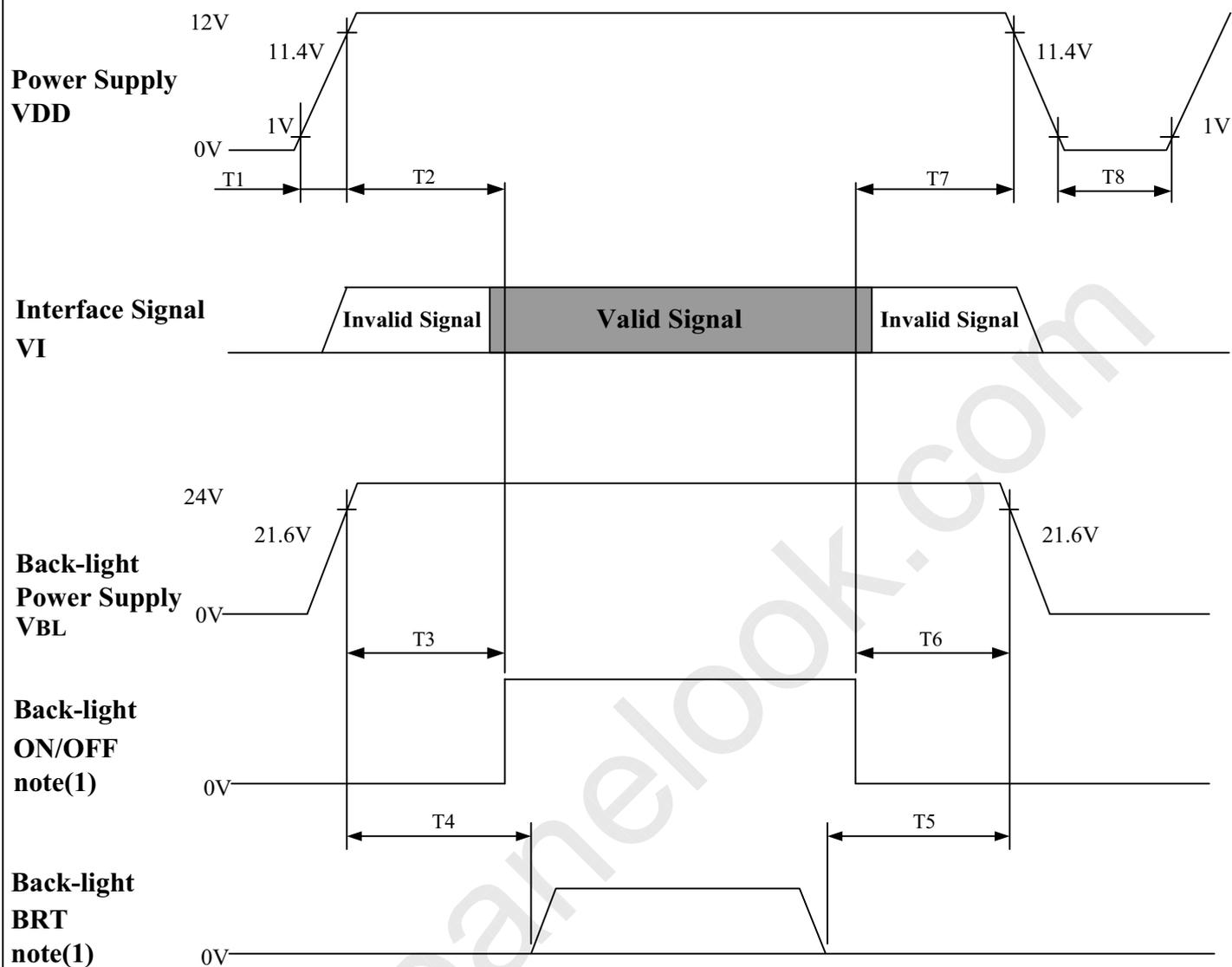
	Item	Symbol	Min.	Typ.	Max.	Unit
RCLK	Cycle Time	1/tCLK	65	66	68	MHz
Rx0 Rx1 Rx2 Rx3	0 data position	tRP0	1/7tCLK-0.41	1/7tCLK	1/7tCLK+0.41	ns
	1st data position	tRP1	-0.41	0	+0.41	
	2nd data position	tRP2	2/7tCLK-0.41	2/7tCLK	2/7tCLK+0.41	
	3rd data position	tRP3	3/7tCLK-0.41	3/7tCLK	3/7tCLK+0.41	
	4th data position	tRP4	4/7tCLK-0.41	4/7tCLK	4/7tCLK+0.41	
	5th data position	tRP5	5/7tCLK-0.41	5/7tCLK	5/7tCLK+0.41	
	6th data position	tRP6	6/7tCLK-0.41	6/7tCLK	6/7tCLK+0.41	

6.2 SYNCHRONIZATION SIGNAL TIMING



Item	Symbol	Min.	Typ.	Max.	Unit	Note
DE	Vertical Frequency	fV	57	60	63	Hz
	Vertical Period	tV	773	800	1500	tH
	Vertical Valid	tVd	768			tH
	Horizontal Frequency	fH	—	48	—	kHz
	Horizontal Period	tH	1400	1708	2000	tCLK
	Horizontal Valid	tHd	1366			tCLK

6.3 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



$$0 \leq T1 \leq 10$$

$$350 \leq T2$$

$$0 \leq T3$$

$$1 \leq T4$$

$$-100 \leq T5$$

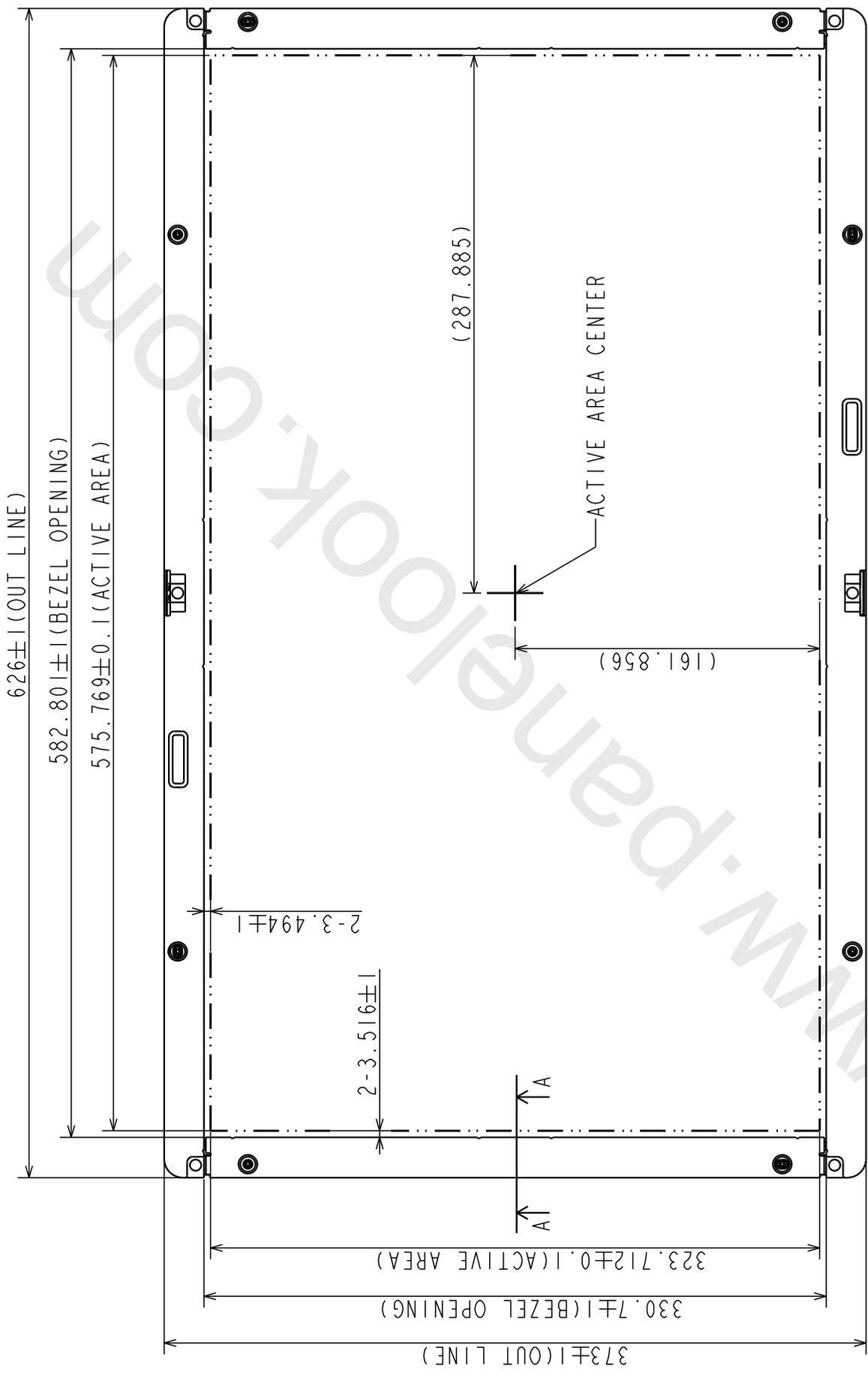
$$-100 \leq T6$$

$$0 \leq T7$$

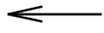
$$350 \leq T8$$

Unit : ms

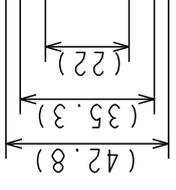
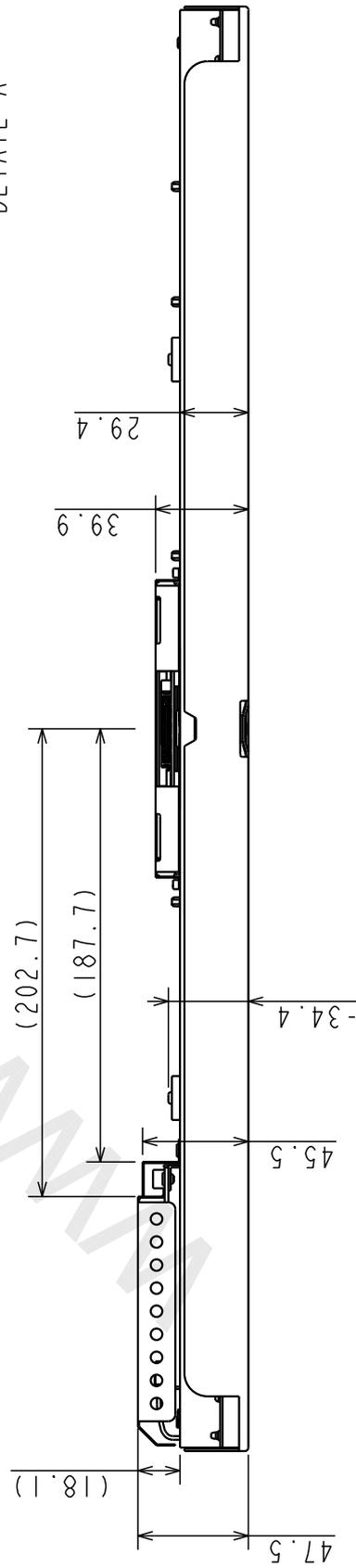
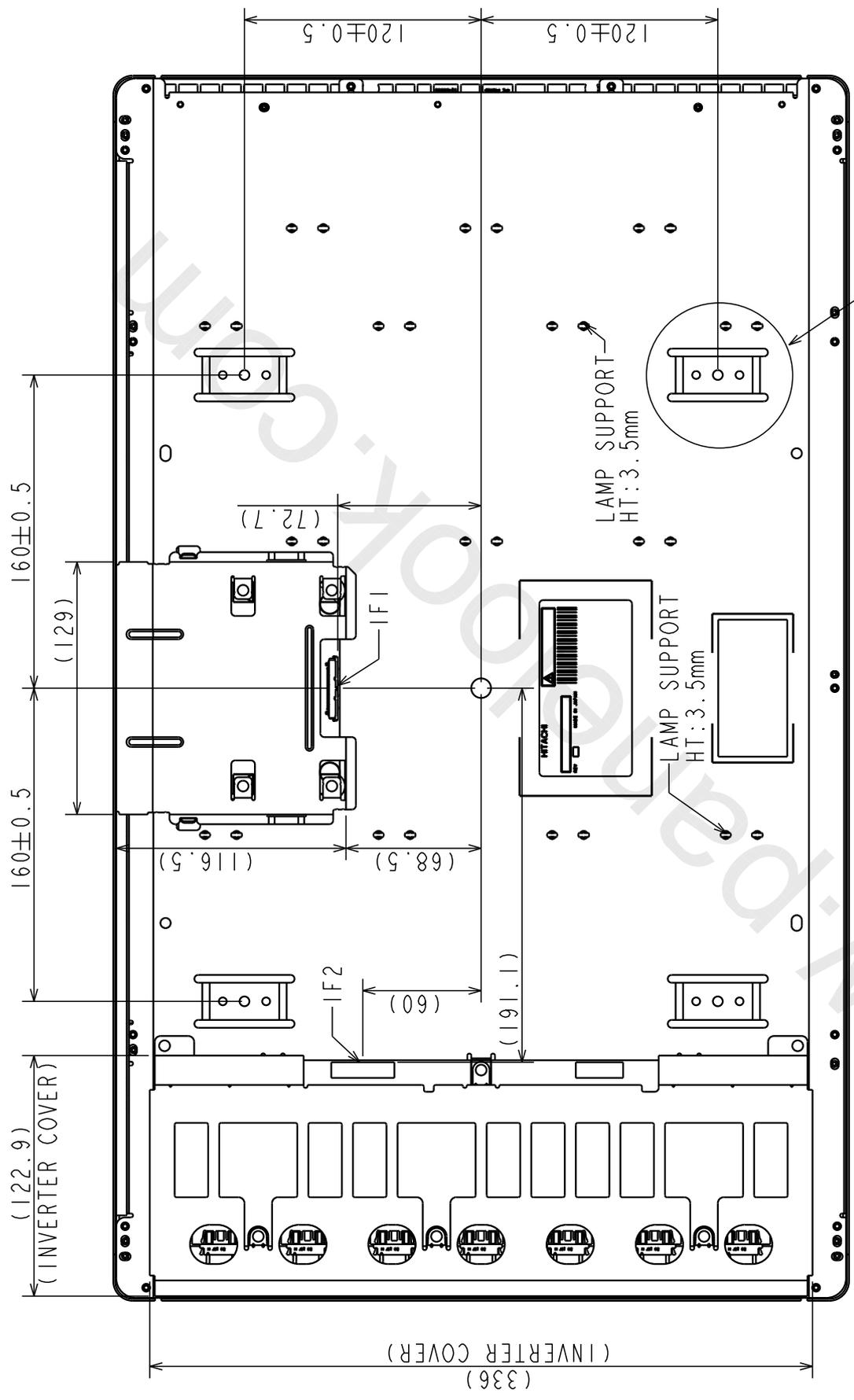
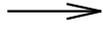
Note 1) In all periods, the backlight ON/OFF signal voltage and the BRT signal voltage should be lower than the backlight power supply voltage.



UPPER SID



LOWER SID



(119)

(122.9)
(INVERTER COVER)

160±0.5

160±0.5

(129)

(72.7)

(116.5)

(68.5)

IF2

(60)

(191.1)

(336)
(INVERTER COVER)

LAMP SUPPORT
HT: 3.5mm

LAMP SUPPORT
HT: 3.5mm

DETAIL A

(18.1)

47.5

45.5

34.4

39.9

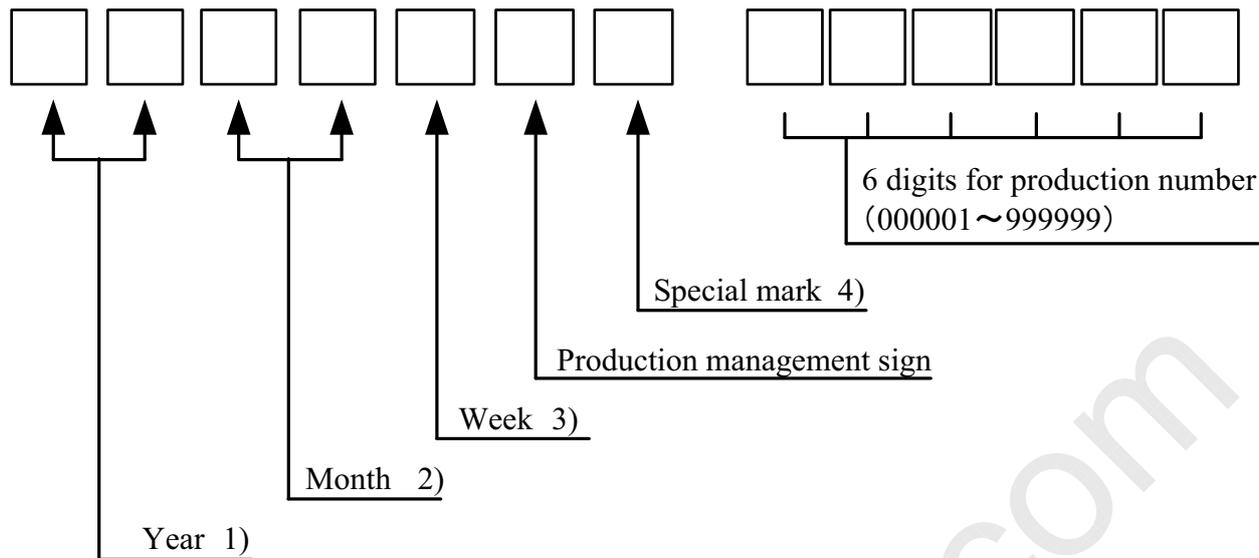
29.4

(202.7)

(187.7)

8. DESIGNATION OF LOT MARK

8.1 LOT MARK



Notes

1)

Year	Mark
2006	06
2007	07
2008	08

2)

Month	Mark	Month	Mark
1	01	7	07
2	02	8	08
3	03	9	09
4	04	10	10
5	05	11	11
6	06	12	12

3)

Week(Day)	Mark
1~7	1
8~14	2
15~21	3
22~28	4
29~31	5

4) It is the mark that was opened up by production person to take correspondence with production number.

8.2 Revision (REV.) control

REV. is the column for manufacturing convenience. A-Z except I and O may be written on this column.

8.3 Location of lot mark

Lot mark is printed on a label. The label is on the metallic bezel as shown in 7. External Dimensional. The style of character will be changed without notice.



9. PRECAUTION

Please pay attention to the followings when a Super-TFT module with a back-light unit is used, handled and mounted.

9.1 Precaution to handling and mounting

- (1) Applying strong force to a part of the module may cause partial deformation of frame or mold, and cause damage to the display.
- (2) The module should gently and firmly be held by both hands. Never hold by just one hand in order to avoid any internal damage. Never drop or hit the module.
- (3) The module should be installed with mounting holes of a module.
- (4) Uneven force such as twisted stress should not be applied to a module when a module is mounted on the cover case. The cover case must have sufficient strength so that external force can not be transmitted directly to a module.
- (5) It is recommended to leave a space between a module and a holding board of a module so that partial force is not applied to a module.

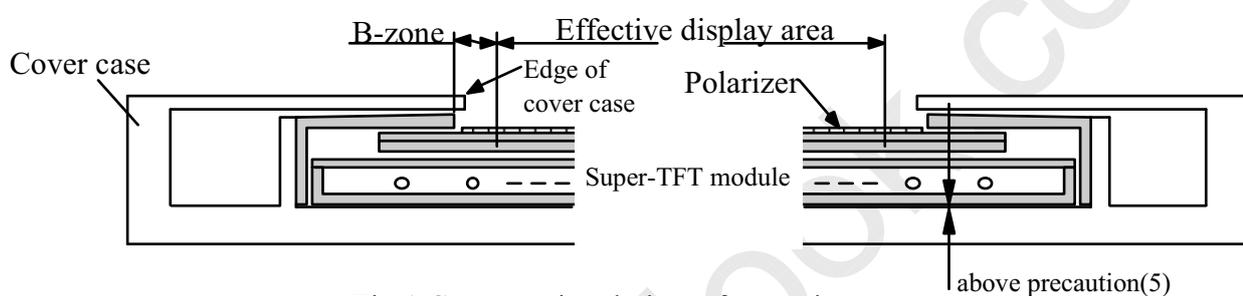


Fig.1 Cross sectional view of a monitor set

- (6) The edge of a cover case should be located inside more than 1mm from the edge of a module front frame.
- (7) A transparent protective plate should be added on the display area of a module in order to protect a polarizer and Super-TFT cell. The transparent protective plate should have sufficient strength so that the plate can not touch a module by external force.
- (8) Materials included acetic acid and choline should not be used for a cover case as well as other parts and boards near a module. Acetic acid attacks a polarizer. Choline attacks electric circuits due to electro-chemical reaction.
- (9) The polarizer on a TFT cell should carefully be handled due to its softness, and should not be touched, pushed or rubbed with glass, tweezers or anything harder than HB pencil lead. The surface of a polarizer should not be touched and rubbed with bare hand, greasy clothes or dusty clothes.
- (10) The surface of a polarizer should be gently wiped with absorbent cotton, chamois or other soft materials slightly contained petroleum benzene when the surface becomes dirty. Normal-hexane as cleaning chemicals is recommended in order to clean adhesives which fix front/rear polarizers on a Super-TFT cell. Other cleaning chemicals such as acetone, toluen and alcohol should not be used to clean adhesives because they cause chemical damage to a polarizer.
- (11) Saliva or water drops should be immediately wiped off. Otherwise, the portion of a polarizer may be deformed and its color may be faded.
- (12) The module should not be opened or modified. It may cause not to operate properly.

- (13) Metallic bezel of a module should not be handled with bare hand or dirty gloves. Otherwise, color of a metallic frame may become dirty during its storage. It is recommended to use clean soft gloves and clean finger stalls when a module is handled at incoming inspection process and production (assembly) process.
- (14) Lamp(CCFL) cables should not be pulled and held.

9.2 Precaution to operation

- (1) The ambient temperature near the operated module should be satisfied with the absolute maximum ratings. Unless it meets the specifications, sufficient cooling system should be adopted to system.
- (2) The spike noise causes the mis-operation of a module. The level of spike noise should be as follows:
-200mV<=over- and under- shoot of VDD<= +200mV
VDD including over- and under- shoot should be satisfied with the absolute maximum ratings.
- (3) Optical response time, luminance and chromaticity depend on the temperature of a Super-TFT module. Response time and saturation time of CCFL luminance become longer at lower temperature operation.
- (4) Sudden temperature change may cause dew on and/or in the a module. Dew males damage to a polarizer and/or electrical contacting portion. Dew causes fading of displayed quality.
- (5) Fixed patterns displayed on a module for a long time may cause after-image. It will be recovered soon.
- (6) A module has high frequency circuits. Sufficient suppression to electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be effective to minimize the interference.
- (7) Noise may be heard when a back-light is operated. If necessary, sufficient suppression should be done by system manufacturers.
- (8) The module should not be connected or removed while a main system works.
- (9) Inserting or pulling I/F connectors causes any trouble when power supply and signal dates are on-state.I/F connectors should be inserted and pulled after power supply and signal dates are turned off.

9.3 Electrostatic discharge control

- (1) Since a module consists of a Super-TFT cell and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharge, persons who are handling a module should be grounded through adequate methods such as a list band. I/F connector pins should not be touched directly with bare hands.
- (2) Protection film for a polarizer on a module should be slowly peeled off so that the electrostatic charge can be minimized.

9.4 Precaution to strong light exposure

- (1) A module should not be exposed under strong light. Otherwise, characteristics of a polarizer and color filter in a module may be degraded.

9.5 Precaution to storage

When modules for replacement are stored for a long time, following precautions should be taken care of:

- (1) Modules should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during storage. Modules should be stored at 0 to 35-C at normal humidity (60%RH or less).
- (2) The surface of polarizers should not come in contact with any other object. It is recommended that modules should be stored in the Hitachi's shipping box.

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9.6 Precaution to handling protection film

- (1) The protection film for polarizers should be peeled off slowly and carefully by persons who are electrically grounded with adequate methods such as a list band. Besides, ionized air should be blown over during peeling action. Dusts on a polarizer should be blown off by an ionized nitrogen gun and so on.
- (2) The protection film should be peeling off without rubbing it to the polarizer. Because, if the film is rubbed together with the polarizer, since the film is attached to the polarizer with a small amount of adhesive, the adhesive may remain on a polarizer.
- (3) The module with protection film should be stored on the conditions explained in 10.5 (1). However, in case that the storage time is too long, adhesive may remain on a polarizer even after a protection film is peeled off. Besides, in case that a module is stored at higher temperature and/or higher humidity, adhesive may remain on a polarizer. The remained adhesive may cause non-uniformity of display image.
- (4) The adhesive can be removed easily with Normal-Hexane. The remained adhesive or its vestige on the polarizer should be wiped off with absorbent cotton or other soft materials such as chamois slightly contained Normal-Hexane.

9.7 Safety

- (1) Since a Super-TFT cell and lamps are made of glass, handling to the broken module should be taken care sufficiently in order not to be injured. Hands touched liquid crystal from a broken cell should be washed sufficiently.
- (2) The module should not be taken apart during operation so that back-light drives by high voltage.

9.8 Environmental protection

- (1) The Super-TFT module contains cold cathode fluorescent lamps. Please follow local ordinance or regulations for its disposal.
- (2) Flexible printed circuits and printed circuits board used in a module contain small amount of lead. Please follow local ordinance or regulations for its disposal.

9.9 Use restrictions and limitations

- (1) This product is not authorized for use in life support devices or systems, military applications or other applications which pose a significant risk of personal injury.
- (2) In no event shall Hitachi, Ltd., be liable for any incidental, indirect or consequential damages in connection with the installation or use of this product, even if informed of the possibility thereof in advance. These limitations apply to all causes of action in the aggregate, including without limitation breach of contract, breach of warranty, negligence, strict liability, misrepresentation and other torts.

9.10 Others

- (1) Electrical components which may not affect electrical performance are subjective to change without notice because of their availability.

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