System on a Programmable Chip

Datasheet

Part Number：BM3109IB

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Introduction

Aiming on building the high-dynamic, high-performance, low-power--dissipation processing platform-SoPC (System on a Programmable Chip) development platform, which combines operating and controlling together, the BM3109IB based its design on the domestic devices and excellent IC design guarantees. Integrating the SoC hardware and FPGA system, the system implements the ability of dynamical-configuration and high-integration.

Meeting the requirements of high-density, intelligence and miniaturization of system, the platform can apply to the developing the multi-specification and small-batch products in the fields of aerospace and military application, which has wide applied future.

With the core of 32-bit RISC embedded microprocessor of SPARC V8 architecture, BM3109IB has rich peripheral interfaces, whole memories. A completely single-board system can be constituted when combined with related peripheral circuits.

The application of BM3109IB allows users to constitute on-board embedded real-time computer system flexibly, which satisfies various kinds of application and performance requirement of miniaturization for aerospace use and aviation use.

Features of BM3109IB：

High-performance CPU processor core: including integer-

processing unit, 64-bit Floating-point processing unit compatible with IEEE-754, independent Instruction Cache and Data Cache, hardware multiplier and divider, interrupt controller, hardware debug unit with trace buffer.

Built-in high-capacity FPGA: including 300K field-program mable gates, internal tri-state bus and the clock manager circuit. The operation frequency is up to 200MHz. Supporting 66-MHz PCI protocol and IEEE 1149.1 boundary-scan logic.

Built-in multilevel storage system: Built-in high-capacity flash (8MB) memory; SRAM (1MB) and SDRAM (16MB) for program running;

On-chip peripherals: 4 UARTS (2 with fifo), DSU hardware debug unit, 10 PWM outputs, 12 counters, 1553B bus(supporting BC/RT/MT), 16 GPIO outputs, 5 external interruption(supporting non-maskable), 4 A/D converters,7 switches for 4 A/D converters, 2 I^2C bus.

Friendly development environment: BM3109IB has a well environment constructed by abundant samples of software development, standard peripheral function library and multi-type IP soft core of FPGA for the users.

Features

Processing Unit

- 32-bit microprocessor of SPARC V8 architecture
- Maximum operating frequency up to 100 MHz
- 8-register window
- Internal 5 stage pipeline
- 16 Kbytes 2-way set-associative Data Cache
- 32 Kbytes 4-way set-associative Instruction Cache
- Floating point unit (FPU) Supporting single and double- precision floating-point data types
- Supporting high-speed on-chip AMBA bus

High-speed, high-density programmable logic

- 300K gates
  - Operating Frequency up to 200 MHz
  - Multi-standard Select IO™ interfaces
  - 16 kinds of high-performance interface standards
  - Associated with ZBTRAM devices directly
- Internal Clock Manager Circuit
  - 4 dedicated delay-locked loops (DLLs) for advanced clock control
  - 4 primary low-skew global clock distribution nets, plus 24 secondary local clock nets

- Memories
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-port RAM, or 16-bit shift register
  - Configurable synchronous dual-port RAMs
  - High-speed interfaces attachable to external high-performance RAMs
- Flexible structure that can balance speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Supporting dedicated multiplier
  - Cascade chain for multi-input functions
- Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
- Internal tri-state bus
- Supporting IEEE 1149.1 boundary-scan logic
- Supporting system programming based on SRAM
  - Infinite ability to be repeat programmed
  - 4 programming modes

Memories

- Up to 8 Mbytes of Flash memory
- Up to 1 Mbytes of SRAM
- Up to 16 Mbytes of SDRAM

On-chip peripheral

- 4 serial communication interfaces, 2 of them with FIFO
- DSU for hardware debug
- 10 PWM outputs
- 12 counters
- 1 high-speed 1553B bus
- 16 general I/O interfaces
- 5 interrupt controllers of external programmable input-interfaces (supporting non-maskable)
- 4 ADC converters
- 7 analog switches for 4 ADC converters
- 2 I^2C bus

Friendly Development environment

Features are given as follow：

- Supporting operating systems:μc-Linux
- Abundant samples for system development: Including system analysis, division of software and hardware units, design of software and hardware and system tests.
- Multi-type software function library of peripherals: The functions Includes UART, Counter, Timer, I^2C, Interrupt and so on.
- Multi-type IP library of FPGA: Including UART, I^2C, memory controlling interfaces and so on.

SoPC Features

- Debug Test: A hardware debug support unit, with 4 hardware observation points, to aid software debugging on target hardware.
- Operating Voltage:
  - 3.3 V ±0.33 V for I/O
  - 1.8 V ±0.18 V for Core
  - 2.5 V ±0.25 V for FPGA
- Operating Temperature: -40～+85 ℃
- Operating Frequency: 1 MHz～100 MHz
- Power Consumption:
  - 2.3W @100MHz
  - Normal/Low-power Mode
- Development Tools
  - BM3109 evaluation board
  - Integrated development environment (IDE)
- packaging: BGA 415
- The frame structure is as shown in the figure 1-1:

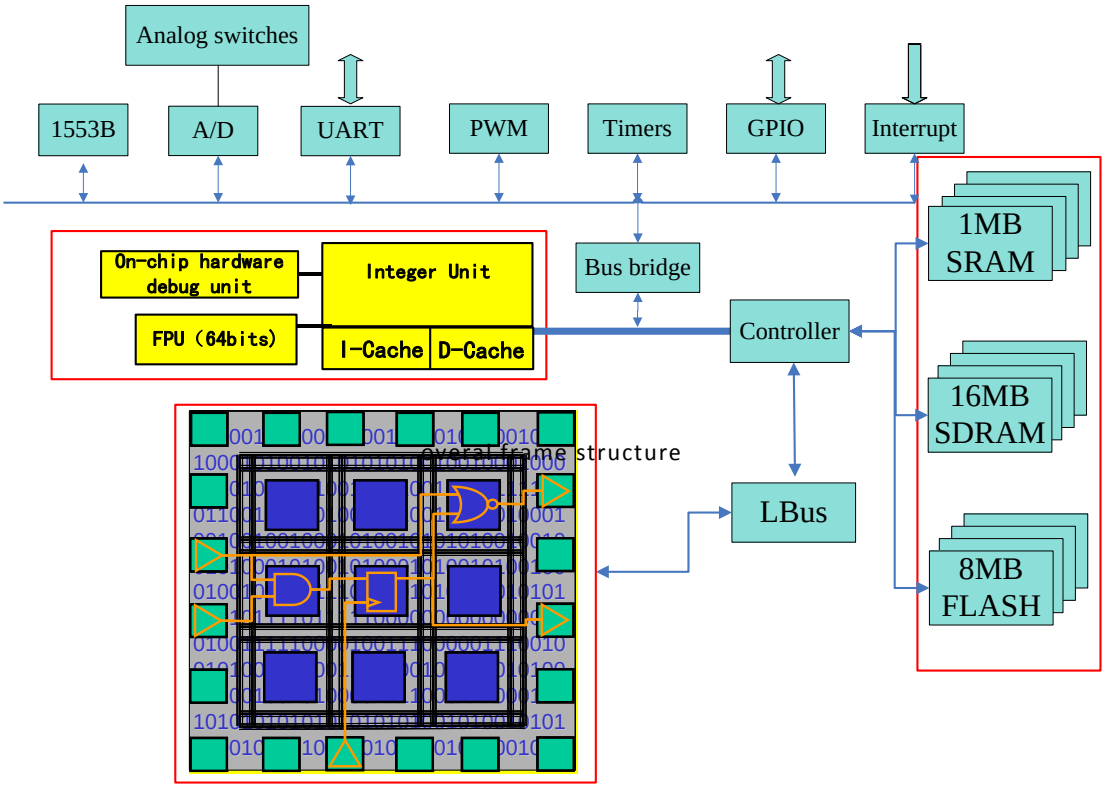

Figure 1-1 Overal Frame Structure

Service and Support：

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