Ver 1.0

SpaceWire Controller

Datasheet

Part Number：BM4802AMQRH

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Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2018.3.7			

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1. Features

- Three bidirectional SpaceWire channels
- Communication Memory Interface(COMI) autonomous accesses to a communication memory
- Host Control Interface(HOCI) gives read/write accesses to the configuration registers
  gives read/write accesses to the SpaceWire channels
- Compliant with SpaceWire ECSS-E-50-12A / ECSS-E-ST-50-12C
- Three bidirectional SpaceWire links
- Full duplex communication
- Data rate from 2Mbit/s up to 200Mbit/s in each direction
- Scalable data bus width 8/16/32bit width available
- Allow Little endian and Big endian configuration
- Clock frequencies: 10MHz/25MHz
- Operating range
  Voltage: 3.3V(IO) 1.8V(core)
  Temperature: -55℃ to 125℃
- Maximum power consumption : 1.0W
- Radiation Performance
  Total ionizing dose：
  ≥100Krad（Si）
  Single event latch-up threshold：
  ≥75MeV·cm^2/mg
  Single event upset threshold：
  ≥15MeV cm^2/mg
- Package:196 pins CQFP

2. General Description

BM4802AMQRH is a SpaceWire controller. It provides an interface between 3 SpaceWire links according to the SpaceWire Standard ECSS-E-50-12A /ECSS-E-ST-50-12C specification and a data processing node consisting of a CPU and a communication data memory. The SpaceWire controller provides HW supported execution of the major parts of the simple interprocessor communication protocol, particularly:

• Transfer of data between two nodes of a multi-processor system with minimal host CPU intervention.

• Execution of simple commands to provide basic features for system control functions.

• Provision of fault tolerant features.

The applications are heterogeneous multi-processor systems supported by scalable interfaces. The SpaceWire controller connects modules with different processors. Any kind of network topology could be realized through the high speed point-to-point SpaceWire-links.

3. Function Block Diagram

A block diagram of BM4802AMQRH is given in Figure 3-1.

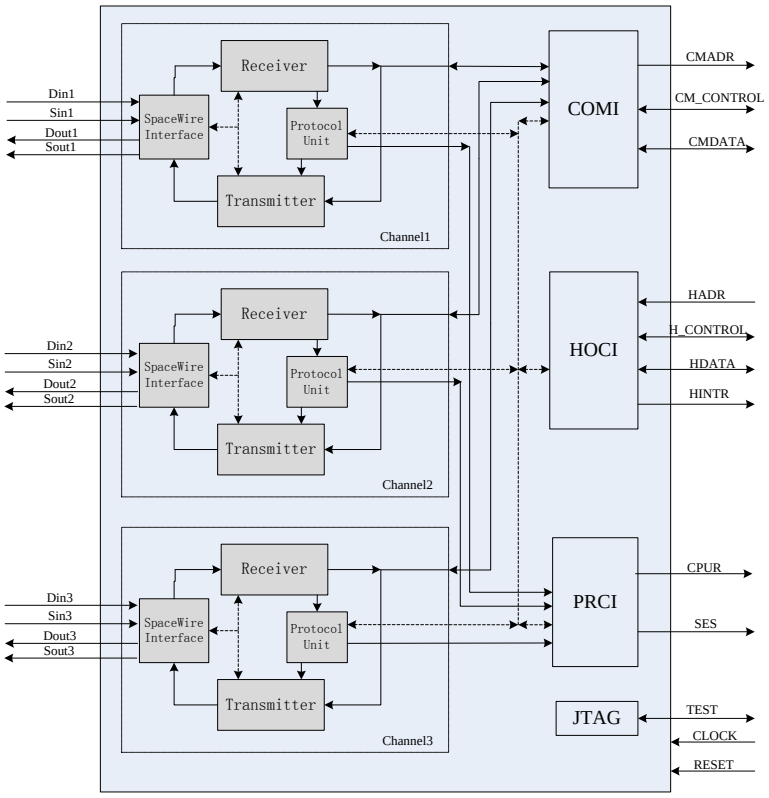
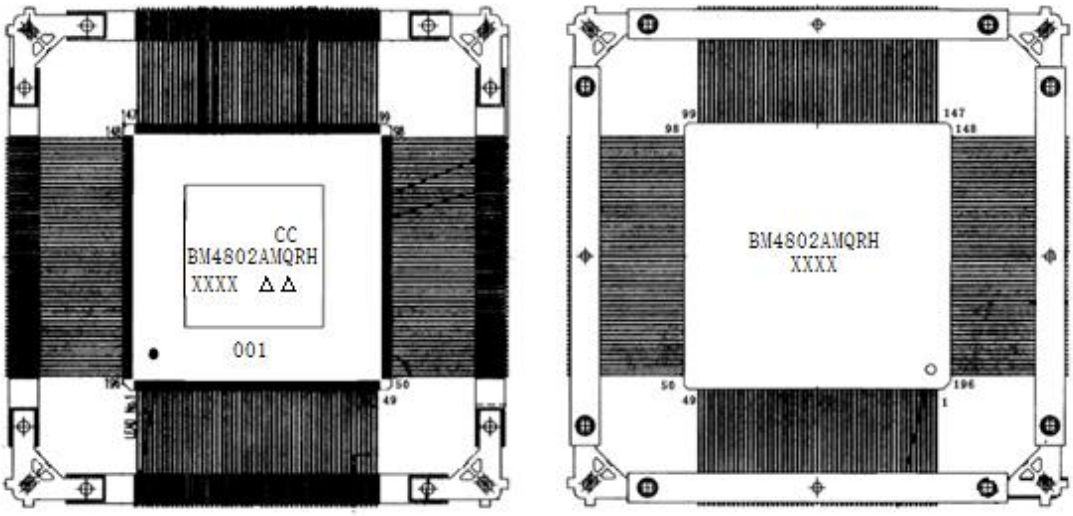


Figure 3-1 SpaceWire controller block diagram

4. Packages and Pin Function Descriptions

The provided package is: CQFP196.

BM4802AMQRH CQFP196 pin configuration is shown in 4-1.



Topside View **Underside View**

Figure 4-1 CQFP196 pin configuration

Talble 4-1 BM4802AMQRH CQFP196 Pin Function Descriptions

Signal name	Type	Function	max. output current [mA]	load [pF]
HSELN	I	Select host interface		
HRDN	I	host interface read strobe		
HWRN	I	host interface write strobe		
HADR(7:0)	I	the SpaceWire controller register address lines. This address lines will be used to access (address) the the SpaceWire controller registers.		
HDATA(31:0)	I/O/Z	the SpaceWire controller data	3	50
HACK	O/Z	host acknowledge.The SpaceWire controller deasserts this output to add wait states to a the SpaceWire controller access. After the SpaceWire controller is ready this output will be asserted.	3	50
HINTRN	O	host interrupt request line	3	50
CADR(3:0)	I	The SpaceWire controller Address. The binary value of this lines will		

		be compared with the value of the the SpaceWire controller ID lines.		
CID(3:0)	I	The SpaceWire controller ID lines: offers possibility to use sixteen the SpaceWire controller within one HSEL*		
HOSTBIGE	I	0: host I/F Little Endian 1: host I/F Big Endian		
BOOTLINK	I	0: control by host 1: control by link		
CMCS(1:0)	O/Z	Communication memory select lines. These pins are asserted as chip selects for the corresponding banks of the communication memory.	6	25
CMRDN	O/Z	Communication memory read strobe. This pin is asserted when the SpaceWire controller reads data from memory.	6	25
CMWRN	O/Z	Communication memory write strobe. This pin is asserted when the SpaceWire controller writes to data memory.	6	25
CMADR(15:0)	O/Z	Communication memory address. The SpaceWire controller outputs an address on these pins.	6	25
CMDATA(31:0)	I/O/Z	Communication memory data. The SpaceWire controller inputs and outputs data from and to com. memory on these pins.	3	25
COCI	I	Communication interface 'occupied' input signal	3	50
COCO	O	Communication interface 'occupied' output signal		
CAM	I	Communication interface arbitration master input signal 1: master 0: slave		
CPURN	O	CPU Reset Signal (can be used as user defined flag)	3	50
SESN(3:0)	O	Specific External Signals (can be	3	50

		used as user defined flags)		
LDI1	I	Link Data Input channel 1		
LSI1	I	Link Strobe Input channel 1		
LDO1	O	Link Data Output channel 1	12	25
LSO1	O	Link Strobe Output channel 1	12	25
LDI2	I	Link Data Input channel 2	25	
LSI2	I	Link Strobe Input channel 2		
LDO2	O	Link Data Output channel 2	12	25
LSO2	O	Link Strobe Output channel 2	12	25
LDI3	I	Link Data Input channel 3		
LSI3	I	Link Strobe Input channel 3		
LDO3	O	Link Data Output channel 3	12	25
LSO3	O	Link Strobe Output channel 3	12	25
TRSTN	I	Test Reset. Resets the test state machine.		
TCK	I	Test Clock. Provides an asynchronous clock for JTAG boundary scan.		
TMS	I	Test Mode Select. Used to control the test state machine.		
TDI	I	Test Data Input. Provides serial data for the boundary scan logic.		
TDO	O	Test Data Output. Serial scan output of the boundary scan path.	3	50
RESETN	I	The SpaceWire controller Reset. Sets the the SpaceWire controller to a known state. This input must be asserted (low) at power-up. The minimum width of RESET low is 5 cycles of CLK10 in parallel with CLK running.		
CLK_HOST	I	External clock input to the SpaceWire controller (max. 25 MHz).		
CLK10	I	External clock input to the SpaceWire controller DS-links		

		(application specific, nominal 10 MHz). Used to generate to transmission speed and link disconnect timeout.		
TIME_CODE	I	falling edge on this signal sends (if enabled) the internal SpaceWire time code value over the links.		
PLLOUT	O	Output of internal PLL.		

5. Pin List

BM4802AMQRH CQFP196 pin list is shown in table 5-1.

Table 5-1 BM4802AMQRH CQFP196 pin list

Pin number	Signal symbol	Pin type	Functional description
1	NC		—
2	NC		—
3	V_{DDA33}	power supply	3.3V power supply
4	CLK_HOST	I	Clock input for HOCI and COMI 25MHz
5	RESETN	I	Reset signal
6	CLK10	I	External input clock 10MHz
7	HOSTBIGE	I	Choose big endian or little endian signal
8	TCK	I	Test clock
9	TMS	I	Choose test mode signal
10	TDI	I	Test data input signal
11	TRSTN	I	Test reset signal
12	TDO	O	Test data output signal
13	V_{DDD33}	power supply	IO power —power (3.3V)
14	V_{SSD33}	ground	IO power—ground(3.3V)
15	HSELN	I	Choose host interface signal
16	HRDN	I	Host interface read signal
17	HWRN	I	Host interface write signal
18	HACK	O	Host ACK signal
19	HINTRN	O	Host interrupt signal
20	V_{DDD18}	power supply	Core power —power (1.8V)
21	V_{SSD18}	ground	Core power—ground(1.8V)

22	HADR(0)	I	Register address signal
23	HADR(1)	I	Register address signal
24	HADR(2)	I	Register address signal
25	HADR(3)	I	Register address signal
26	HADR(4)	I	Register address signal
27	HADR(5)	I	Register address signal
28	HADR(6)	I	Register address signal
29	HADR(7)	I	Register address signal
30	V_{DDD33}	power supply	IO power —power (3.3V)
31	V_{SSD33}	ground	IO power—ground(3.3V)
32	BOOTLINK	I	Host/link control signal
33	CADR(0)	I	Address signal comparison with circuit identifier
34	CADR(1)	I	Address signal comparison with circuit identifier
35	CADR(2)	I	Address signal comparison with circuit identifier
36	CADR(3)	I	Address signal comparison with circuit identifier
37	CID(0)	I	circuit identifier signal
38	CID (1)	I	circuit identifier signal
39	CID (2)	I	circuit identifier signal
40	CID (3)	I	circuit identifier signal
41	V_{DDD18}	power supply	Core power —power (1.8V)
42	V_{SSD18}	ground	Core power—ground(1.8V)
43	HDATA(0)	I/O	Host interface data signal(low bit)
44	HDATA(1)	I/O	Host interface data signal
45	HDATA(2)	I/O	Host interface data signal
46	HDATA(3)	I/O	Host interface data signal
47	HDATA(4)	I/O	Host interface data signal
48	HDATA(5)	I/O	Host interface data signal
49	HDATA(6)	I/O	Host interface data signal
50	V_{DDD33}	power supply	IO power —power (3.3V)
51	V_{SSD33}	ground	IO power—ground(3.3V)
52	HDATA(7)	I/O	Host interface data signal
53	HDATA(8)	I/O	Host interface data signal
54	HDATA(9)	I/O	Host interface data signal

55	HDATA(10)	I/O	Host interface data signal
56	HDATA(11)	I/O	Host interface data signal
57	V_{DDD18}	power supply	Core power —power (1.8V)
58	V_{SSD18}	ground	Core power—ground(1.8V)
59	HDATA(12)	I/O	Host interface data signal
60	HDATA(13)	I/O	Host interface data signal
61	HDATA(14)	I/O	Host interface data signal
62	HDATA(15)	I/O	Host interface data signal
63	HDATA(16)	I/O	Host interface data signal
64	HDATA(17)	I/O	Host interface data signal
65	V_{DDD33}	power supply	IO power —power (3.3V)
66	V_{SSD33}	ground	IO power—ground(3.3V)
67	HDATA(18)	I/O	Host interface data signal
68	HDATA(19)	I/O	Host interface data signal
69	HDATA(20)	I/O	Host interface data signal
70	HDATA(21)	I/O	Host interface data signal
71	HDATA(22)	I/O	Host interface data signal
72	HDATA(23)	I/O	Host interface data signal
73	V_{DDD18}	power supply	Core power —power (1.8V)
74	V_{SSD18}	ground	Core power—ground(1.8V)
75	HDATA(24)	I/O	Host interface data signal
76	HDATA(25)	I/O	Host interface data signal
77	HDATA(26)	I/O	Host interface data signal
78	V_{DDD33}	power supply	IO power —power (3.3V)
79	V_{SSD33}	ground	IO power—ground(3.3V)
80	HDATA(27)	I/O	Host interface data signal
81	HDATA(28)	I/O	Host interface data signal
82	HDATA(29)	I/O	Host interface data signal
83	V_{DDD18}	power supply	Core power —power (1.8V)
84	V_{SSD18}	ground	Core power—ground(1.8V)
85	HDATA(30)	I/O	Host interface data signal
86	HDATA(31)	I/O	Host interface data signal(high bit)
87	CPURN	O	CPU reset signal
88	SESN(0)	O	External special signal

89	SESN(1)	O	External special signal
90	SESN(2)	O	External special signal
91	SESN(3)	O	External special signal
92	CAM	I	COMI master/slaver arbitration signal
93	COCI	I	COMI arbitration input signal
94	COCO	O	COMI arbitration output signal
95	CMCS(0)	O	Spw controller Bank choose signal
96	CMCS(1)	O	Spw controller Bank choose signal
97	V_{DDD33}	power supply	IO power —power (3.3V)
98	V_{SSD33}	ground	IO power—ground(3.3V)
99	CMRDN	O	Spw controller read signal
100	CMWRN	O	Spw controller write signal
101	CMADR(0)	O	Spw controller address signal(low bit)
102	CMADR(1)	O	Spw controller address signal
103	CMADR(2)	O	Spw controller address signal
104	CMADR(3)	O	Spw controller address signal
105	CMADR(4)	O	Spw controller address signal
106	V_{DDD18}	power supply	Core power —power (1.8V)
107	V_{SSD18}	ground	Core power—ground(1.8V)
108	CMADR(5)	O	Spw controller address signal
109	CMADR(6)	O	Spw controller address signal
110	CMADR(7)	O	Spw controller address signal
111	CMADR(8)	O	Spw controller address signal
112	CMADR(9)	O	Spw controller address signal
113	CMADR(10)	O	Spw controller address signal
114	CMADR(11)	O	Spw controller address signal
115	V_{DDD33}	power supply	IO power —power (3.3V)
116	V_{SSD33}	ground	IO power—ground(3.3V)
117	CMADR(12)	O	Spw controller address signal
118	CMADR(13)	O	Spw controller address signal
119	CMADR(14)	O	Spw controller address signal
120	CMADR(15)	O	Spw controller address signal(high bit)
121	CMDATA(0)	I/O	Spw controller data signal(low bit)
122	CMDATA(1)	I/O	Spw controller data signal
123	CMDATA(2)	I/O	Spw controller data signal
124	V_{DDD18}	power	Core power —power (1.8V)

		supply	
125	V_{SSD18}	ground	Core power—ground(1.8V)
126	CMDATA(3)	I/O	Spw controller data signal
127	CMDATA(4)	I/O	Spw controller data signal
128	CMDATA(5)	I/O	Spw controller data signal
129	V_{DDD33}	power supply	IO power —power (3.3V)
130	V_{SSD33}	ground	IO power—ground(3.3V)
131	CMDATA(6)	I/O	Spw controller data signal
132	CMDATA(7)	I/O	Spw controller data signal
133	CMDATA(8)	I/O	Spw controller data signal
134	V_{DDD33}	power supply	IO power —power (3.3V)
135	V_{SSD33}	ground	IO power—ground(3.3V)
136	CMDATA(9)	I/O	Spw controller data signal
137	CMDATA(10)	I/O	Spw controller data signal
138	CMDATA(11)	I/O	Spw controller data signal
139	CMDATA(12)	I/O	Spw controller data signal
140	CMDATA(13)	I/O	Spw controller data signal
141	CMDATA(14)	I/O	Spw controller data signal
142	V_{DDD18}	power supply	Core power —power (1.8V)
143	V_{SSD18}	ground	Core power—ground(1.8V)
144	CMDATA(15)	I/O	Spw controller data signal
145	CMDATA(16)	I/O	Spw controller data signal
146	CMDATA(17)	I/O	Spw controller data signal
147	CMDATA(18)	I/O	Spw controller data signal
148	CMDATA(19)	I/O	Spw controller data signal
149	CMDATA(20)	I/O	Spw controller data signal
150	V_{DDD33}	power supply	IO power —power (3.3V)
151	V_{SSD33}	ground	IO power—ground(3.3V)
152	CMDATA(21)	I/O	Spw controller data signal
153	CMDATA(22)	I/O	Spw controller data signal
154	CMDATA(23)	I/O	Spw controller data signal
155	V_{DDD33}	power supply	IO power —power (3.3V)
156	V_{SSD33}	ground	IO power—ground(3.3V)
157	CMDATA(24)	I/O	Spw controller data signal

158	CMDATA(25)	I/O	Spw controller data signal
159	CMDATA(26)	I/O	Spw controller data signal
160	V_{DDD18}	power supply	Core power —power (1.8V)
161	V_{SSD18}	ground	Core power—ground(1.8V)
162	CMDATA(27)	I/O	Spw controller data signal
163	CMDATA(28)	I/O	Spw controller data signal
164	CMDATA(29)	I/O	Spw controller data signal
165	CMDATA(30)	I/O	Spw controller data signal
166	CMDATA(31)	I/O	Spw controller data signal(high bit)
167	V_{SSD33}	ground	IO power —power (3.3V)
168	V_{SSD33}	ground	IO power—ground(3.3V)
169	TST_CLK	I	Scan clock
170	SCAN_MODE	I	Scan mode
171	V_{SSD33}	ground	IO power —power (3.3V)
172	V_{DDD33}	power supply	IO power—ground(3.3V)
173	scan_enable	I	Scan enable
174	GK		Connect with lid
175	NC		—
176	LDI1	I	Link1 data input singal
177	LSI1	I	Link1 data input singal
178	LDO1	O	Link1 data output singal
179	LSO1	O	Link1 data output singal
180	LDI2	I	Link2 data input singal
181	LSI2	I	Link2 data input singal
182	PLL_TOUT	O	PLL output clock
183	V_{DDD33}	power supply	IO power —power (3.3V)
184	V_{DDD33}	power supply	IO power—ground(3.3V)
185	V_{DDD18}	power supply	Core power —power (1.8V)
186	LDO2	O	Link2 data output singal
187	LSO2	O	Link2 data output singal
188	LDI3	I	Link3 data input singal
189	LSI3	I	Link3 data input singal
190	LDO3	O	Link3 data output singal
191	LSO3	O	Link3 data output singal

192	TIME_CODE	I	Time code send control signal
193	PLL_BP	I	Time bypass selection signal
194	V_{SSA18}	ground	Core power —power (1.8V)
195	V_{DDA18}	power supply	Core power—ground(1.8V)
196	V_{SSA33}	ground	PLL IO power—ground(3.3V)

6. Detailed Description

6.1 Function Description

The main functions of BM4802AMQRH are as follows:

1) Configure function

CPU configures SpaceWire controller write register through HOCI interface, and check the status right or wrong through SpaceWire controller read register. This function can be used to initialize the SpaceWire controller, configure the transmission rate and set the mode.

2) Transparent mode

CPU sends data to SpaceWire controller link channel or receive data from SpaceWire controller link channel through HOCI interface. HOCI interface supports big endian and little endian. Data width supports 8bits, 16bits and 32bits. When CPU configures the start address and the end address of COMI transmission, DPRAM can automatically send data on the address range. COMI interface supports big endian and little endian. Data width supports 8bits, 16bits and 32bits. COMI can be used to complete efficient transmission of a large number of data.

3) Routing mode data forwarding mode

SpaceWire controller implements routing function when CPU is configured to enable routing and routing addresses. The data head is judged in the data link channel, and the routing channel is selected to realize the forwarding of the data package.

4) Remote memory access protocol mode

In this mode, SpaceWire controller is used as a controlled node. The read and write register do not need local CPU. One of 3 links is used as the control link, and the main control node is used to configure and control register read/write and data transmission. The access register does not trough HOCI interface, its 32bit data bus can be used as GPIO port, and the direction of each bit (in /out) can be set

independently.

5) Simple interprocessor communication protocol mode

This mode can be used for simple/complex instruction interpretation, response, error reporting, transmission and testing. Base on this protocol, data characters and simple system control commands can be passed between nodes in a multiprocessor system.

6.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 10℃～30℃ and relative humidity less than 70%. There should be no acid , alkali or other radiant gas in the environment,

6.3 Absolute Maximum Ratings

a) Core supply voltage range to ground potential（V_{DDD33}、V_{DDA33}）：-0.3V ～ 2.0V
b) IO supply voltage range to ground potential（V_{DDD18}、V_{DDA18}）：-0.3V ～ 3.8V
c) Storage temperature（T_{stg}）：-65℃～ 150℃
d) Power dissipation（P_D）：1W
e) Thermal resistance（$R_{th(J-C)}$）：5℃/W
f) Maximum junction temperature（T_J） ：175℃
g) Lead temperature（T_h ， 10s）：260℃
h) Input voltage range（V_I）：-0.3 V ～3.6V

6.4 Recommended Operation Conditions

a) Core supply voltage range to ground potential（V_{DDD18}、V_{DDA18}）：1.65V ～ 1.95V
b) IO supply voltage range to ground potential（V_{DDD33}、V_{DDA33}）：3.0V ～ 3.6V
c) Case operation temperature range(T_A) ：-55℃~125℃
d) Operation frequency：2MHz~200MHz

7. Specifications

All electrical characteristics are shown in table 7-1 and tabel7-2.

Table 7-1 BM4802AMQRH absolute maximum rating

Parameter	Symbol	Value	Unit
I/O Voltage	V_{DDD33} 、V_{DDA33}	-0.3~3.8	V
Core Voltage	V_{DDD18}、V_{DDA18}	-0.3~2.0	V
Storage Temperature Range	T_{stg}	-65~+150	˚C
Operating Temperature Range (Ambient)	To	-55 ~+125	˚C
Thermal resistance junction to case	$R_{th(J-C)}$	5℃/W	-

Table 7-2 DC electrical characteristics

Paramater	Symbol	Limit Value		Units
		Min	Max	
Operating Voltage（I/O Voltage）	V_{DDD33} 、V_{DDA33}	3.0	3.6	V
Operating Voltage（Core Voltage）	V_{DDD18}、V_{DDA18}	1.65	1.95	V
Input negative clamp voltage	V_{IK}	-1.2	-0.2	V
Output high level voltage	V_{OH}	2.4	—	V
Output low level voltage	V_{OL}	—	0.4	V
Input high level voltage	V_{IH}	2.2	—	V
Input low level voltage	V_{IL}	—	0.8	V
Input high level leakage current	I_{IH}	—	1	μA
Output low level leakage current	I_{IL}	-1	—	μA
Pull-down input high level leakage current	I_{IHPD}	—	200	μA
Pull-up input low level leakage current	I_{ILPU}	-120	—	μA
3 state output high level leakage current	I_{OZH}	—	1	μA
3 state output low level leakage current	I_{OZL}	-1	—	μA
Stand-by supply current	$I_{DD1(SB)}$ (V_{DDD18})	—	5	mA
	$I_{DD2(SB)}$ (V_{DDD33})	—	10	mA
Operating supply current	$I_{DD1(OP)}$ (V_{DDD18})	—	230	mA
	$I_{DD2(OP)}$ (V_{DDD33})	—	130	mA

8. Package Specifications

The specifications of CQFP196 package are shown in figure8-1.

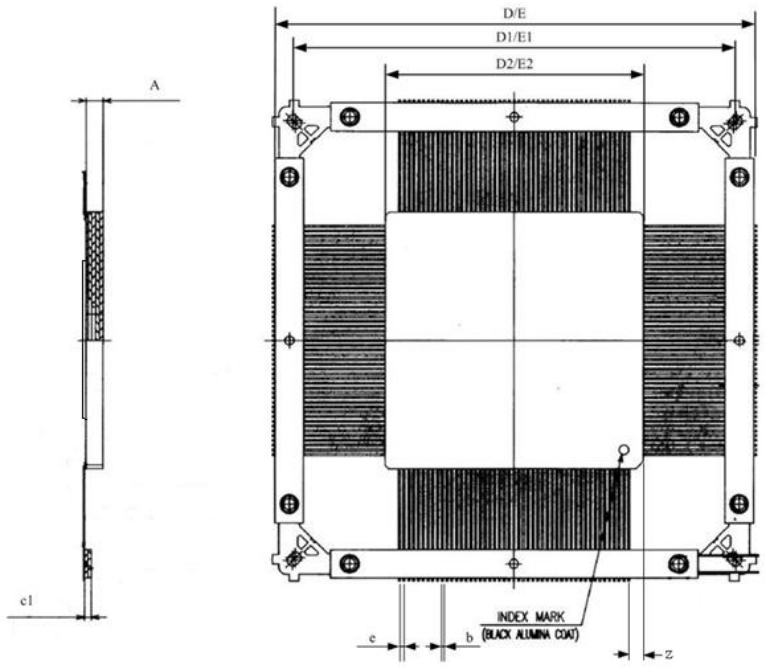


Figure 8-1 CQFP196 package specifications

Table 8-1 size symbol list

Value （unit：mm）

Size symbol	min	typical	max
A	2.00	——	2.80
b	0.2	——	0.3
c1	0.65	——	1.15
e	——	0.635	——
D/E	62.49	——	64.76
D1/E1	57.72	——	59.12
D2/E2	33.80	——	34.80
z	1.65	——	2.3

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