Ver 1.0

SpaceWire Router

Datasheet

Part Number： BM4803AMQRH

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1. Features

- •Eight SpaceWire bi-directional serial ports.
- •Two external parallel input/output ports each comprising an input FIFO and an output FIFO.
- •A crossbar switch connecting any input port to any output port.
- •An internal configuration port accessible via the crossbar switch from the external parallel input/output port or the SpaceWire input/output ports.
- •A routing table accessible via the configuration port which holds the logical address to output port mapping.
- •Control logic to control the operation of the switch, performing arbitration and group adaptive routing.
- •Control registers that can be written and read by the configuration port and which hold control information e.g. link operating speed.
- •An external time-code interface comprising tick_in, tick_out and current tick count value.
- •Internal status/error registers accessible via the configuration port.
- •Watchdog timers on all ports.
- •Internal status/error registers accessible via the configuration port using the RMAP protocol
- • External status/error signals.
- •Power supply: IO power supply 3.3V, Core power supply 1.8V
- • Maximum power dissipation:1.6W
- •ESD:2000V
- • Radiation resistance

  Total ionizing dose：≥100Krad（Si）

  Single event latch-up threshold：≥75MeV·cm^2/mg

  Single event upset threshold：≥15MeV cm^2/mg
- •Package: 196 pins CQFP

2. General Description

BM4803AMQRH is a SpaceWire router. It consists of comprises 8 SpaceWire ports and a routing matrix. The routing matrix enables packets arriving at one SpaceWire port to be transferred to and sent out of another port on the routing switch. A SpaceWire routing switch is thus able to connect together many SpaceWire nodes, providing a means of routing packets between the nodes connected to it.

3. Function Block Diagram

A block diagram of BM4803AMQRH is given in Figure 3-1.

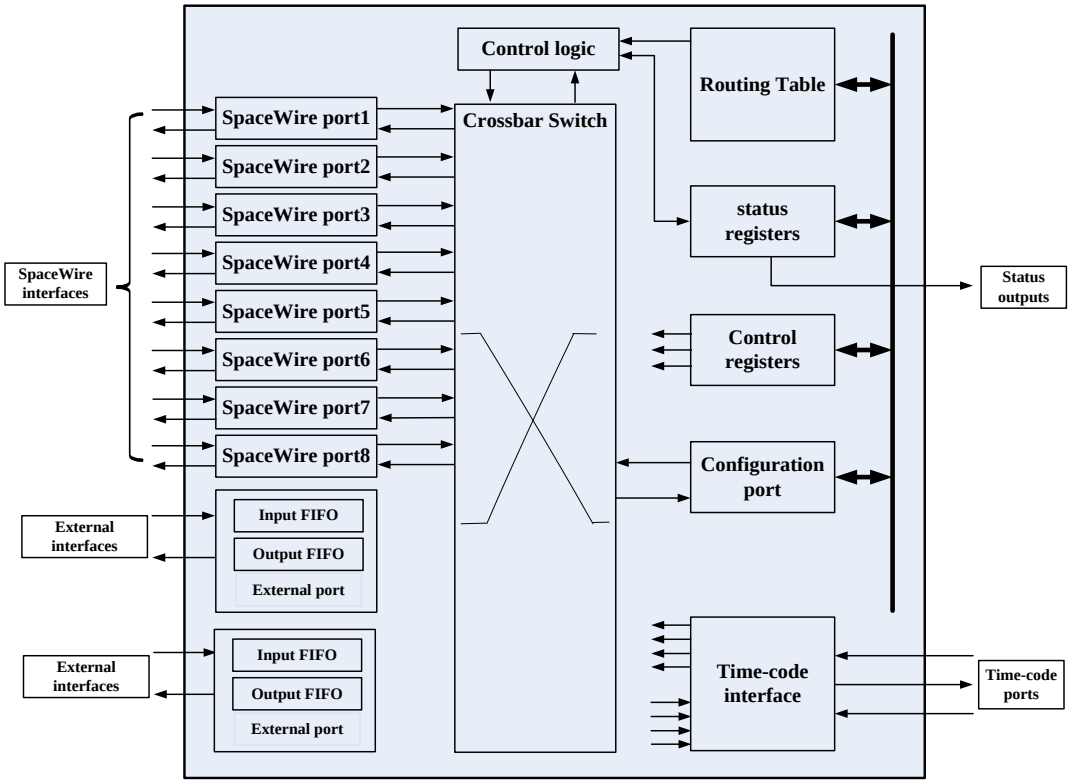
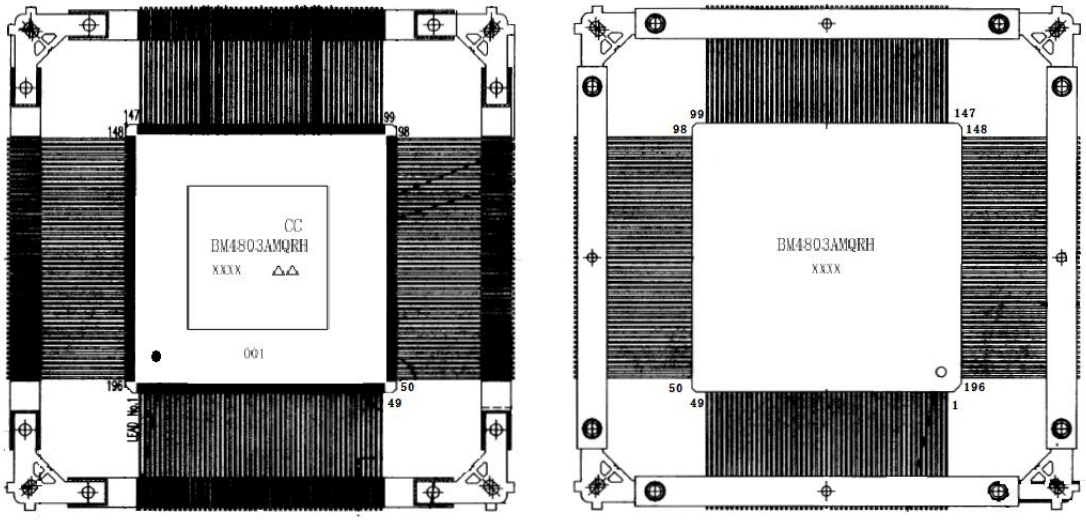


Figure 3-1 SpaceWire router block diagram

4. Packages and Pin Function Descriptions

The provided package is: CQFP196.

BM4803AMQRH CQFP196 pin configuration is shown in 4-1.



Topside View **Underside View**

Figure 4-1 CQFP196 pin configuration

Talble 4-1 BM4803AMQRH CQFP196 Pin Function Descriptions

Global Signals				
PinNo	**Signal**	**Dir**	**Description**	**Type**
2	clk	In	System clock. Provides the reference clock for all modules except the interface receivers.	CMOS3V3
3	rstn	In	Asynchronous system reset (active low).	CMOS3V3
4	testloen	In	ASIC Test control signal; Shall be connected to logic ‘0’ during normal operation. Tie to ground.	CMOS3V3
5	testen	In	ASIC Test control signal; Shall be connected to logic ‘0’ during normal operation. Tie to ground.	CMOS3V3
10 9 6	feedbdiv (2) feedbdiv (1) feedbdiv (0)	In	Set the output clock rate of the internal PLL as follows: “000”-> 100MHz “001”-> 120MHz “010”-> 140MHz “011”-> 160MHz “100”-> 180MHz	CMOS3V3

			“101”-> 200MHz “110”-> 200MHz “111”-> 200MHz	

Data and Strobe SpaceWire Signals				
PinNo	**Signal**	**Dir**	**Description**	**Type**
24 23	doutp[0] doutm[0]	Out	Differential output pair, data part of Data-Strobe SpaceWire port 1.	LVDS+ LVDS-
34 33	doutp[1] doutm[1]	Out	Differential output pair, data part of Data-Strobe SpaceWire port 2.	LVDS+ LVDS-
46 45	doutp[2] doutm[2]	Out	Differential output pair, data part of Data-Strobe SpaceWire port 3.	LVDS+ LVDS-
55 54	doutp[3] doutm[3]	Out	Differential output pair, data part of Data-Strobe SpaceWire port 4.	LVDS+ LVDS-
67 66	doutp[4] doutm[4]	Out	Differential output pair, data part of Data-Strobe SpaceWire port 5.	LVDS+ LVDS-
77 76	doutp[5] doutm[5]	Out	Differential output pair, data part of Data-Strobe SpaceWire port 6.	LVDS+ LVDS-
87 86	doutp[6] doutm[6]	Out	Differential output pair, data part of Data-Strobe SpaceWire port 7.	LVDS+ LVDS-
97 96	doutp[7] doutm[7]	Out	Differential output pair, data part of Data-Strobe SpaceWire port 8.	LVDS+ LVDS-
22 21	soutp[0] soutm[0]	Out	Differential output pair, strobe part of Data-Strobe SpaceWire port 1.	LVDS+ LVDS-
32 31	soutp[1] soutm[1]	Out	Differential output pair, strobe part of Data-Strobe SpaceWire port 2.	LVDS+ LVDS-
40 39	soutp[2] soutm[2]	Out	Differential output pair, strobe part of Data-Strobe SpaceWire port 3.	LVDS+ LVDS-

53 50	soutp[3] soutm[3]	Out	Differential output pair, strobe part of Data-Strobe SpaceWire port 4.	LVDS+ LVDS-
65 64	soutp[4] soutm[4]	Out	Differential output pair, strobe part of Data-Strobe SpaceWire port 5.	LVDS+ LVDS-
75 74	soutp[5] soutm[5]	Out	Differential output pair, strobe part of Data-Strobe SpaceWire port 6.	LVDS+ LVDS-
83 82	soutp[6] soutm[6]	Out	Differential output pair, strobe part of Data-Strobe SpaceWire port 7.	LVDS+ LVDS-
95 94	soutp[7] soutm[7]	Out	Differential output pair, strobe part of Data-Strobe SpaceWire port 8.	LVDS+ LVDS-
17 18	dinp[0] dinm[0]	In	Differential input pair, data part of Data-Strobe SpaceWire port 1.	LVDS+ LVDS-
25 26	dinp[1] dinm[1]	In	Differential input pair, data part of Data-Strobe SpaceWire port 2.	LVDS+ LVDS-
35 36	dinp[2] dinm[2]	In	Differential input pair, data part of Data-Strobe SpaceWire port 3.	LVDS+ LVDS-
47 48	dinp[3] dinm[3]	In	Differential input pair, data part of Data-Strobe SpaceWire port 4.	LVDS+ LVDS-
60 61	dinp[4] dinm[4]	In	Differential input pair, data part of Data-Strobe SpaceWire port 5.	LVDS+ LVDS-
68 69	dinp[5] dinm[5]	In	Differential input pair, data part of Data-Strobe SpaceWire port 6.	LVDS+ LVDS-
78 79	dinp[6] dinm[6]	In	Differential input pair, data part of Data-Strobe SpaceWire port 7.	LVDS+ LVDS-
88 89	dinp[7] dinm[7]	In	Differential input pair, data part of Data-Strobe SpaceWire port 8.	LVDS+ LVDS-
19	sinp[0]	In	Differential input pair, strobe part	LVDS+

20	sinm[0]		of Data-Strobe SpaceWire port 1.	LVDS-
27 28	sinp[1] sinm[1]	In	Differential input pair, strobe part of Data-Strobe. SpaceWire port 2.	LVDS+ LVDS-
37 38	sinp[2] sinm[2]	In	Differential input pair, strobe part of Data-Strobe SpaceWire port 3.	LVDS+ LVDS-
50 51	sinp[3] sinm[3]	In	Differential input pair, strobe part of Data-Strobe SpaceWire port 4.	LVDS+ LVDS-
62 63	sinp[4] sinm[4]	In	Differential input pair, strobe part of Data-Strobe SpaceWire port 5.	LVDS+ LVDS-
70 71	sinp[5] sinm[5]	In	Differential input pair, strobe part of Data-Strobe SpaceWire port 6.	LVDS+ LVDS-
80 81	sinp[6] sinm[6]	In	Differential input pair, strobe part of Data-Strobe SpaceWire port 7.	LVDS+ LVDS-
90 93	sinp[7] sinm[7]	In	Differential input pair, strobe part of Data-Strobe SpaceWire port 8.	LVDS+ LVDS-

External Port Interface Signals				
PinNo	**Signal**	**Dir**	**Description**	**Type**
112 111 110 107 104 103 102 101 100	ext9_out_data[8] ext9_out_data[7] ext9_out_data[6] ext9_out_data[5] ext9_out_data[4] ext9_out_data[3] ext9_out_data[2] ext9_out_data[1] ext9_out_data[0]	Out	Output data from external port number one FIFO. Bit eight determines the type - data, EOP or EEP. The encodings are defined as: (8) (7……...…0)—Bits (0) (ddddddddd)—Data byte (1) (XXXXXXX0)—EOP (1) (XXXXXXX1)—EEP Bit 7 is the most significant bit of the data byte	CMOS 3V3

113	ext9_out_empty_n	Out	FIFO ready signal for external output port zero. When high the FIFO has data. When low the FIFO is empty.	CMOS 3V3
114	ext9_out_read_n	In	Asserted (low) to read from the external output port zero FIFO. A pull-up resistor should be connected to this input if External FIFO port 9 is not being used.	CMOS 3V3
123 122 121 120 119 118 117 116 115	ext9_in_data[8] ext9_in_data[7] ext9_in_data[6] ext9_in_data[5] ext9_in_data[4] ext9_in_data[3] ext9_in_data[2] ext9_in_data[1] ext9_in_data[0]	In	Input data to external port number one FIFO. Bit eight determines the type - data, EOP or EEP. The encodings are defined as: (8) (7……...…0)—Bits (0) (ddddddd)—Data byte (1) (XXXXXXX0)—EOP (1) (XXXXXXX1)—EEP Bit 7 is the most significant bit of the data byte. Pull-up resistors should be connected to these inputs if External FIFO port 9 is not being used.	CMOS 3V3
124	ext9_in_full_n	Out	FIFO ready signal for external input port zero. When high there is space in the FIFO so it can be written to. When low the FIFO is full.	CMOS 3V3
127	ext9_in_write_n	In	Asserted (low) to write to the external input port zero FIFO. A pull-up resistor should be connected to this input if External FIFO port 9 is not being used.	CMOS 3V3
138 137 136 133 132 131	ext10_out_data[8] ext10_out_data[7] ext10_out_data[6] ext10_out_data[5] ext10_out_data[4] ext10_out_data[3]	Out	Output data from external port number two FIFO . Bit eight determines the type - data, EOP or EEP. The encodings are defined as: (8) (7……...…0)—Bits (0) (ddddddd)—Data byte (1) (XXXXXXX0)—EOP (1) (XXXXXXX1)—EEP	CMOS 3V3

129 128	ext10_out_data[2] ext10_out_data[1] ext10_out_data[0]		Bit 7 is the most significant bit of the data byte.	
139	ext10_out_empty_n	Out	FIFO ready signal for external output port one. When high the FIFO has data. When low the FIFO is empty.	CMOS 3V3
142	ext10_out_read_n	In	Asserted (low) to read from the external output port one FIFO. A pull-up resistor should be connected to this input if External FIFO port 10 is not being used.	CMOS 3V3
151 150 149 148 147 146 145 144 143	ext10_in_data[8] ext10_in_data[7] ext10_in_data[6] ext10_in_data[5] ext10_in_data[4] ext10_in_data[3] ext10_in_data[2] ext10_in_data[1] ext10_in_data[0]	In	Input data to external port number two FIFO. Bit eight determines the type - data, EOP or EEP. The encodings are defined as: (8) (7……...…0)—Bits (0) (ddddddd)—Data byte (1) (XXXXXXX0)—EOP (1) (XXXXXXX1)—EEP Bit 7 is the most significant bit of the data byte. Pull-up resistors should be connected to these inputs if External FIFO port 10 is not being used.	CMOS 3V3
152	ext10_in_full_n	Out	FIFO ready signal for external input port one. When high there is space in the FIFO so it can be written to. When low the FIFO is full.	CMOS 3V3
153	ext10_in_write_n	In	Asserted (low) to write to the external input port one FIFO. A pull-up resistor should be connected to this input if External FIFO port 10 is not being used.	CMOS 3V3

Time-Code Signals				
PinNo	**Signal**	**Dir**	**Description**	**Type**
158	ext_tick_in	In	The rising edge of the EXT_TICK_IN signal	COM

			is used to indicate when a time-code is to be sent. On the rising edge of the EXT_TICK_IN signal the SEL_EXT_TIME signal is sampled to determine if the time-code value is to be provided by the internal time-counter or by the external time input EXT_TIME_IN(7:0). The SEL_EXT_TIME and the EXT_TIME_IN(7:0) signals must be set up prior to the rising edge of EXT_TICK_IN and must be held static sometime afterwards. If the time-code port is not being used this input should be pulled down.	3V3
166 165 164 163 162 161 160 159	ext_time_in[7] ext_time_in[6] ext_time_in[5] ext_time_in[4] ext_time_in[3] ext_time_in[2] ext_time_in[1] ext_time_in[0]	In	EXT_TIME_IN(7:0) provides the value of the timecode to be distributed by the router when an external time-code source is selected i.e. when SEL_EXT_TIME is high on the rising edge of EXT_TICK_IN. When SEL_EXT_TIME is high on the rising edge of EXT_TICK_IN the value of the time-code counter is used for bits 5:0 of the time-code and bits 7:6 of the EXT_TIME_IN(7:0) are used for the two control signals, bits 7:6 of the time-code. If the time-code port is not being used these inputs should be pulled down.	COM 3V3
167	sel_ext_time	In	If SEL_EXT_TIME is high on the rising edge of EXT_TICK_IN the value on EXT_TIME_IN(7:0) is loaded into the internal time-code register and propagated by the router. If SEL_EXT_TIME is low on the rising edge of EXT_TICK_IN the value to be sent in the time-code will be taken from the internal time-code counter in the router. The two control-bits (bits 7:6) of the time-code will come from bits 7:6 of the EXT_TIME_IN(7:0) input. If the time-code port is not being used this input should be pulled down.	COM 3V3
168	time_ctr_rst	In	This signal causes the internal time-code counter to be reset to zero. The timing parameters used for EXT_TICK_IN also apply to the time-code counter reset signal (TIME_CTR_RST). If the time-code port is	COM 3V3

			not being used this input should be pulled down.	
169	ext_tick_out	Out	The falling edge of EXT_TICK_OUT is used to indicated the reception of a time-code. The value of this time-code is place on the EXT_TIME_OUT(7:0) outputs and is valid on the rising edge of EXT_TICK_OUT.	COM 3V3
179 178 177 176 173 172 171 170	ext_time_out[7] ext_time_out[6] ext_time_out[5] ext_time_out[4] ext_time_out[3] ext_time_out[2] ext_time_out[1] ext_time_out[0]	Out	Received time-code value which is valid when EXT_TICK_OUT is asserted. The value of a received time-code is output on the falling edge of EXT_TICK_OUT. The EXT_TIME_OUT(7:0) value is held until the next time-code is output.	COM 3V3

Link error indication Signals				
PinNo	**Signal**	**Dir**	**Description**	**Type**
183 182 181 180	stat_mux_addr[3] stat_mux_addr[2] stat_mux_addr[1] stat_mux_addr[0]	in	Select the error indication status signals to be output on STAT_MUX_OUT .These inputs should be driven or pulled up or down depending on what information is required from the status outputs.	CMOS 3V3
195 194 193 192 191 188 187 186	stat_mux_out[7] stat_mux_out[6] stat_mux_out[5] stat_mux_out[4] stat_mux_out[3] stat_mux_out[2] stat_mux_out[1] stat_mux_out[0]	inout	Multi function pin. Power on Configuration After reset the STAT_MUX_OUT pins are inputs which define the power on configuration status of the router. Normal Operation After the power on reset configuration of the router has been read from STAT_MUX_OUT the pins are driven as outputs by the router.	CMOS 3V3

Reset Configuration Signals			
Signal	**Dir**	**Description**	**Type**
stat_mux_out (2:0) [maps to->por_tx_rate (2:0)]	In	Sets the transmitter maximum data rate after reset. The data rate can subsequently be changed during normal operation using port configuration commands. The values are listed below. "111" – Full data rate after link start-up. "110" – 1/2 data rate after link start-up. "101" – 1/3 data rate after link start-up. "100" – 1/4 data rate after link start-up. "011" – 1/5 data rate after link start-up. "010" – 1/6 data rate after link start-up. "001" – 1/7 data rate after link start-up. "000" – 1/8 data rate after link start-up. Note: POR_TX_RATE affects all SpaceWire ports in the router. Note: The data rate is dependent on FEEDBDIV at reset	CMOS 3V3
stat_mux_out (3) [maps to-> por_addr_self_n]	In	If asserted (low) after reset allows a router port to address itself and therefore cause an input packet to be returned through the same input port. This mode may only be suitable for debug and test operations. This signal is active low.	CMOS 3V3
stat_mux_out (4) [maps to-> por_timeout_en_n]	In	Power on reset signal which determines if output port timeouts are enabled at start-up. When asserted (low) the port timeouts are enabled. When de-asserted (high) they are disabled. This signal is active low. An external pull down resistor is recommended on this pin so to enable the watchdog timers.	CMOS 3V3
stat_mux_out (5) [maps to-> por_sel_timeout0_n]	In	Power on reset value which determines the initial timeout value. The following values determine which timeout is selected at power up. '1' => Timeout period is ~ 60-80 us. '0' => Timeout period is ~ 1.3 ms.	CMOS 3V3

		Timeout Period is: '1' => 200x(2^2)x(10 MHz clk period) '0' => 200x(2^16)x(10 MHz clk period) An external pull down resistor is recommended on this pin to provide the longer timeout interval.	
stat_mux_out (6) [maps to-> por_start_on_req_n]	In	Power on reset signal which determines if the output ports automatically start up when they are the destination address of a packet. When asserted (low) the output port will automatically start on request. This signal is active low.	CMOS 3V3
stat_mux_out (7) [maps to-> por_dsble_on_silence_n]	In	Power on reset signal which determines if the output ports are disabled when no activity is detected on an output port for the current timeout period. When asserted (low) an output port is disabled when it has not sent any information for longer than the current timeout period. This signal is active low.	CMOS 3V3

5. Pin List

BM4803AMQRH CQFP196 pin list is shown in table 5-1.

Table 5-1 BM4803AMQRH CQFP196 pin list

Pin number	Signal symbol	Functional description
1	V_{DD33}	3.3V power supply
2	clk	30MHz clock
3	rstn	Reset
4	testloen	Scan mode
5	testen	Scan enable
6	feedbdiv[0]	Pll divider bit 0（LS）
7	V_{SS18}	1.8V gnd
8	V_{DD18}	1.8V power supply
9	feedbdiv[1]	Pll divider bit 1（LS）
10	feedbdiv[2]	Pll divider bit 2（MS）
11	test_func_clk	Chip test pin
12	test_func	Chip test pin
13	V_{SS18_pll}	1.8V gnd

14	V_{DD18_pll}	1.8V power supply
15	V_{SS33_pll}	3.3V gnd
16	V_{DD33_pll}	3.3V power supply
17	dinp[0]	SpW port 1 input data +
18	dinm[0]	SpW port 1 input data -
19	sinp[0]	SpW port 1 input strobe +
20	sinm[0]	SpW port 1 input strobe -
21	soutm[0]	SpW port 1 output strobe -
22	soutp[0]	SpW port 1 output strobe +
23	doutm[0]	SpW port 1 output data -
24	doutp[0]	SpW port 1 output data +
25	dinp[1]	SpW port 2 input data +
26	dinm[1]	SpW port 2 input data -
27	sinp[1]	SpW port 2 input strobe +
28	sinm[1]	SpW port 2 input strobe -
29	V_{SS_lvds}	LVDS gnd
30	V_{DD33_lvds}	LVDS 3.3V power supply
31	soutm[1]	SpW port 2 output strobe -
32	soutp[1]	SpW port 2 output strobe +
33	doutm[1]	SpW port 2 output data -
34	doutp[1]	SpW port 2 output data +
35	dinp[2]	SpW port 3 input data +
36	dinm[2]	SpW port 3 input data -
37	sinp[2]	SpW port 3 input strobe +
38	sinm[2]	SpW port 3 input strobe -
39	soutm[2]	SpW port 3 output strobe -
40	soutp[2]	SpW port 3 output strobe +
41	V_{SS_lvds}	LVDS gnd
42	V_{SS_lvds}	LVDS gnd
43	V_{DD18_lvds}	LVDS 1.8V power supply
44	V_{DD33_lvds}	LVDS 3.3V power supply
45	doutm[2]	SpW port 3 output data -
46	doutp[2]	SpW port 3 output data +
47	dinp[3]	SpW port 4 input data +
48	dinm[3]	SpW port 4 input data -
49	NC	
50	sinp[3]	SpW port 4 input strobe +
51	sinm[3]	SpW port 4 input strobe -
52	soutm[3]	SpW port 4 output strobe -
53	soutp[3]	SpW port 4 output strobe +
54	doutm[3]	SpW port 4 output data -
55	doutp[3]	SpW port 4 output data +

56	V_{SS_lvds}	LVDS gnd
57	V_{DD33_lvds}	LVDS 3.3V power supply
58	V_{SS_lvds}	LVDS gnd
59	V_{DD18_lvds}	LVDS 1.8V power supply
60	dinp[4]	SpW port 5 input data +
61	dinm[4]	SpW port 5 input data -
62	sinp[4]	SpW port 5 input strobe +
63	sinm[4]	SpW port 5 input strobe -
64	soutm[4]	SpW port 5 output strobe -
65	soutp[4]	SpW port 5 output strobe +
66	doutm[4]	SpW port 5 output data -
67	doutp[4]	SpW port 5 output data +
68	dinp[5]	SpW port 6 input data +
69	dinm[5]	SpW port 6 input data -
70	sinp[5]	SpW port 6 input strobe +
71	sinm[5]	SpW port 6 input strobe -
72	V_{SS_lvds}	LVDS gnd
73	V_{DD33_lvds}	LVDS 3.3V power supply
74	soutm[5]	SpW port 6 output strobe -
75	soutp[5]	SpW port 6 output strobe +
76	doutm[5]	SpW port 6 output data -
77	doutp[5]	SpW port 6 output data +
78	dinp[6]	SpW port 7 input data +
79	dinm[6]	SpW port 7 input data -
80	sinp[6]	SpW port 7 input strobe +
81	sinm[6]	SpW port 7 input strobe -
82	soutm[6]	SpW port 7 output strobe -
83	soutp[6]	SpW port 7 output strobe +
84	V_{SS_lvds}	LVDS gnd
85	V_{DD18_lvds}	LVDS 1.8V power supply
86	doutm[6]	SpW port 7 output data -
87	doutp[6]	SpW port 7 output data +
88	dinp[7]	SpW port 8 input data +
89	dinm[7]	SpW port 8 input data -
90	sinp[7]	SpW port 8 input strobe +
91	V_{SS_lvds}	LVDS gnd
92	V_{DD33_lvds}	LVDS 3.3V power supply
93	sinm[7]	SpW port 8 input strobe -
94	soutm[7]	SpW port 8 output strobe -
95	soutp[7]	SpW port 8 output strobe +
96	doutm[7]	SpW port 8 output data -
97	doutp[7]	SpW port 8 output data +

98	V_{SS33}	3.3V gnd
99	V_{DD33}	3.3V power supply
100	ext9_out_data[0]	External FIFO port 9 output data
101	ext9_out_data[1]	External FIFO port 9 output data
102	ext9_out_data[2]	External FIFO port 9 output data
103	ext9_out_data[3]	External FIFO port 9 output data
104	ext9_out_data[4]	External FIFO port 9 output data
105	V_{SS33}	3.3V gnd
106	V_{DD33}	3.3V power supply
107	ext9_out_data[5]	External FIFO port 9 output data
108	V_{SS18}	1.8V gnd
109	V_{DD18}	1.8V power supply
110	ext9_out_data[6]	External FIFO port 9 output data
111	ext9_out_data[7]	External FIFO port 9 output data
112	ext9_out_data[8]	External FIFO port 9 output data
113	ext9_out_empty_n	External FIFO port 9 output empty
114	ext9_out_read_n	External FIFO port 9 output read
115	ext9_in_data[0]	External FIFO port 9 input data
116	ext9_in_data[1]	External FIFO port 9 input data
117	ext9_in_data[2]	External FIFO port 9 input data
118	ext9_in_data[3]	External FIFO port 9 input data
119	ext9_in_data[4]	External FIFO port 9 input data
120	ext9_in_data[5]	External FIFO port 9 input data
121	ext9_in_data[6]	External FIFO port 9 input data
122	ext9_in_data[7]	External FIFO port 9 input data
123	ext9_in_data[8]	External FIFO port 9 input data
124	ext9_in_full_n	External FIFO port 9 input full
125	V_{SS33}	3.3V gnd
126	V_{DD33}	3.3V power supply
127	ext9_in_write_n	External FIFO port 9 input write
128	ext10_out_data[0]	External FIFO port 10 output data
129	ext10_out_data[1]	External FIFO port 10 output data
130	ext10_out_data[2]	External FIFO port 10 output data
131	ext10_out_data[3]	External FIFO port 10 output data
132	ext10_out_data[4]	External FIFO port 10 output data
133	ext10_out_data[5]	External FIFO port 10 output data
134	V_{SS18}	1.8V gnd
135	V_{DD18}	1.8V power supply
136	ext10_out_data[6]	External FIFO port 10 output data
137	ext10_out_data[7]	External FIFO port 10 output data
138	ext10_out_data[8]	External FIFO port 10 output data
139	ext10_out_empty_n	External FIFO port 10 output empty

140	V_{SS33}	3.3V gnd
141	V_{DD33}	3.3V power supply
142	ext10_out_read_n	External FIFO port 10 output read
143	ext10_in_data[0]	External FIFO port 10 input data
144	ext10_in_data[1]	External FIFO port 10 input data
145	ext10_in_data[2]	External FIFO port 10 input data
146	ext10_in_data[3]	External FIFO port 10 input data
147	ext10_in_data[4]	External FIFO port 10 input data
148	ext10_in_data[5]	External FIFO port 10 input data
149	ext10_in_data[6]	External FIFO port 10 input data
150	ext10_in_data[7]	External FIFO port 10 input data
151	ext10_in_data[8]	External FIFO port 10 input data
152	ext10_in_full_n	External FIFO port 10 input full
153	ext10_in_write_n	External FIFO port 10 input wrte
154	V_{SS33}	3.3V gnd
155	V_{DD33}	3.3V power supply
156	V_{SS18}	1.8V gnd
157	V_{DD18}	1.8V power supply
158	ext_tick_in	Time-code tick in
159	ext_time_in[0]	Time-code input
160	ext_time_in[1]	Time-code input
161	ext_time_in[2]	Time-code input
162	ext_time_in[3]	Time-code input
163	ext_time_in[4]	Time-code input
164	ext_time_in[5]	Time-code input
165	ext_time_in[6]	Time-code input
166	ext_time_in[7]	Time-code input
167	sel_ext_time	Time-code counter/input selection
168	time_ctr_rst	Time-code counter reset
169	ext_tick_out	Time-code tick out
170	ext_time_out[0]	Time-code output
171	ext_time_out[1]	Time-code output
172	ext_time_out[2]	Time-code output
173	ext_time_out[3]	Time-code output
174	V_{SS33}	3.3V gnd
175	V_{DD33}	3.3V power supply
176	ext_time_out[4]	Time-code output
177	ext_time_out[5]	Time-code output
178	ext_time_out[6]	Time-code output
179	ext_time_out[7]	Time-code output
180	stat_mux_addr[0]	Status output multiplexer address
181	stat_mux_addr[1]	Status output multiplexer address

182	stat_mux_addr[2]	Status output multiplexer address
183	stat_mux_addr[3]	Status output multiplexer address
184	V_{SS18}	1.8V gnd
185	V_{DD18}	1.8V power supply
186	stat_mux_out[0]	Status output /configuration input
187	stat_mux_out[1]	Status output /configuration input
188	stat_mux_out[2]	Status output /configuration input
189	V_{SS33}	3.3V gnd
190	V_{DD33}	3.3V power supply
191	stat_mux_out[3]	Status output /configuration input
192	stat_mux_out[4]	Status output /configuration input
193	stat_mux_out[5]	Status output /configuration input
194	stat_mux_out[6]	Status output /configuration input
195	stat_mux_out[7]	Status output /configuration input
196	V_{SS33}	3.3V gnd

6. Detailed Description

6.1 Function Description

The main functions of BM4803AMQRH are as follows:

1) SpaceWire ports

The SpaceWire router has eight bi-directional SpaceWire links each conformant with the SpaceWire standard. Each SpaceWire link is controlled by an associated link register and routing control logic. Network level error recovery is performed when an error is detected on the SpaceWire link as defined in the SpaceWire standard. Packets received on SpaceWire links are routed by the routing control logic to the configuration port, other SpaceWire link ports or the external FIFO ports. Packets with invalid addresses are discarded by the SpaceWire router dependent on the packet address. The SpaceWire link status is recorded in the associated link register and error status is held by the router until cleared by a configuration command.

2) External ports

The SpaceWire router has two bi-directional parallel FIFO interfaces that can be used to connect the router to an external host system. The external port FIFO is two data characters deep. Each FIFO is written to or read from synchronously with the 30MHz system clock. An eight-bit data interface and an extra control bit for end of

packet markers are provided by each external port FIFO. Packets received by the external port are routed by the routing control logic to the configuration port, SpaceWire link ports or the other external port dependent on the packet address. Packets with invalid addresses are discarded by the SpaceWire router.

3) Configuration ports

The SpaceWire router has one configuration port which performs read and write operations to internal router registers. Packets are routed to the configuration port when a packet with a leading address byte of zero is received. The Remote Memory Access Protocol (RMAP) to access the configuration port. If an invalid command packet is received then the error is flagged to an associated status register and the packet is discarded.

4) Routing table

The SpaceWire router routing table is set by the router command packets to assign logical addresses to physical destination ports on the router. A group of destination ports can be set, in each routing table location, to enable group adaptive routing. In group adaptive routing a packet can be routed to its destination through one of a set of output ports dependent on which ports in the set are free to use. When a packet is received with a logical address the routing table is checked by the routing control logic and the packet is routed to the destination port when the port is ready.

Routing table locations are set to invalid at power on or at reset. An invalid routing address will cause the packet to be spilled by the control logic. The routing table logical addresses can also be set to support high priority and header deletion. High priority packets are routed before low priority packets and header deletion of logical addresses can be used to support regional logical addressing.

5) Routing control logic and crossbar

The routing control logic is responsible for arbitration of output ports, group adaptive routing and the crossbar switching. Arbitration is performed when two or more source ports are requesting to use the same destination port. A priority based arbitration scheme with two priority levels, high and low, is used where high priority packets are routed before low priority packets. Fair arbitration is performed on packets which have the same priority levels to ensure each packet gets equal access to the output port.

Group adaptive routing control selects one of a number of output ports for sending out the source packet. The crossbar switch connects an input port to an output port allowing data to flow from the input port to the output port. Several input ports

may be connected simultaneously to several output ports all passing data. Two or more input ports may not be connected to a single output port. The crossbar switch is a “non-blocking” type because the connection of one input port to an output port does not prevent another input port being connected to another output port at the same time. It is possible for all eight input ports to be each connected to an output port so that all input ports and output ports are being used.

6) Time-code processing

An internal time-code register is used in the router to allow the router to be a time-code master or a time-code slave.

In master mode the time-code interface is used to provide a tick-in to the SpaceWire routing causing time-codes to be propagated through the network. Two modes of time master operation are supported, an automatic mode where a time-code is propagated on each external tick-in and a normal mode where the time-code is propagated dependent on the external time-in signal.

In time-code slave mode a valid received time-code, one plus the value of the router time-code register, causes a tick-out to be sent to the SpaceWire links and the external time-code interface. The time-code is propagated to all time-code ports except the port on which the time-code was received. If the time-code received is not one plus the value of the time-code register then the time-code register is updated but the tick-out is not performed. In this way circular network paths do not cause a constant stream of time-codes to be sent in a loop.

7) Control/status registers

The control and status registers in the SpaceWire router provide the means to control the operation of the router, set the router configuration and parameters or monitor the status of the device. The registers are accessed using RMAP command packets received by the configuration port.

6.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 10℃～30℃ and relative humidity less than 70%. There should be no acid , alkali or other radiant gas in the environment,

6.3 Absolute Maximum Ratings

a) Core supply voltage range to ground potential（V_{DD18}、V_{DD18_pll}、V_{DD18_LVDS}）：-0.3V ～2.0V
b) IO supply voltage range to ground potential（V_{DD33}、V_{DD33_pll}、V_{DD33_LVDS}）：-0.3V ～3.8V
c) Storage temperature（T_{stg}）：-65℃～ 150℃
d) Power dissipation（P_D）：1.6W
e) Thermal resistance（$R_{th(J-C)}$）：5℃/W
f) Maximum junction temperature（T_J） ：175℃
g) Lead temperature（T_h ，10s）：260℃
h) Input voltage range（V_I）：-0.5 V ～3.6V

6.4 Recommended Operation Conditions

a) Core supply voltage range to ground potential（V_{DD18}、V_{DD18_pll}、V_{DD18_LVDS}）：1.65V ～1.95V
b) IO supply voltage range to ground potential（V_{DD33}、V_{DD33_pll}、V_{DD33_LVDS}）：3.0V ～3.6V
c) Case operation temperature range(T_A) ：-55℃~125℃
d) Operation frequency：2MHz~200MHz

7. Specifications

All electrical characteristics are shown in table 7-1 and tabel7-2.

Table 7-1 BM4803AMQRH electrical characteristics

paramater	symbol	limit value		units
		min	max	
Input negative clamp voltage	V_{IK}	-1.2	-0.2	V
output high level voltage	V_{OH}	2.4	—	V
output low level voltage	V_{OL}	—	0.4	V
input high level voltage	V_{IH}	2.0	—	V
input low level voltage	V_{IL}	—	0.8	V
input high level leakage current	I_{IH}	—	1	μA
output low level leakage current	I_{IL}	-1	—	μA

pull-down input high level leakage current	I_{IHPD}	—	200	μA
pull-up input low level leakage current	I_{ILPU}	-120	—	μA
3 state output high level leakage current	I_{OZH}	—	1	μA
3 state output low level leakage current	I_{OZL}	-1	—	μA
Stand-by supply current	$I_{DD1(SB)}$ (V_{DD18})	—	5	mA
	$I_{DD2(SB)}$ (V_{DD33})	—	5	mA
	$I_{DD3(SB)}$ (V_{DD18_lvds})	—	10	mA
	$I_{DD4(SB)}$ (V_{DD33_lvds})	—	105	mA
Operating supply current	$I_{DD1(OP)}$ (V_{DD18})		330	mA
	$I_{DD2(OP)}$ (V_{DD33})	—	100	mA
	$I_{DD3(OP)}$ (V_{DD18_lvds})	—	15	mA
	$I_{DD4(OP)}$ (V_{DD33_lvds})	—	130	mA

Table 7-2 LVDS interface electrical characteristics

parameter	symbol	limit value		units
		min	max	
differential output voltage	V_{OD}	247	454	mV
common mode output voltage	V_{OS}	622	1375	mV
differential output voltage drift	$\|\Delta V_{OD}\|$	0	50	mV
common mode output voltage drift	$\|\Delta V_{OS}\|$	0	200	mV
common mode input voltage	V_i	200	2200	mV
differential mode input voltage	V_{idth}	-100	100	mV

8. Package Specifications

The specifications of CQFP196 package are shown in figure8-1.

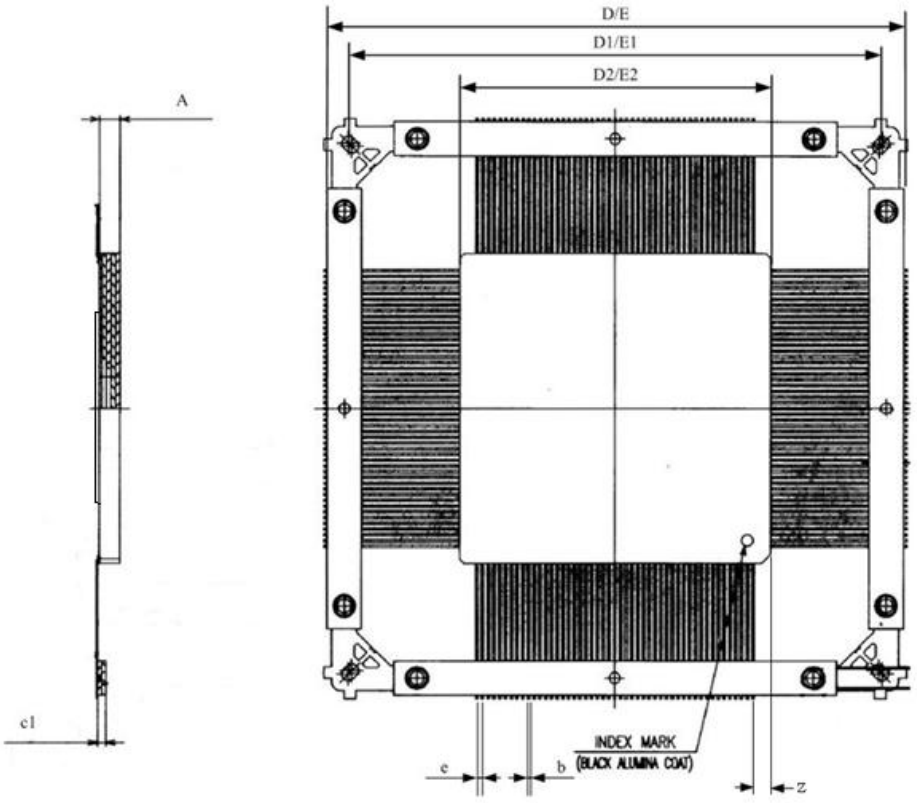


Figure 8-1 CQFP196 package specifications

Table 8-1 size symbol list

Value （unit：mm）

Size symbol	min	typical	max
A	2.00	——	2.80
b	0.2	——	0.3
c1	0.65	——	1.15
e	——	0.635	——
D/E	62.49	——	64.76
D1/E1	57.72	——	59.12
D2/E2	33.80	——	34.80
z	1.65	——	2.3

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