

For Air-Conditioner Fan Motor

3-Phase Brushless Fan Motor Driver

BM6243FS

General Description

This 3-phase Brushless Fan motor driver IC adopts PrestoMOSFET™ as the output transistor, and put in a small full molding package with the high voltage gate driver chip. The protection circuits for overcurrent, overheating, under voltage lock out and the high voltage bootstrap diode with current regulation are built-in. It provides optimum motor drive system for a wide variety of applications by the combination with controller BD6201x series and enables motor unit standardization.

Features

- 600V PrestoMOSFET™ Built-in
- Output Current 2.5A
- Bootstrap operation by floating high side driver (including diode)
- 3.3V logic input compatible
- Protection circuits provided: CL, OCP, TSD, UVLO, MLP and the external fault input
- Fault Output (open drain)

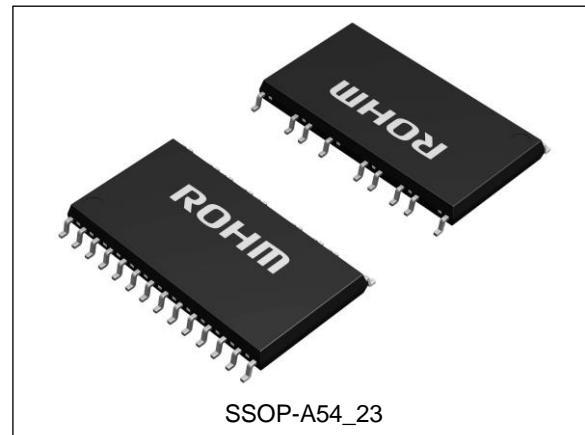
Applications

- Air Conditioners; Air Purifiers; Water Pumps; Dishwashers; Washing Machines

Key Specifications

- Output MOSFET Voltage: 600V
- Driver Output Current (DC): $\pm 2.5\text{A}$ (Max)
- Driver Output Current (Pulse): $\pm 4.0\text{A}$ (Max)
- Output MOSFET DC On Resistance: 1.7Ω (Typ)
- Maximum Junction Temperature: $+150^\circ\text{C}$

Package W(Typ) x D(Typ) x H(Max)
SSOP-A54_23 22.0mm x 14.1mm x 2.4mm



Typical Application Circuit

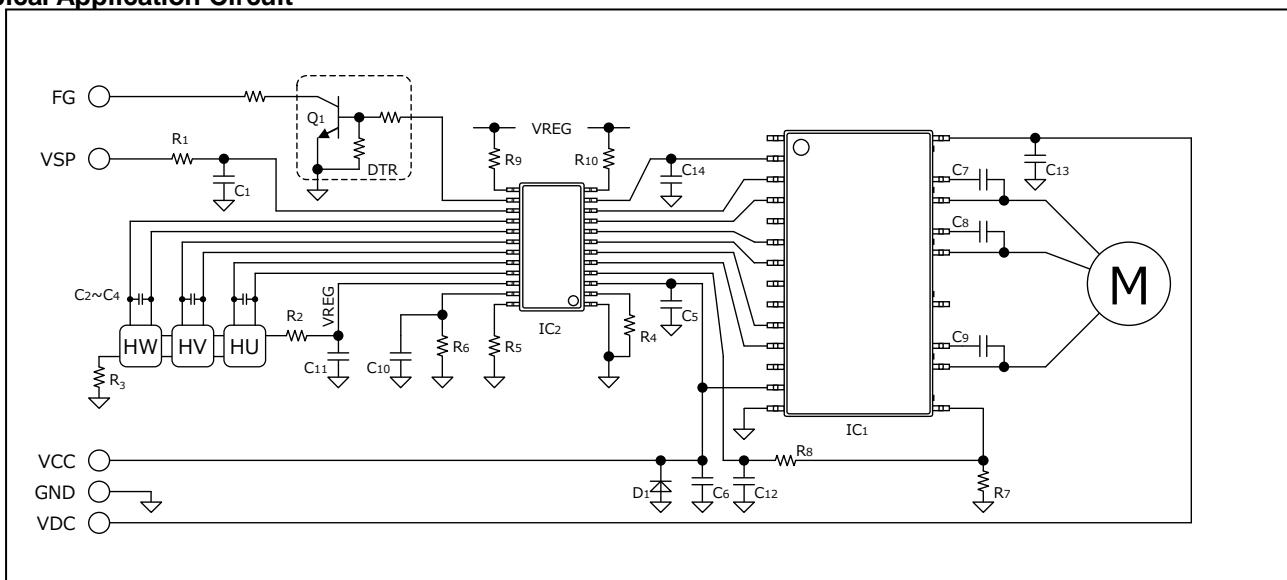


Figure 1. Application Circuit Example(BM6243FS & BD6201xFs)

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Block Diagram and Pin Configuration

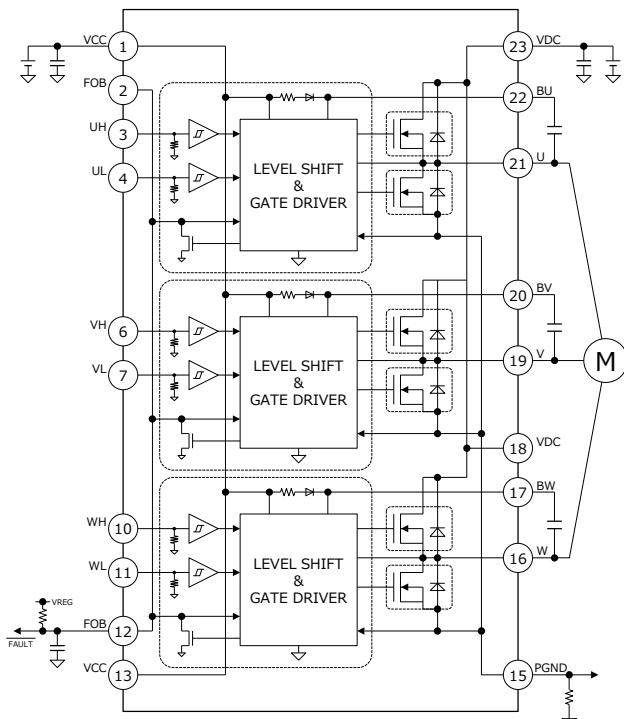


Figure 2. Block Diagram

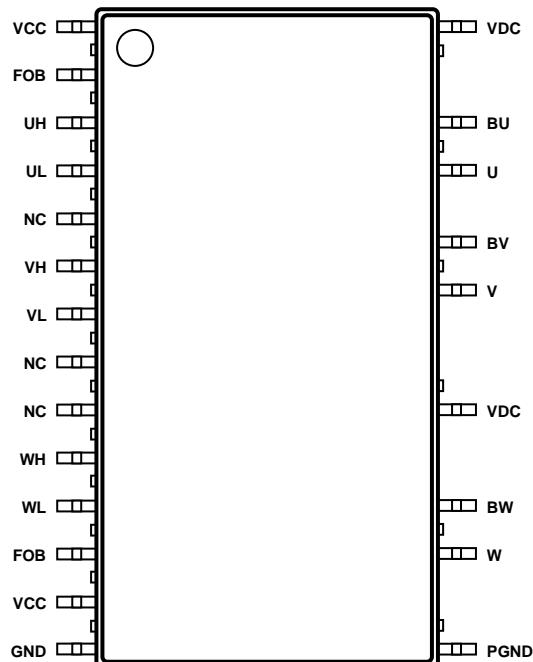


Figure 3. Pin Configuration (Top View)

Pin Description

Pin	Name	Function	Pin	Name	Function
1	VCC	Low voltage power supply	23	VDC	High voltage power supply
2	FOB	Fault signal output (open drain)	-	VDC	
3	UH	Phase U high side control input	22	BU	Phase U floating power supply
4	UL	Phase U low side control input	-	U	
5	NC	No connection	21	U	Phase U output
6	VH	Phase V high side control input	20	BV	Phase V floating power supply
7	VL	Phase V low side control input	-	V	
8	NC	No connection	19	V	Phase V output
9	NC	No connection	-	VDC	
10	WH	Phase W high side control input	18	VDC	High voltage power supply
11	WL	Phase W low side control input	17	BW	Phase W floating power supply
12	FOB	Fault signal output (open drain)	-	W	
13	VCC	Low voltage power supply	16	W	Phase W output
14	GND	Ground	15	PGND	Ground (current sense pin)

Note) All pin cut surfaces visible from the side of package are not connected, except the pin number is expressed as a “-”.

Description of Blocks

1. Control Input Pins (UH,UL,VH,VL,WH,WL)

The input threshold voltages of the control pins are 2.5V and 0.8V, with a hysteresis voltage of approximately 0.4V. The IC will accept input voltages up to the VCC voltage. When the same phase control pins are input high at the same time, the high side and low side gate driver outputs become low. Dead time is installed in the control signals. The control input pins are connected internally to pull-down resistors (100kΩ nominal). However, the switching noise on the output stage may affect the input on these pins and cause undesired operation. In such cases, attaching an external pull-down resistor (10kΩ recommended) between each control pin and ground, or connecting each pin to an input voltage of 0.8V or less (preferably GND), is recommended.

Truth Table

HIN	LIN	HO	LO
L	L	L	L
H	L	H	L
L	H	L	H
H	H	Inhibition	

Note) HIN: UH,VH,WH, LIN: UL,VL,WL

2. Under Voltage Lock Out (UVLO) Circuit

To secure the lowest power supply voltage necessary to operate the driver, and to prevent under voltage malfunctions, the UVLO circuits are independently built into the upper side floating driver and the lower side driver. When the supply voltage falls to V_{UVL} or below, the controller forces driver outputs low. When the voltage rises to V_{UVH} or above, the UVLO circuit ends the lockout operation and returns the chip to normal operation. Even if the controller returns to normal operation, the output begins from the following control input signal.

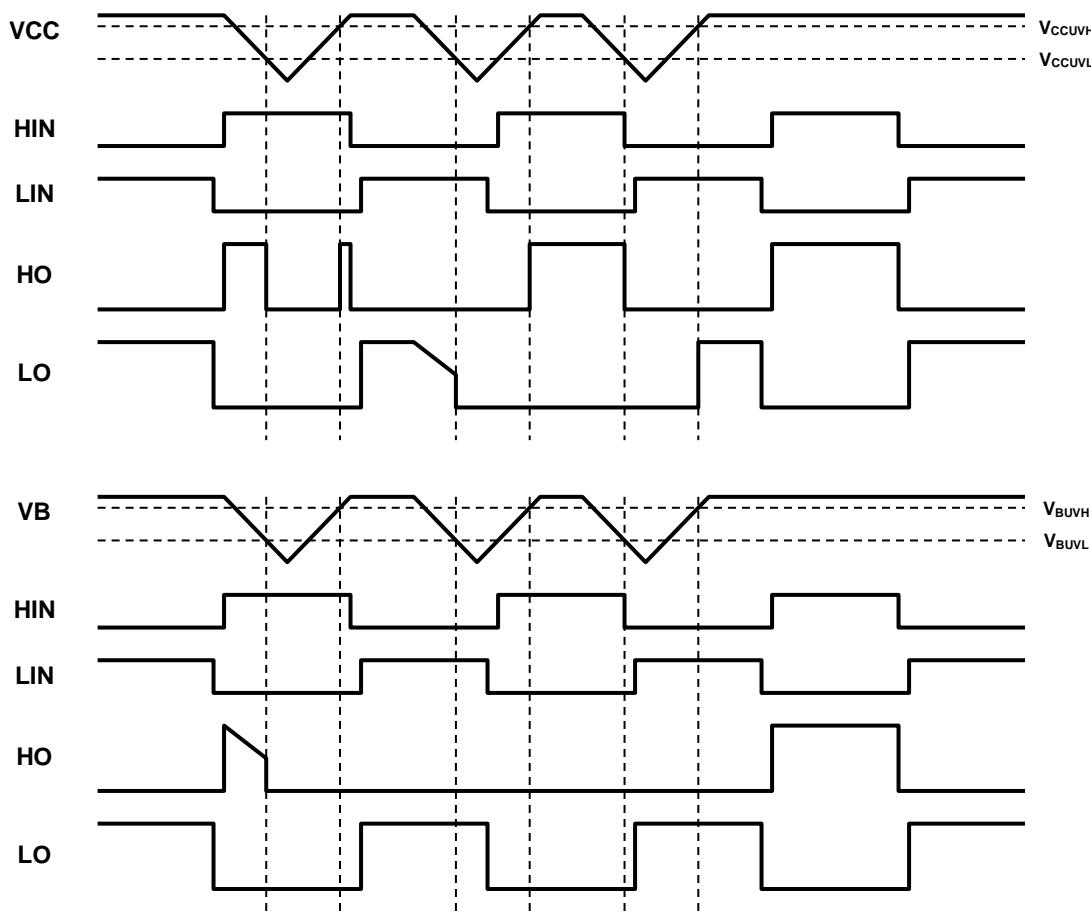


Figure 4. Low Voltage Monitor - UVLO - Timing Chart

Description of Blocks - continued

3. Bootstrap Operation

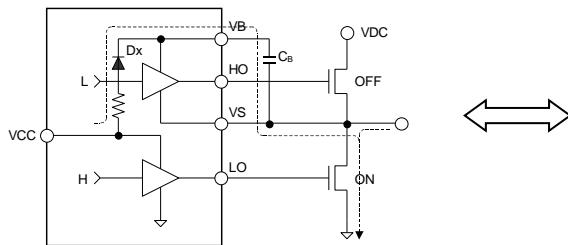


Figure 5. Charging Period

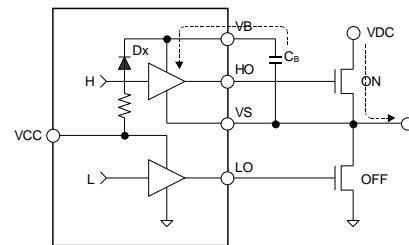


Figure 6. Discharging Period

The bootstrap is operated by the charge period and the discharge period being alternately repeated for bootstrap capacitor (CB) as shown in the figure above. In a word, this operation is repeated while the output of an external transistor is switching with synchronous rectification. Because the supply voltage of the floating driver is charged from the VCC power supply to CB through prevention of backflow diode DX, it is approximately (VCC-1V). The resistance series connection with DX has the impedance of approximately 200 Ω .

The capacitance value for the bootstrap is the following formula:

$$C_{BOOT} \gg \frac{\frac{(I_{BBQ} + I_{LBD})}{f_{PWM}} + 2 \times Q_g + Q_{LOSS}}{\Delta V_{DROP}} \approx 36nF$$

where:

I_{BBO} is the floating driver power supply quiescence current, 150 μ A(Max)

I_{BDQ} is the heating driver power supply quiescence current, I_{LBD} is the bootstrap diode reverse bias current, 10uA(Max)

f_{PWM} is the carrier frequency, 20kHz

Q_g is the output MOSFET total gate charge, 50nC(Max)

Q_{loss} is the floating driver transmission loss. 1nC(Max)

ΔV_{DROP} is the drop voltage of the floating driver power supply 3V

The allowed drop voltage actually becomes smaller by the range of the used power supply voltage, the output MOSFET ON resistance, the forward voltages of the internal boot diode (the drop voltage to the capacitor by the charge current), and the power supply voltage monitor circuits etc. Please set the calculation value to the criterion about the capacitance value tenfold or more to secure the margin in consideration of temperature characteristics and the value change, etc. Moreover, the example of the mentioned above assumes the synchronous rectification switching. Because the total gate charge is needed only by the carrier frequency in the upper switching section, for example 150° commutation driving, it becomes a great capacity shortage in the above settings. Set it after confirming actual application operation.

4. Thermal Shutdown (TSD) Circuit

The TSD circuit operates when the junction temperature of the gate driver exceeds the preset temperature (150°C nominal). At this time, the controller forces all driver outputs low. Since thermal hysteresis is provided in the TSD circuit, the chip returns to normal operation when the junction temperature falls below the preset temperature (125°C nominal). The TSD circuit is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation in the presence of extreme heat. Do not continue using the IC after the TSD circuit is activated, and do not use the IC in an environment where activation of the circuit is assumed. Moreover, it is not possible to follow the output MOSFET junction temperature rising rapidly because it is a gate driver chip that monitors the temperature and it is likely not to function effectively.

5. Overcurrent Protection (OCP) Circuit

The overcurrent protection circuit can be activated by connecting a low value resistor for current detection between the PGND pin and the GND pin. When the PGND pin voltage reaches or surpasses the threshold value (0.9V typical), the gate driver outputs low to the gate of all output MOSFETs, thus initiating the overcurrent protection operation.

Description of Blocks - continued

6. Fault Signal Output

When the gate driver detects either state that should be protected (UVLO / TSD / OCP), the FOB pin outputs low (open drain) for at least 25μs nominal. The FOB pin has wired-OR connection with each phase gate driver chip internally, and into another phase also entering the protection operation. Even when this function is not used, the FOB pin is pull-up to the voltage of 3V or more and at least a resistor with a value 10kΩ or more. Moreover, the signal from the outside of the chip is not passed because of the built-in analog filter, but the internal control signals (UVLO / TSD / OCP) pass the filter (2.0μs Min) for the malfunction prevention by the switching noise, etc.

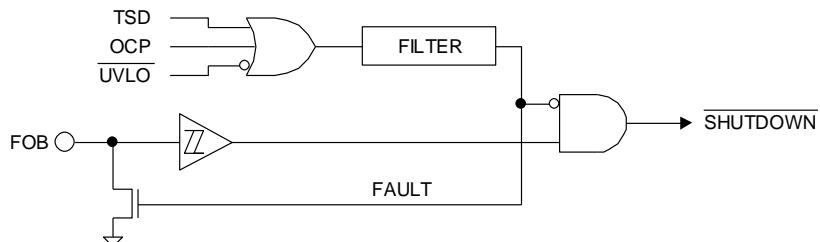


Figure 7. Fault Signal Bi-Directional Input Pin Interface

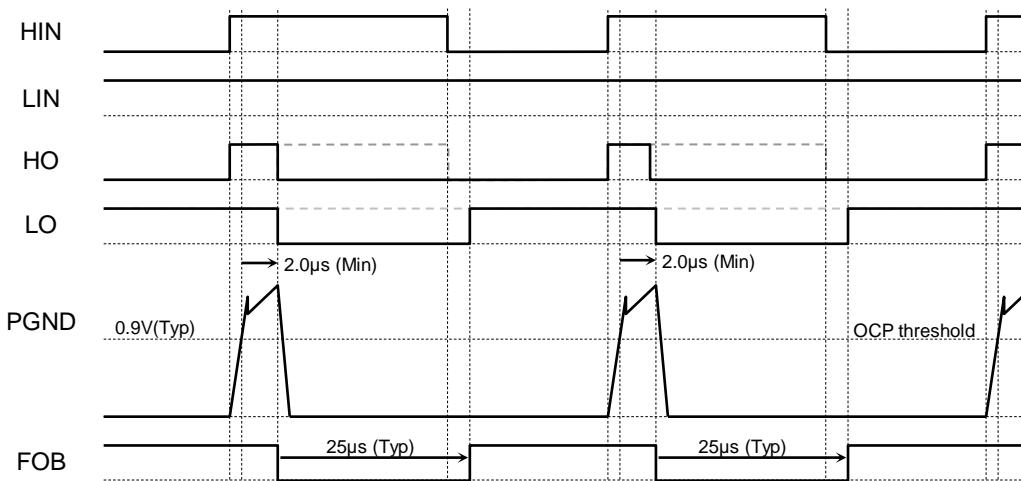


Figure 8. Fault Operation ~ OCP ~ Timing Chart

The release time from the protection operation can be changed by inserting an external capacitor. Refer to the formula below. Release time of 2ms or more is recommended.

$$t = -\ln\left(1 - \frac{2.0}{V_{PU}}\right) \cdot R \cdot C \quad [\text{s}]$$

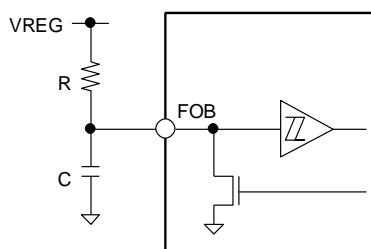


Figure 9. Release Time Setting Application Circuit

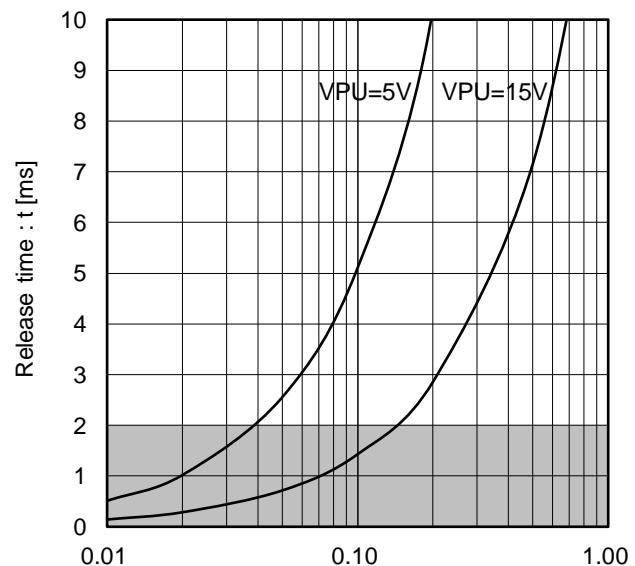


Figure 10. Release Time (Reference Data @ R=100kΩ)

6. Fault Signal Output - continued

When using controller BD6201x series as a control IC, the FOB pin can be linked to the external fault signal input pin of the side of the control IC since it has the internal pull-up resistor. Refer to figure 11.

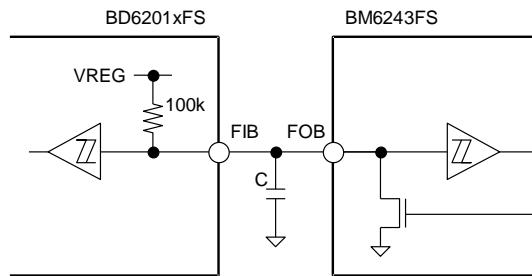


Figure 11. Interface Equivalent Circuit

7. Switching Time

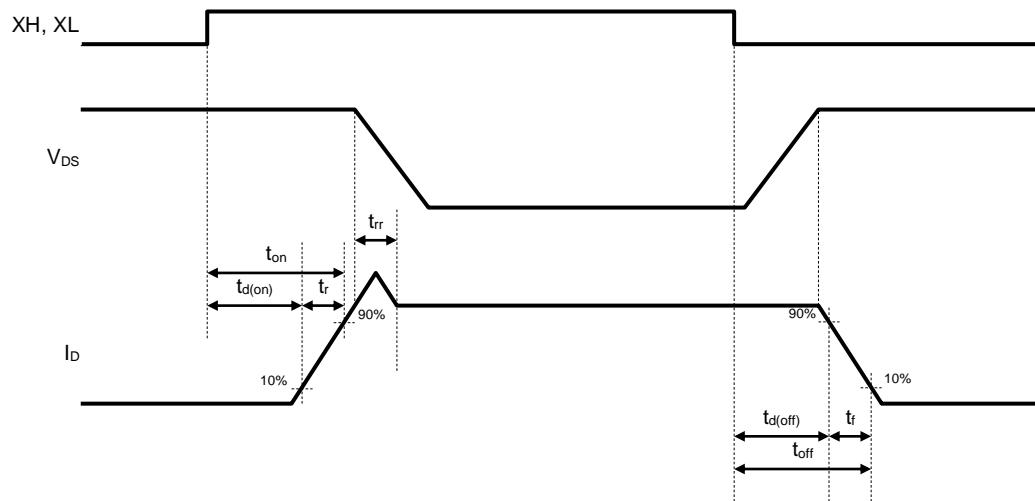


Figure 12. Switching Time Definition

Parameter	Symbol	Reference	Unit	Conditions
High Side Switching Time	$t_{dH(on)}$	950	ns	VDC=300V, VCC=15V, $I_D=1.25A$ Inductive load
	t_{rH}	150	ns	
	t_{rrH}	220	ns	
	$t_{dH(off)}$	490	ns	
	t_{fH}	20	ns	
Low Side Switching Time	$t_{dL(on)}$	870	ns	The propagation delay time: Internal gate driver input stage to the driver IC output.
	t_{rL}	145	ns	
	t_{rrL}	160	ns	
	$t_{dL(off)}$	555	ns	
	t_{fL}	30	ns	

Absolute Maximum Ratings (T_j=25°C)

Parameter	Symbol	Ratings	Unit
Output MOSFET	V _{DSS}	600	V
Supply Voltage	V _{DC}	-0.3 to +600	V
Output Voltage	V _U , V _V , V _W	-0.3 to +600	V
High Side Supply Pin Voltage	V _{BU} , V _{BV} , V _{BW}	-0.3 to +600	V
High Side Floating Supply Voltage	V _{BU} -V _U , V _{BV} -V _V , V _{BW} -V _W	-0.3 to +20	V
Low Side Supply Voltage	V _{CC}	-0.3 to +20	V
All Others	V _{I/O}	-0.3 to +V _{CC}	V
Driver Outputs (DC)	I _{OMAX(DC)}	±2.5	A
Driver Outputs (Pulse)	I _{OMAX(PLS)}	±4.0 ^(Note 1)	A
Fault Signal Output	I _{OMAX(FOB)}	15	mA
Storage Temperature	T _{STG}	-55 to +150	°C
Maximum Junction Temperature	T _{jmax}	150	°C

(Note) All voltages are with respect to ground unless otherwise specified.

(Note 1) P_w ≤ 10μs, Duty cycle ≤ 1%

Caution1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance ^(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 3)	1s	
SSOP-A54_23				
Junction to Ambient	θ _{JA}	41.7		°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ _{JT}	10		°C/W

(Note 1) Based on JESD51-2A(Still-Air)

(Note 2) Refer to Figure 13. for temperature measurement point on the component package top surface.

(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mm
Top		
Copper Pattern	Thickness	
Footprints and Traces	70μm	

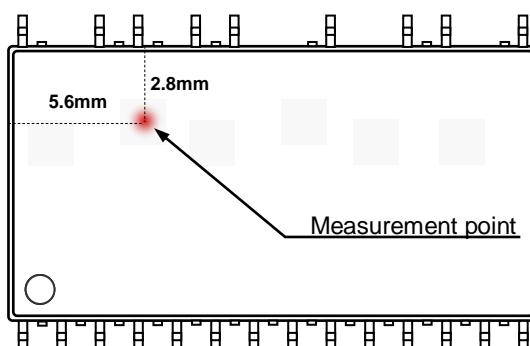


Figure 13. Temperature Measurement Point

Recommended Operating Conditions (T_j=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DC}	-	310	400	V
High Side Floating Supply Voltage	V _{BU} -V _U , V _{BV} -V _V , V _{BW} -V _W	13.5	15	16.5	V
Low Side Supply Voltage	V _{CC}	13.5	15	16.5	V
Bootstrap Capacitor	C _B	1.0	-	-	μF
VCC Bypass Capacitor	C _{VCC}	1.0	-	-	μF
Minimum Input Pulse Width	t _{MIN}	0.8	-	-	μs
Dead Time	t _{DT}	1.5	-	-	μs
Shunt Resistor (PGND)	R _S	0.5	-	-	Ω
Junction Temperature	T _j	-40	-	+125	°C

(Note) All voltages are with respect to ground unless otherwise specified.

Electrical Characteristics (Driver part, Unless otherwise specified V_{CC}=15V and T_j=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply						
HS Quiescence Current	I _{BBQ}	30	70	150	μA	XH=XL=L, each phase
LS Quiescence Current	I _{CCQ}	0.2	0.7	1.3	mA	XH=XL=L
Output MOSFET						
D-S Breakdown Voltage	V _{(BR)DSS}	600	-	-	V	I _D =1mA, XH=XL=L
Leak Current	I _{DSS}	-	-	100	μA	V _{DS} =600V, XH=XL=L
DC On Resistance	R _{DS(ON)}	-	1.7	2.5	Ω	I _D =1.25A
Diode Forward Voltage	V _{SD}	-	1.1	1.5	V	I _D =1.25A
Bootstrap Diode						
Leak Current	I _{LBD}	-	-	10	μA	V _{BX} =600V
Forward Voltage	V _{FBD}	1.5	1.8	2.1	V	I _{BD} =-5mA with series-res.
Series Resistance	R _{BD}	-	200	-	Ω	
Control Inputs						
Input Bias Current	I _{XIN}	30	50	70	μA	V _{IN} =5V
Input High Voltage	V _{XINH}	2.5	-	VCC	V	
Input Low Voltage	V _{XINL}	0	-	0.8	V	
Under Voltage Lock Out						
High Side Release Voltage	V _{BUVH}	9.5	10.0	10.5	V	V _{BX} - V _X
High Side Lockout Voltage	V _{BUVL}	8.5	9.0	9.5	V	V _{BX} - V _X
Low Side Release Voltage	V _{CCUVH}	11.0	11.5	12.0	V	
Low Side Lockout Voltage	V _{CCUVL}	10.0	10.5	11.0	V	
Over Current Protection						
Threshold Voltage	V _{SNS}	0.8	0.9	1.0	V	
Fault Output						
Output Low Voltage	V _{FOL}	-	-	0.8	V	I _O =+10mA
Input High Voltage	V _{FINH}	2.5	-	VCC	V	
Input Low Voltage	V _{FINL}	0	-	0.8	V	
Noise Masking Time	t _{MASK}	2.0	-	-	μs	

(Note) All voltages are with respect to ground unless otherwise specified.

Typical Performance Curves (Reference Data)

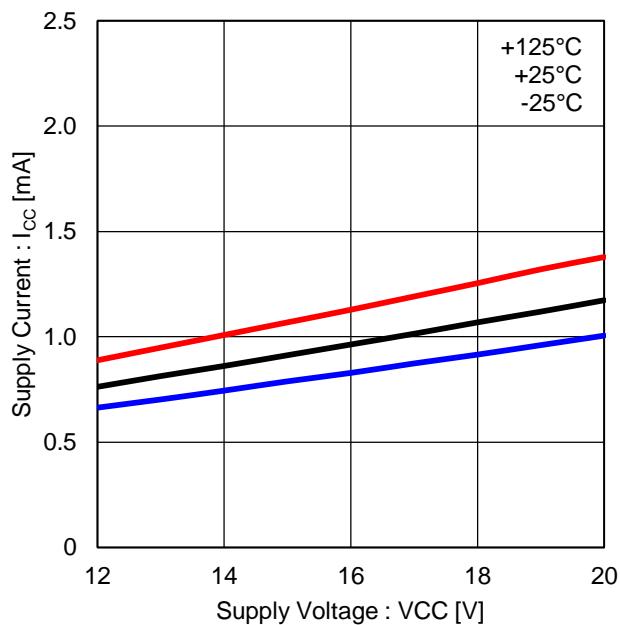


Figure 14. Quiescence Current (Low Side Drivers)

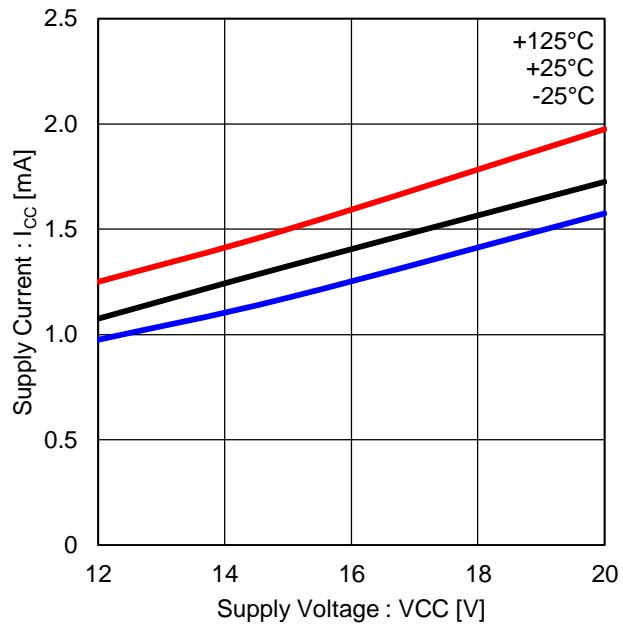
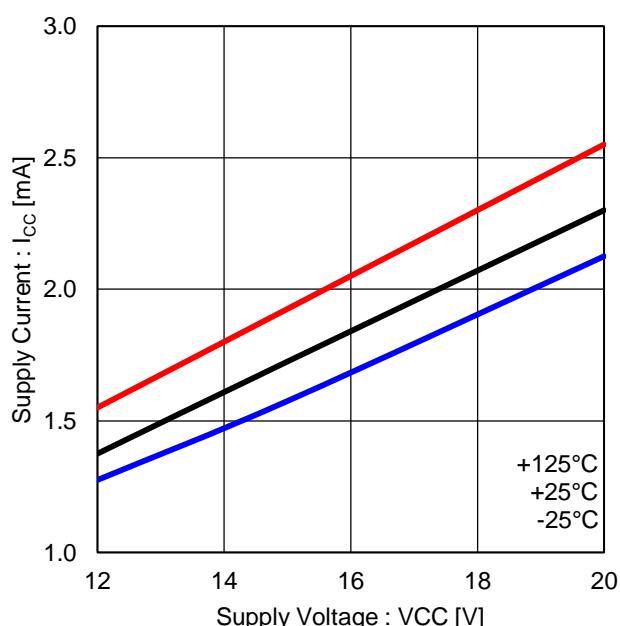
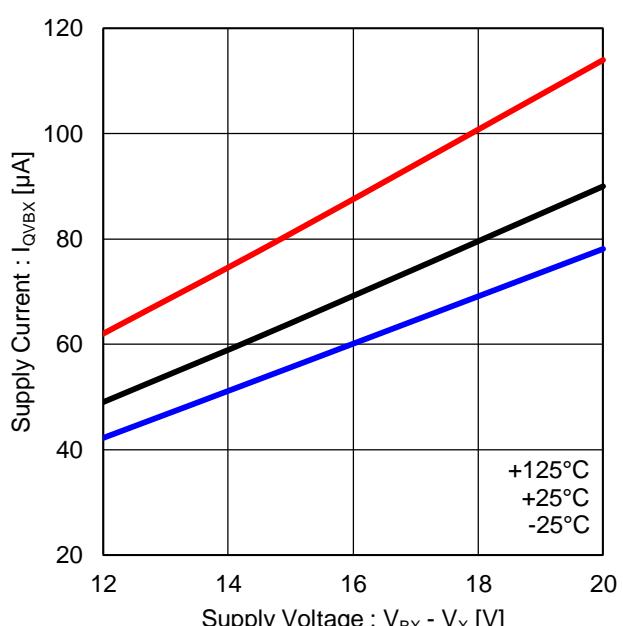
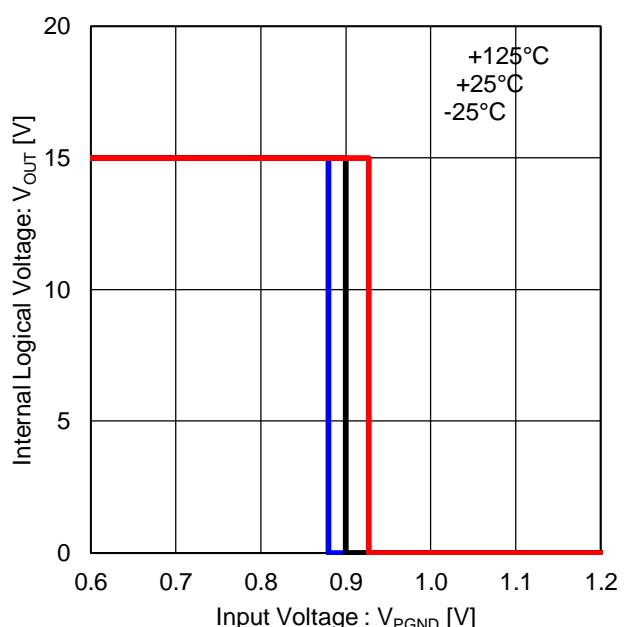
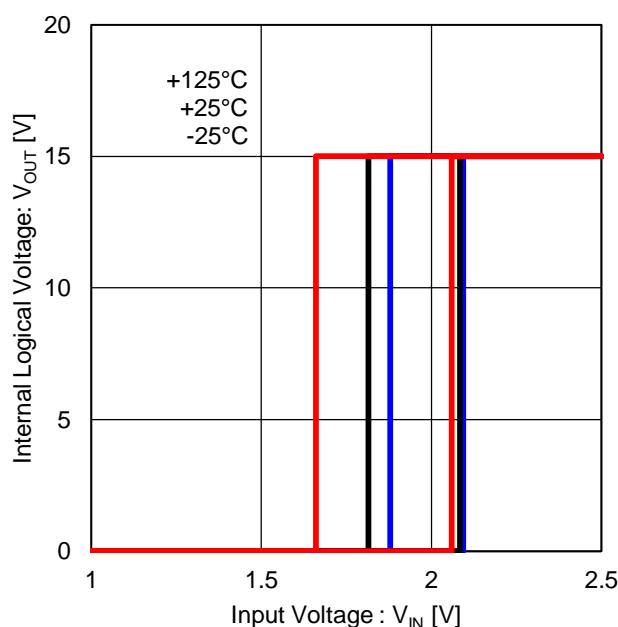
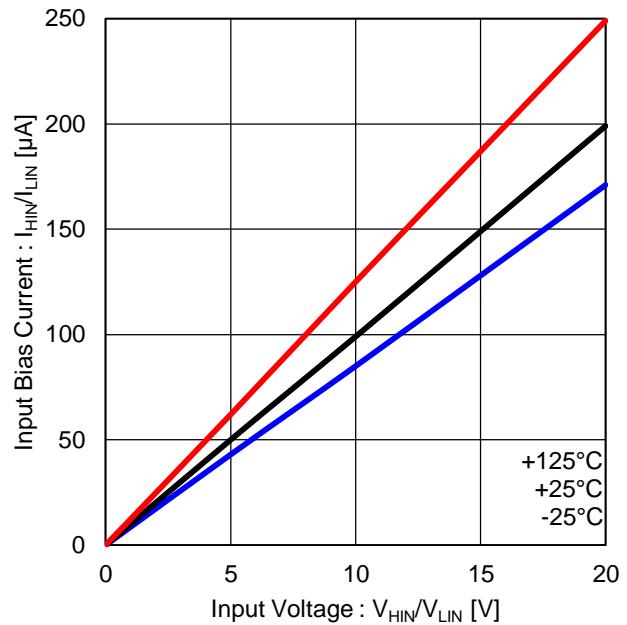
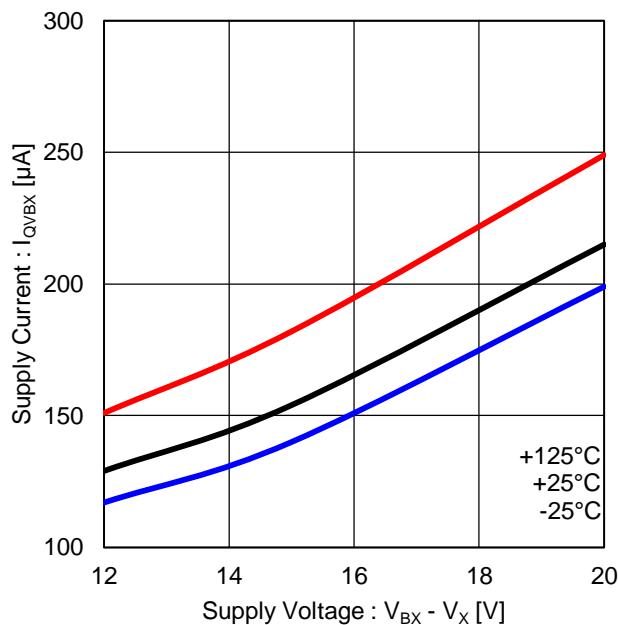
Figure 15. Low Side Drivers Operating Current (f_{PWM}: 20kHz, One-Phase Switching)Figure 16. Low Side Drivers Operating Current (f_{PWM}: 20kHz, Two-Phase Switching)

Figure 17. Quiescence Current (High Side Driver, Each Phase)

Typical Performance Curves (Reference Data) - continued



Typical Performance Curves (Reference Data) - continued

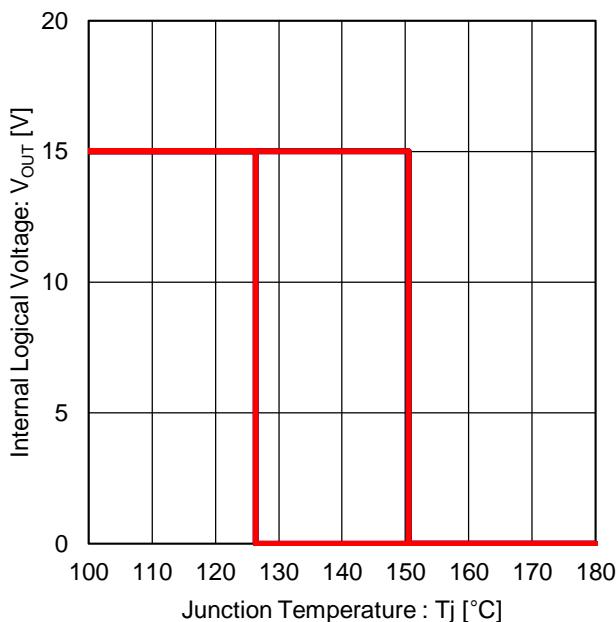


Figure 22. Thermal Shut Down

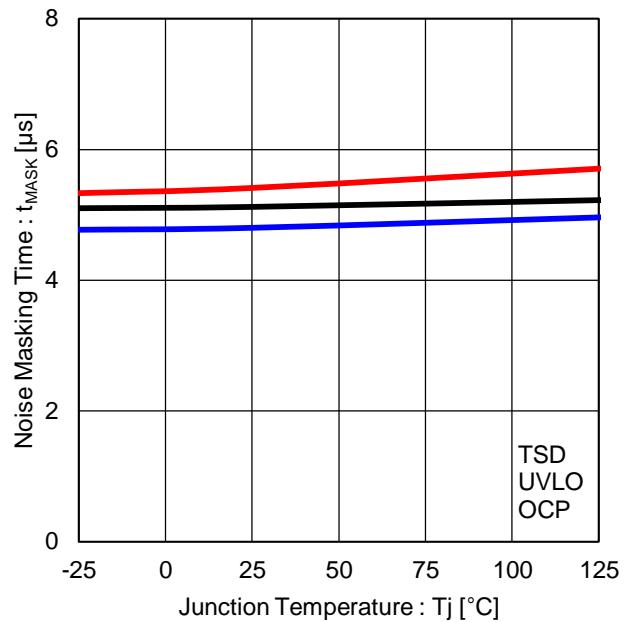


Figure 23. Noise Masking Time

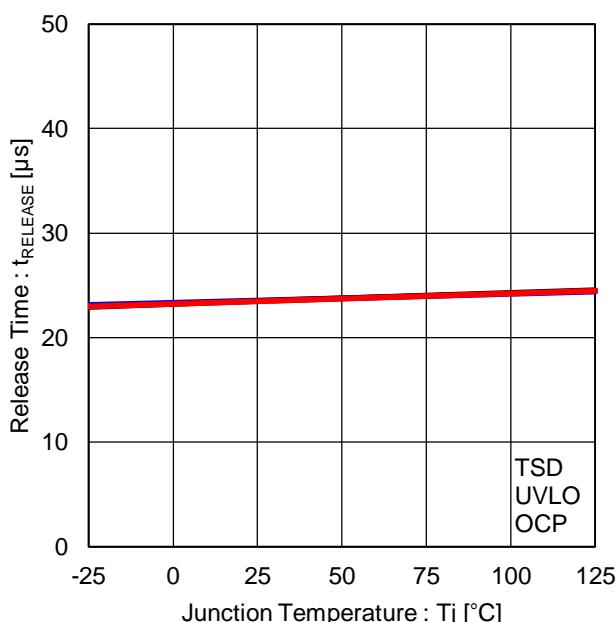


Figure 24. Release Time (No External Capacitor)

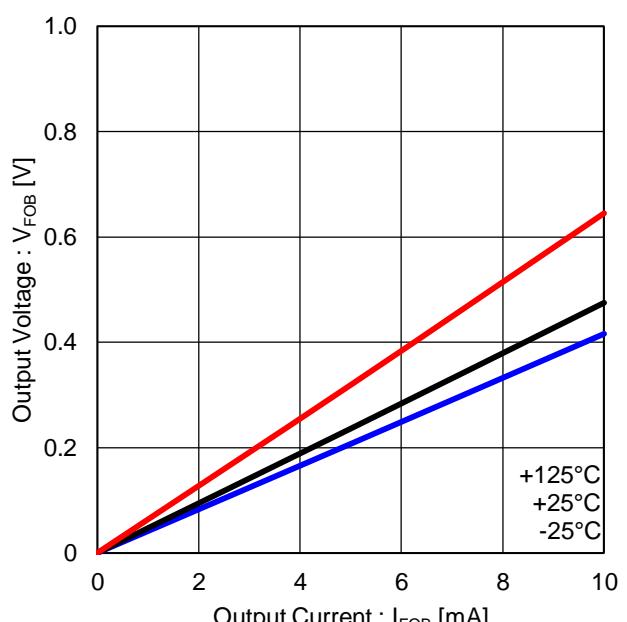


Figure 25. Fault Output ON Resistance

Typical Performance Curves (Reference Data) - continued

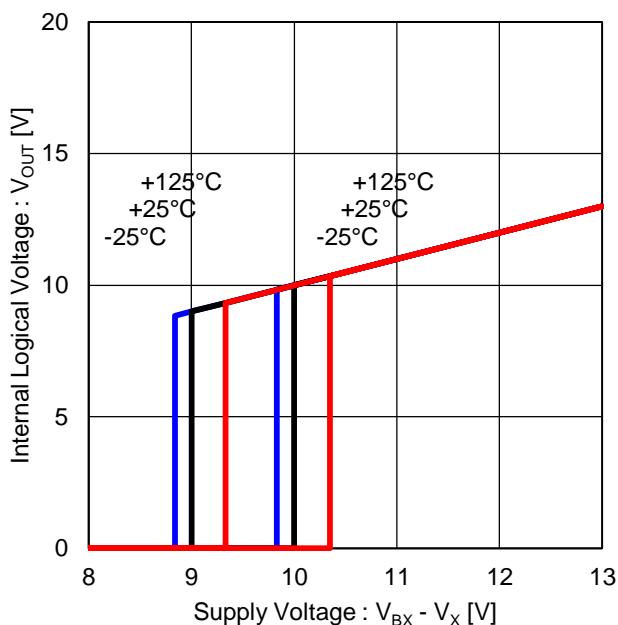


Figure 26. Under Voltage Lock Out (High side Driver)

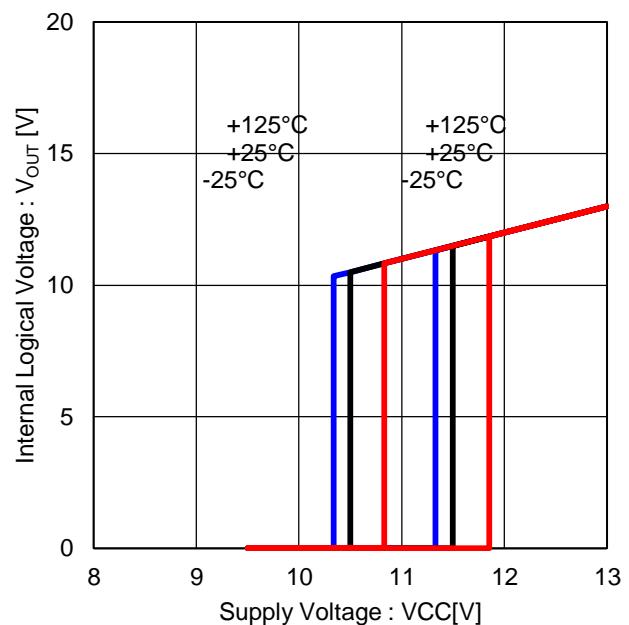


Figure 27. Under Voltage Lock Out (Low Side Drivers)

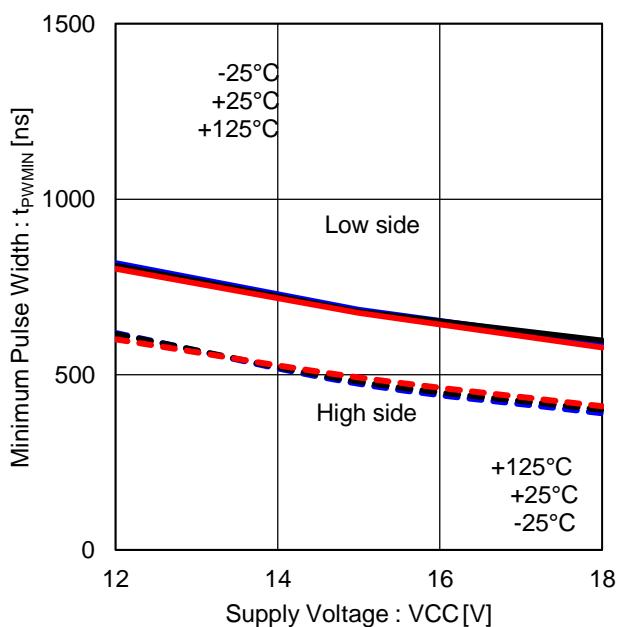


Figure 28. Minimum Input Pulse Width

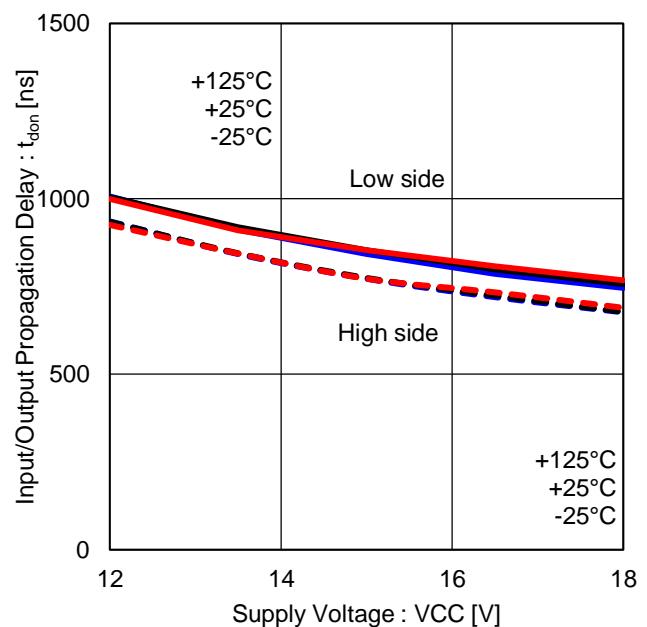


Figure 29. Input/Output Propagation Delay (On delay)

Typical Performance Curves (Reference Data) - continued

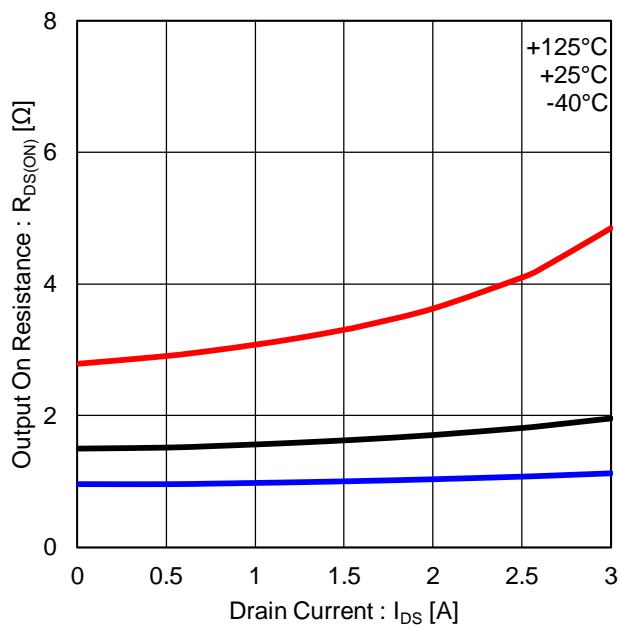


Figure 30. Output MOSFET ON Resistance

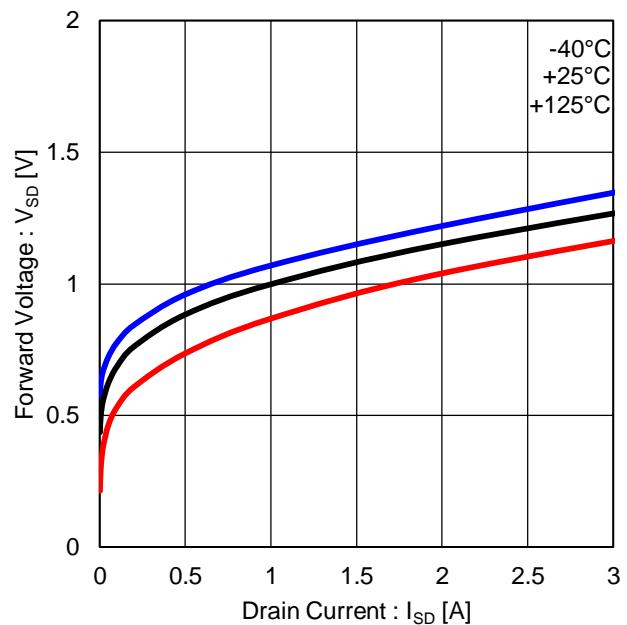


Figure 31. Output MOSFET Body Diode

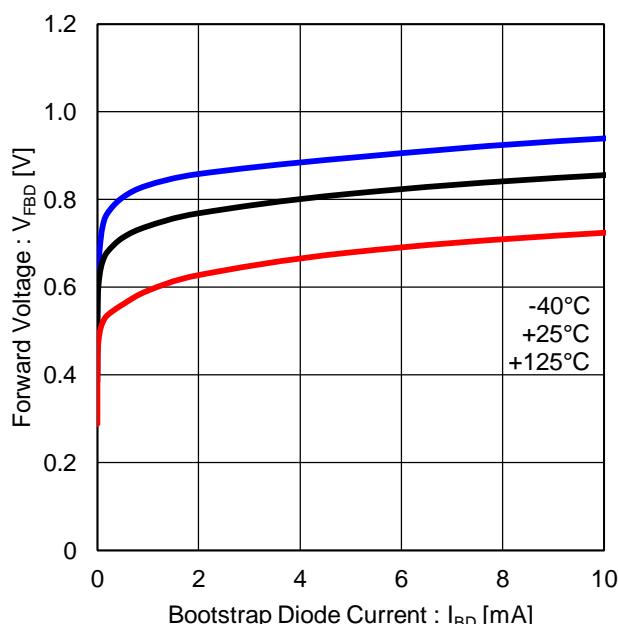


Figure 32. Bootstrap Diode Forward Voltage

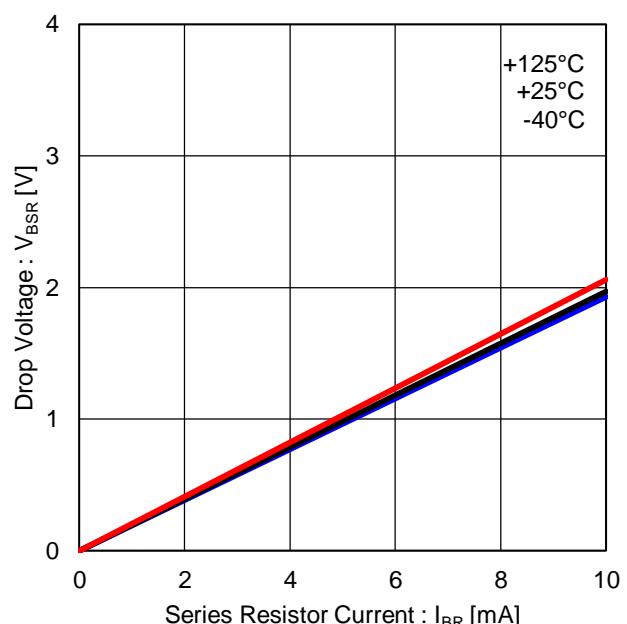
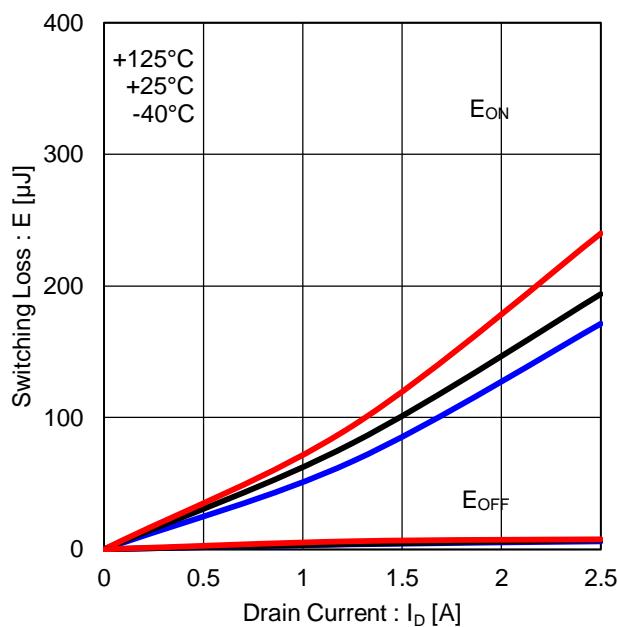
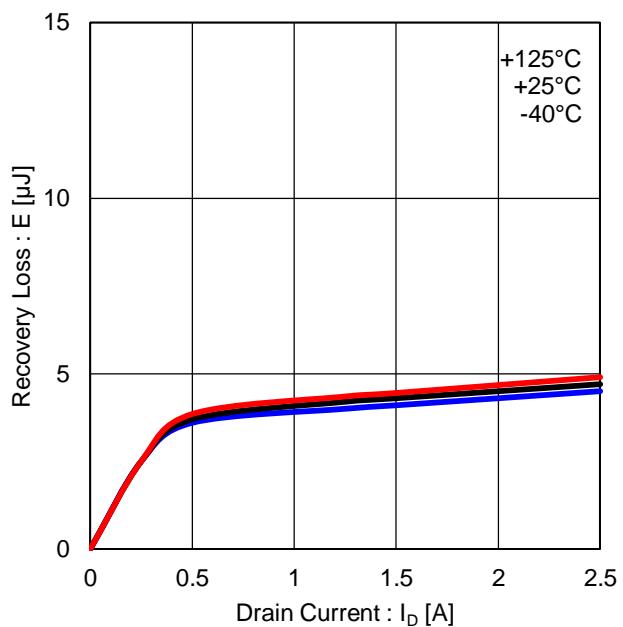
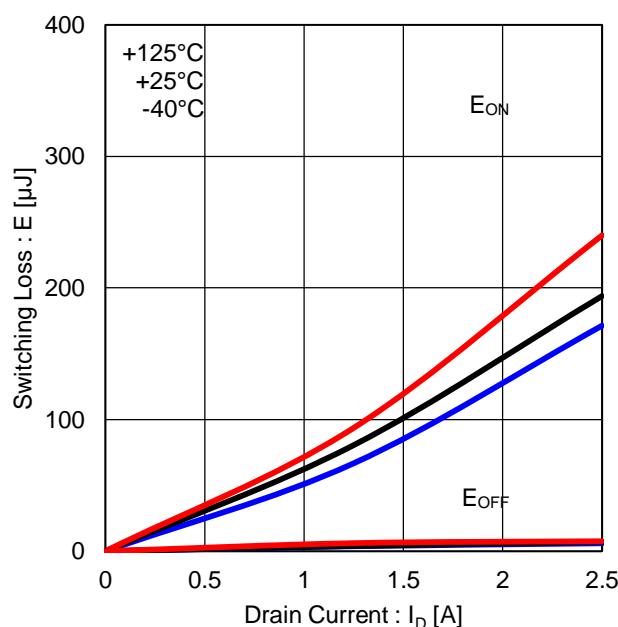
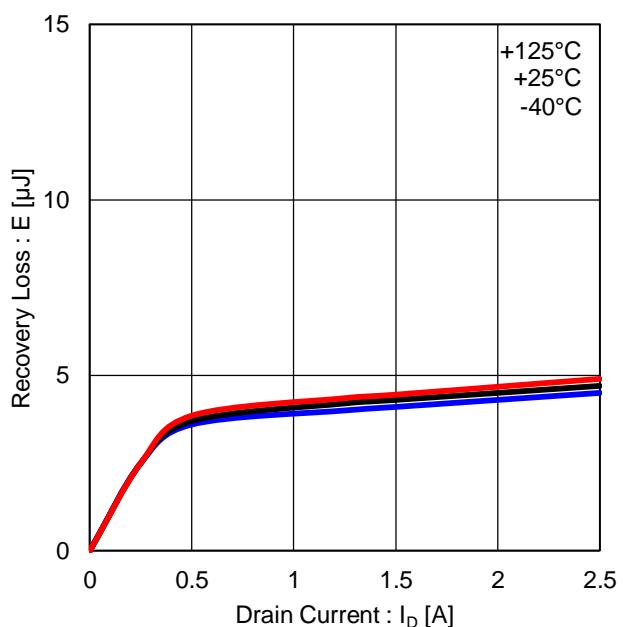


Figure 33. Bootstrap Series Resistor

Typical Performance Curves (Reference Data) - continued

Figure 34. High Side Switching Loss
(VDC=300V)Figure 35. High Side Recovery Loss
(VDC=300V)Figure 36. Low Side Switching Loss
(VDC=300V)Figure 37. Low Side Recovery Loss
(VDC=300V)

Application Example

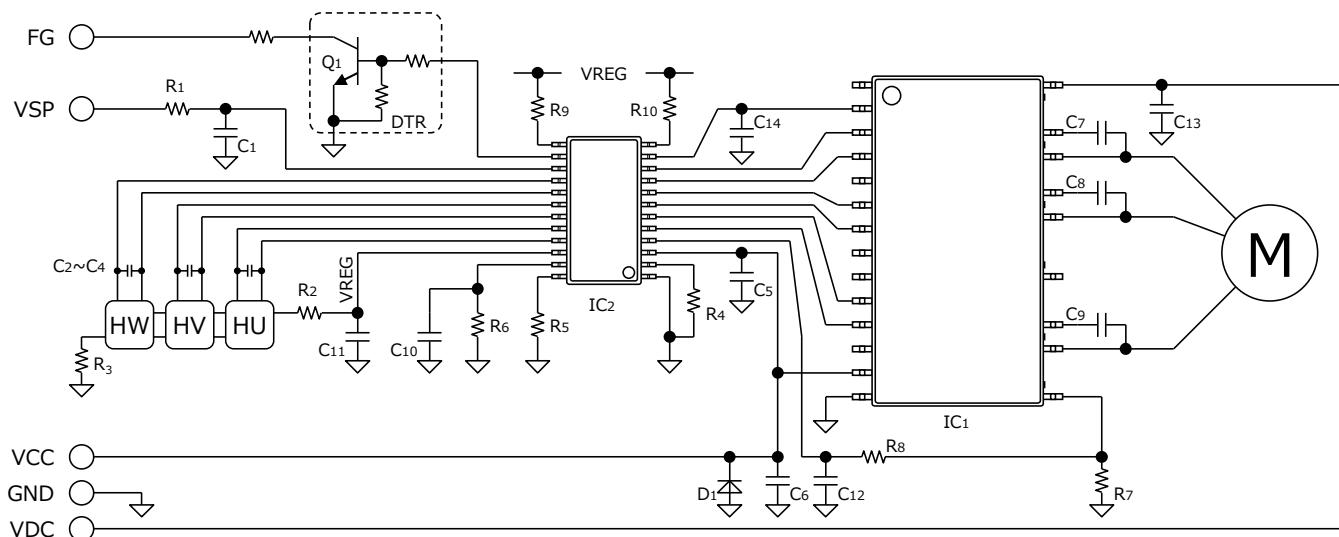
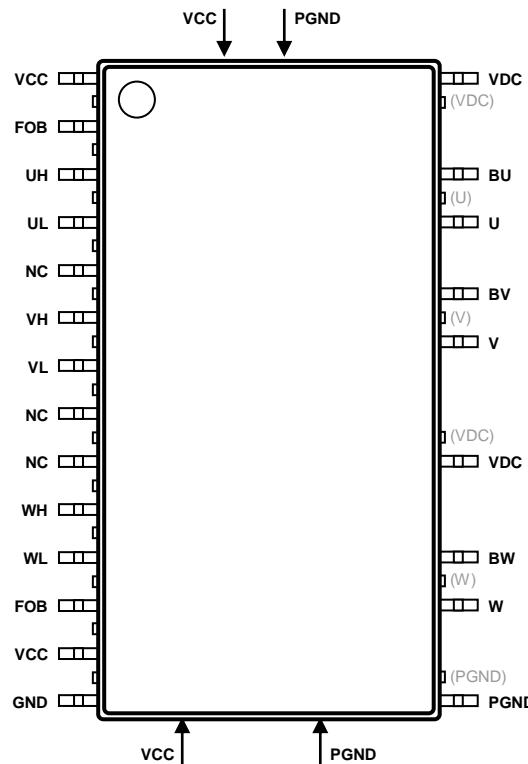


Figure 38. Application Example (180° Sinusoidal Commutation Controller + BM6243FS)

Parts List

Parts	Value	Manufacturer	Type	Parts	Value	Ratings	Type
IC ₁	-	ROHM	BM6243FS	C ₁	0.1μF	50V	Ceramic
IC ₂	-	ROHM	BD62018AFS	C ₂	2200pF	50V	Ceramic
R ₁	1kΩ	ROHM	MCR18EZPF1001	C ₃	2200pF	50V	Ceramic
R ₂	150Ω	ROHM	MCR18EZPJ151	C ₄	2200pF	50V	Ceramic
R ₃	150Ω	ROHM	MCR18EZPJ151	C ₅	10 μF	50V	Ceramic
R ₄	20kΩ	ROHM	MCR18EZPF2002	C ₆	10 μF	50V	Ceramic
R ₅	100kΩ	ROHM	MCR18EZPF1003	C ₇	2.2μF	50V	Ceramic
R ₆	100kΩ	ROHM	MCR18EZPF1003	C ₈	2.2μF	50V	Ceramic
R ₇	0.5Ω	ROHM	MCR50JZHFL1R50 // 3	C ₉	2.2μF	50V	Ceramic
R ₈	10kΩ	ROHM	MCR18EZPF1002	C ₁₀	0.1μF	50V	Ceramic
R ₉	0Ω	ROHM	MCR18EZPJ000	C ₁₁	2.2μF	50V	Ceramic
R ₁₀	0Ω	ROHM	MCR18EZPJ000	C ₁₂	100pF	50V	Ceramic
Q ₁	-	ROHM	DTC124EUA	C ₁₃	0.1μF	630V	Ceramic
D ₁	-	ROHM	KDZ20B	C ₁₄	0.1μF	50V	Ceramic
				HX	-	-	Hall elements

Dummy Pin Descriptions



Dummy pins handling inside the package

- VCC pins, 1pin and 12pin are electrically connected in the inner lead frame.
- FOB pins, 2pin and 13pin are electrically connected in the inner lead frame.
- VDC pins, 18pin and 23pin are electrically connected in the inner lead frame.

Figure 39. Dummy Pins

I/O Equivalent Circuits

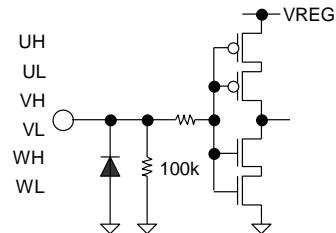


Figure 40.UH,UL,VH,VL,WH,WL

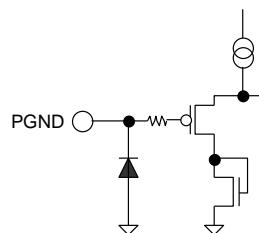


Figure 41. PGND

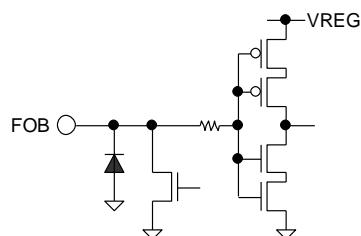


Figure 42. FOB

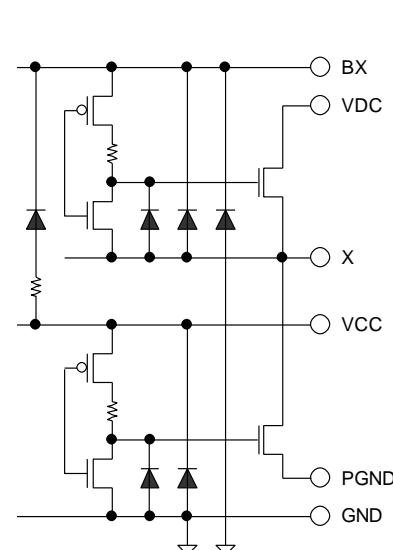


Figure 43. VCC, GND, VDC, BX(BU/BV/BW), X(U/V/W)

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

Do not force voltage to the input pins when the power does not supply to the IC. Also, do not force voltage to the input pins that exceed the supply voltage or in the guaranteed the absolute maximum rating value even if the power is supplied to the IC.

When using this IC, the high voltage pins VDC, BU/U, BV/V and BW/W need a resin coating between these pins. It is judged that the inter-pins distance is not enough. If any special mode in excess of absolute maximum ratings is to be implemented with this product or its application circuits, it is important to take physical safety measures, such as providing voltage-clamping diodes or fuses. And, set the output transistor so that it does not exceed absolute maximum ratings or ASO. In the event a large capacitor is connected between the output and ground, and if VCC and VDC are short-circuited with 0V or ground for any reason, the current charged in the capacitor flows into the output and may destroy the IC.

This IC contains the controller chip, P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

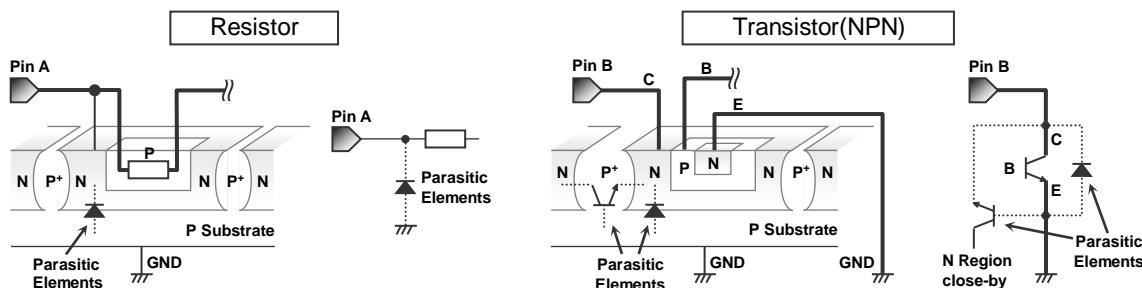
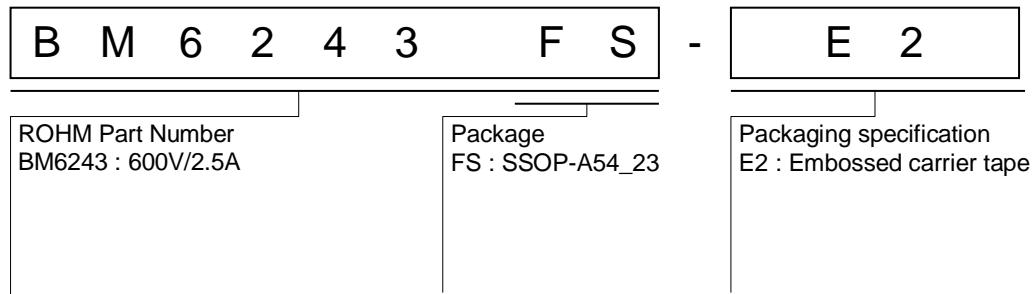


Figure 44. Example of IC structure

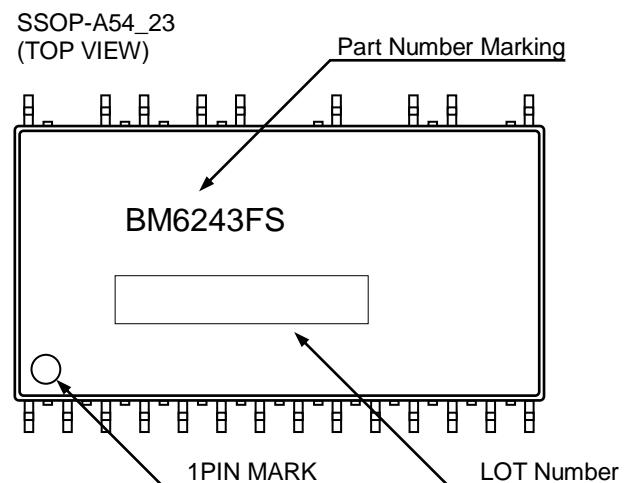
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

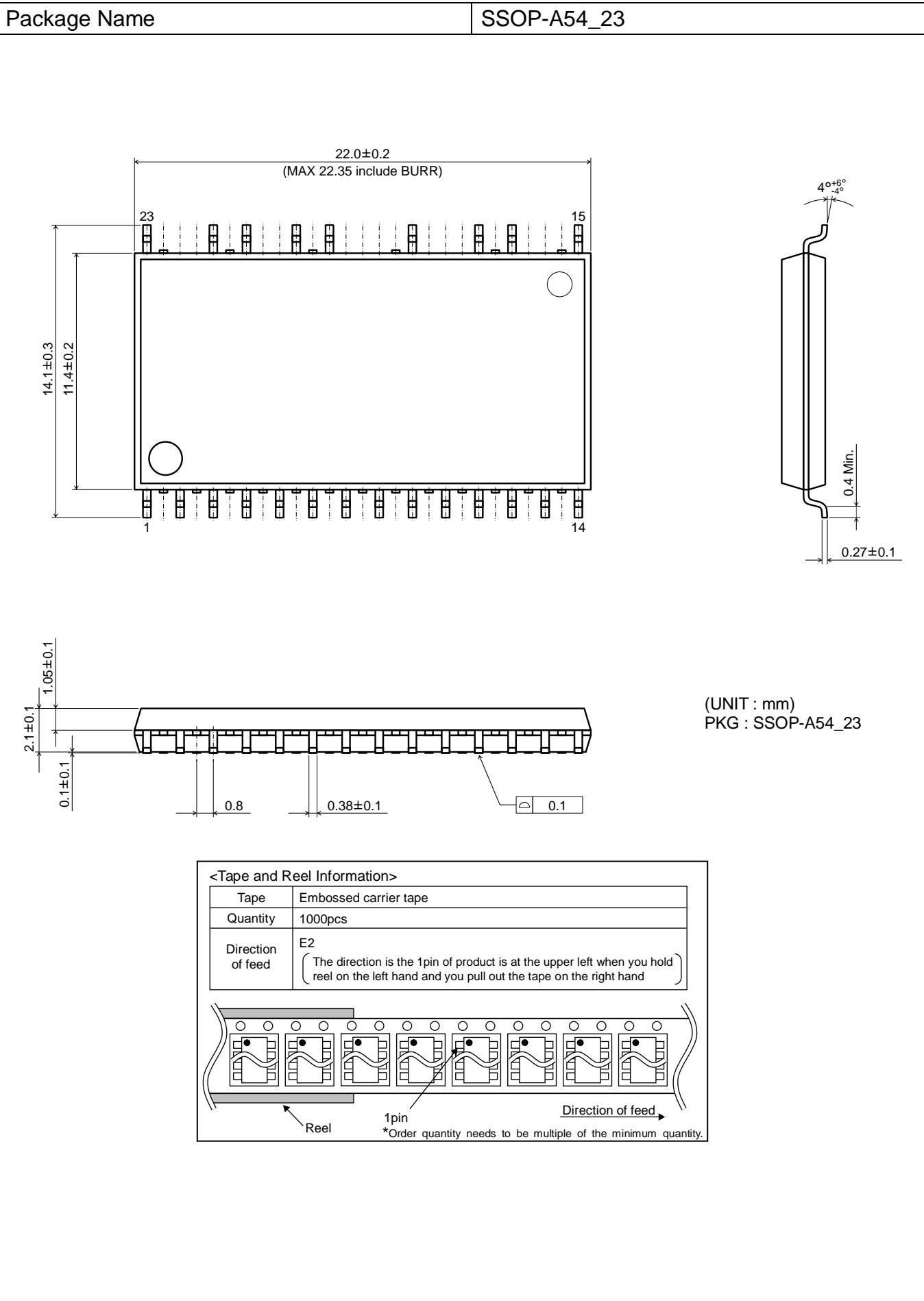
Ordering Information



Marking Diagrams



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
06.Jul.2018	001	New Release

Notice

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
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Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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