Datasheet

System Power IC Series for TFT-LCD Panel

I2C Control Multi-channel System Power Supply IC

BM81006MWW

General Description

BM81006MWW is a system power supply for TFT-LCD. It generates required bias voltage for source driver, T-con and Gate driver: VDD1, VDD2, VDD3, AVDD, HAVDD, VGH, VGL, VCLP, VCLN, VCOM, GAMMA and GPM.
I2C BUS control enables free setting of output voltage and sequences.

Key Specifications

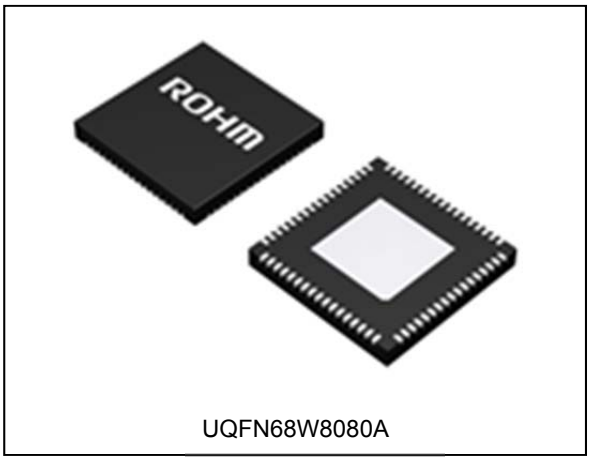
- VIN Input Voltage Range: 9.1V to 14.7V
- AVDD Output Voltage Range: VIN×1.06V to 19.4V
- HAVDD Output Voltage Range: 6.75V to 9.70V
- VGH Output Voltage Range: 15.0V to 45.0V
- VGL Output Voltage Range: -2.0V to -22.0V
- Switching Frequency: 750kHz(Typ)
- Operating Temperature Range: -40°C to +105°C

Features

- Asynchronous Buck Converter for VDD x3
- Asynchronous Boost Converter for AVDD
- Synchronous Buck Converter with Built-in FET for HAVDD
- Asynchronous Boost Converter for VGH
- VGH Low Temperature Compensation Function
- Asynchronous Inverting Converter for VGL
- Negative Output Amplifier for VCLN
- GPM(Gate Pulse Modulation) Function
- GPM Positive Clamp Voltage Regulator
- Amplifier for VCOM x2
- VCOM DVR(Digital Variable Range) Function (with 7bit EEPROM)
- Programmable Gamma Amplifier with 8bit DAC x4
- Built-in Reset Function
- Sequence Control Function
- Soft-start Function
- I2C BUS Control
- Protection Circuits:
  - Under Voltage Lockout Protection (UVLO)
  - Thermal Shutdown Protection (TSD)
  - Timer-Latch Type Short Circuit Protection (SCP)
  - Over Voltage Protection (OVP)
  - Over Current Protection (OCP)

Package

	W(Typ) x D(Typ) x H (Max)
UQFN68W8080A	8.0mm x 8.0mm x 0.8mm



UQFN68W8080A

Application

TFT-LCD Panel

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Typical Application Circuit

(TOP VIEW)

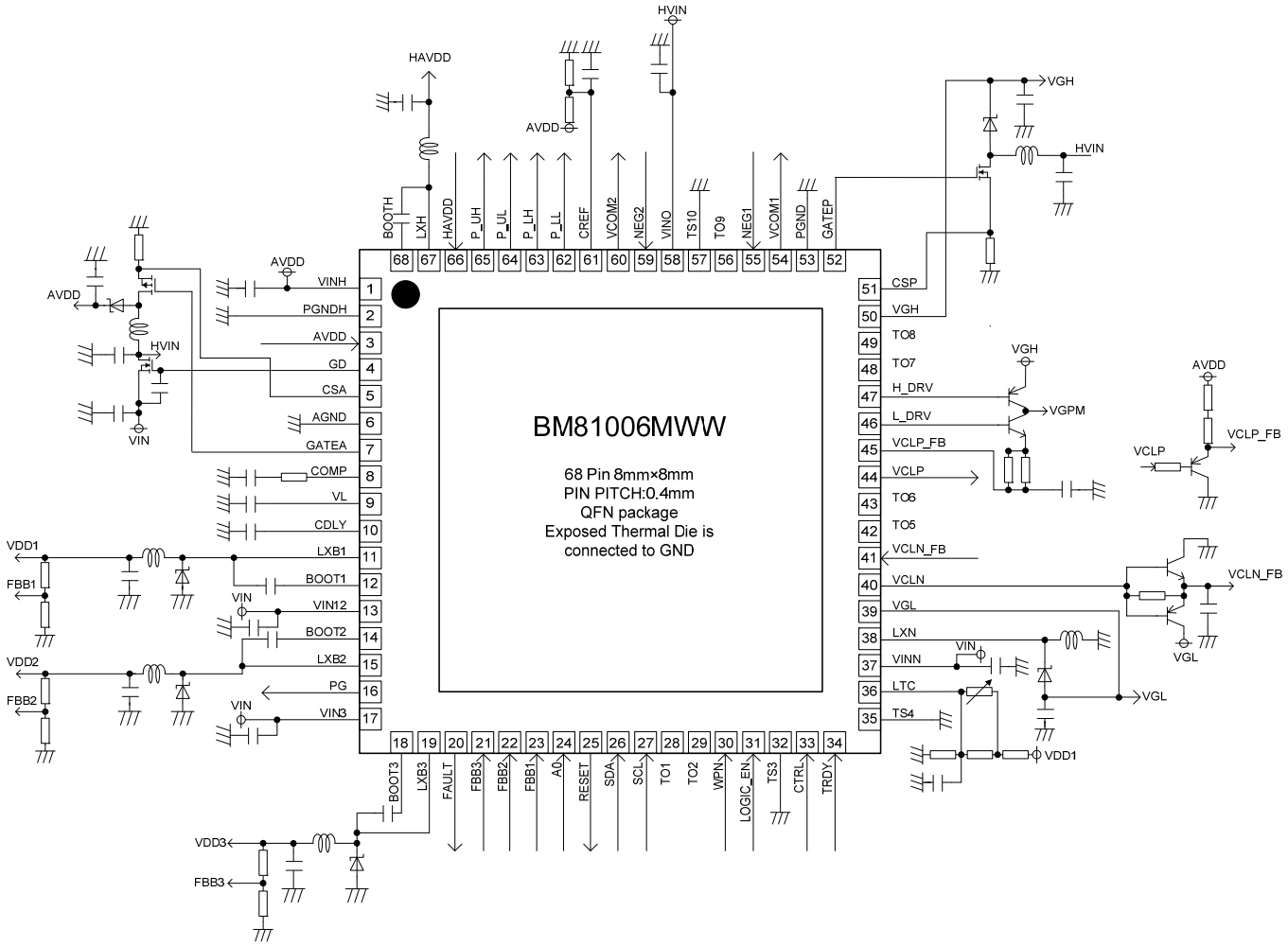


Figure 1. Application Circuit

Contents

Pin Configuration

(TOP VIEW)

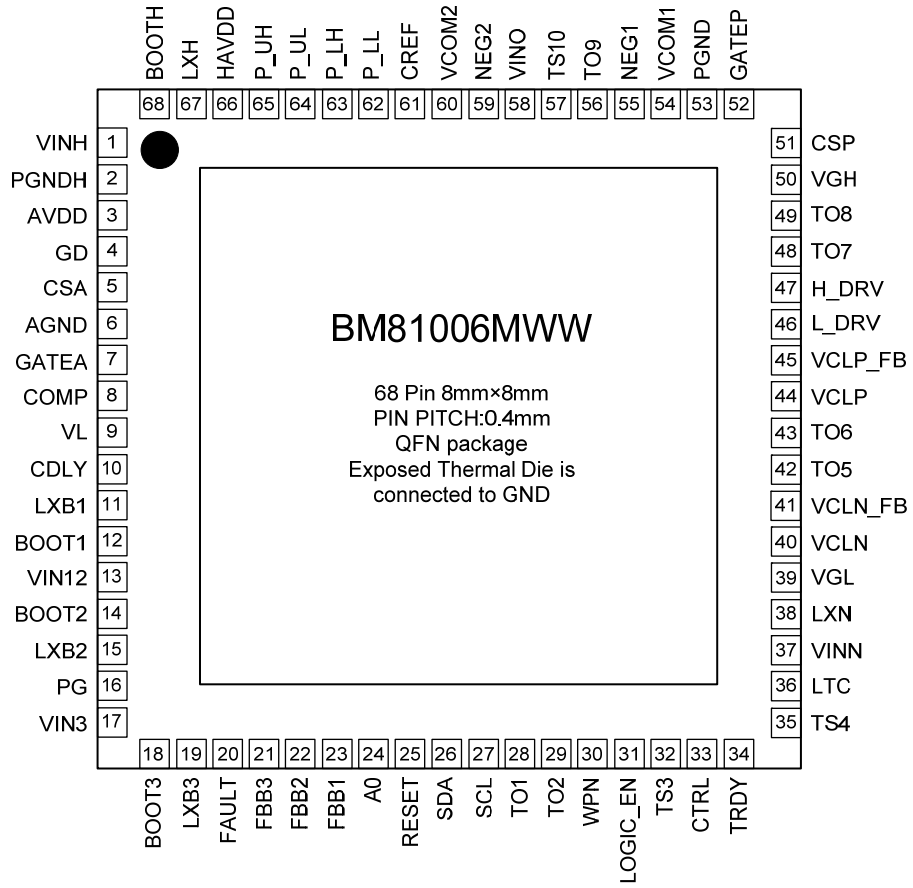


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	VINH	HAVDD power supply
2	PGNDH	HAVDD ground
3	AVDD	AVDD feedback input and Gamma power supply
4	GD	Load switch gate drive
5	CSA	AVDD current sense
6	AGND	Analog ground
7	GATEA	AVDD low side NMOS gate drive
8	COMP	AVDD phase compensation
9	VL	Internal power regulator
10	CDLY	RESET signal delay adjustment
11	LXB1	VDD1 switching
12	BOOT1	VDD1 bootstrap capacitor connection
13	VIN12	VDD1 and VDD2 power supply
14	BOOT2	VDD2 bootstrap capacitor connection
15	LXB2	VDD2 switching
16	PG	Power Good signal output
17	VIN3	VDD3 power supply
18	BOOT3	VDD3 bootstrap capacitor connection
19	LXB3	VDD3 switching
20	FAULT	Fault signal input/output

Pin Description – continued

Pin No.	Pin Name	Function
21	FBB3	VDD3 feedback input
22	FBB2	VDD2 feedback input
23	FBB1	VDD1 feedback input
24	A0	Slave address select
25	RESET	RESET signal output
26	SDA	Serial data input
27	SCL	Serial clock input
28	TO1	Test output normally open
29	TO2	Test output normally open
30	WPN	EEPROM writable input
31	LOGIC_EN	Enable input for VDDx
32	TS3	Test input normally short to ground
33	CTRL	GPM control input
34	TRDY	Enable input for channels except VDDx
35	TS4	Test input normally short to ground
36	LTC	Low temperature compensation input
37	VINN	VGL power supply
38	LXN	VGL switching
39	VGL	VGL feedback input
40	VCLN	VCLN external buffer drive
41	VCLN_FB	VCLN feedback input
42	TO5	Test output normally open
43	TO6	Test output normally open
44	VCLP	VCLP external buffer drive
45	VCLP_FB	VCLP feedback input
46	L_DRV	GPM low side external PNP drive
47	H_DRV	GPM high side external NPN drive
48	TO7	Test output normally open
49	TO8	Test output normally open
50	VGH	VGH feedback input and GPM power supply
51	CSP	VGH current sense
52	GATEP	VGH low side NMOS gate drive
53	PGND	Power ground
54	VCOM1	VCOM amplifier 1 output
55	NEG1	VCOM amplifier 1 negative input
56	TO9	Test output normally open
57	TS10	Test input normally short to ground
58	VINO	VCOM amplifier power supply
59	NEG2	VCOM amplifier 2 negative input
60	VCOM2	VCOM amplifier 2 output
61	CREF	VCOM reference voltage
62	P_LL	Programmable Gamma amplifier output
63	P_LH	Programmable Gamma amplifier output
64	P_UL	Programmable Gamma amplifier output
65	P_UH	Programmable Gamma amplifier output
66	HAVDD	HAVDD feedback input
67	LXH	HAVDD switching
68	BOOTH	HAVDD bootstrap capacitor connection

Block Diagram

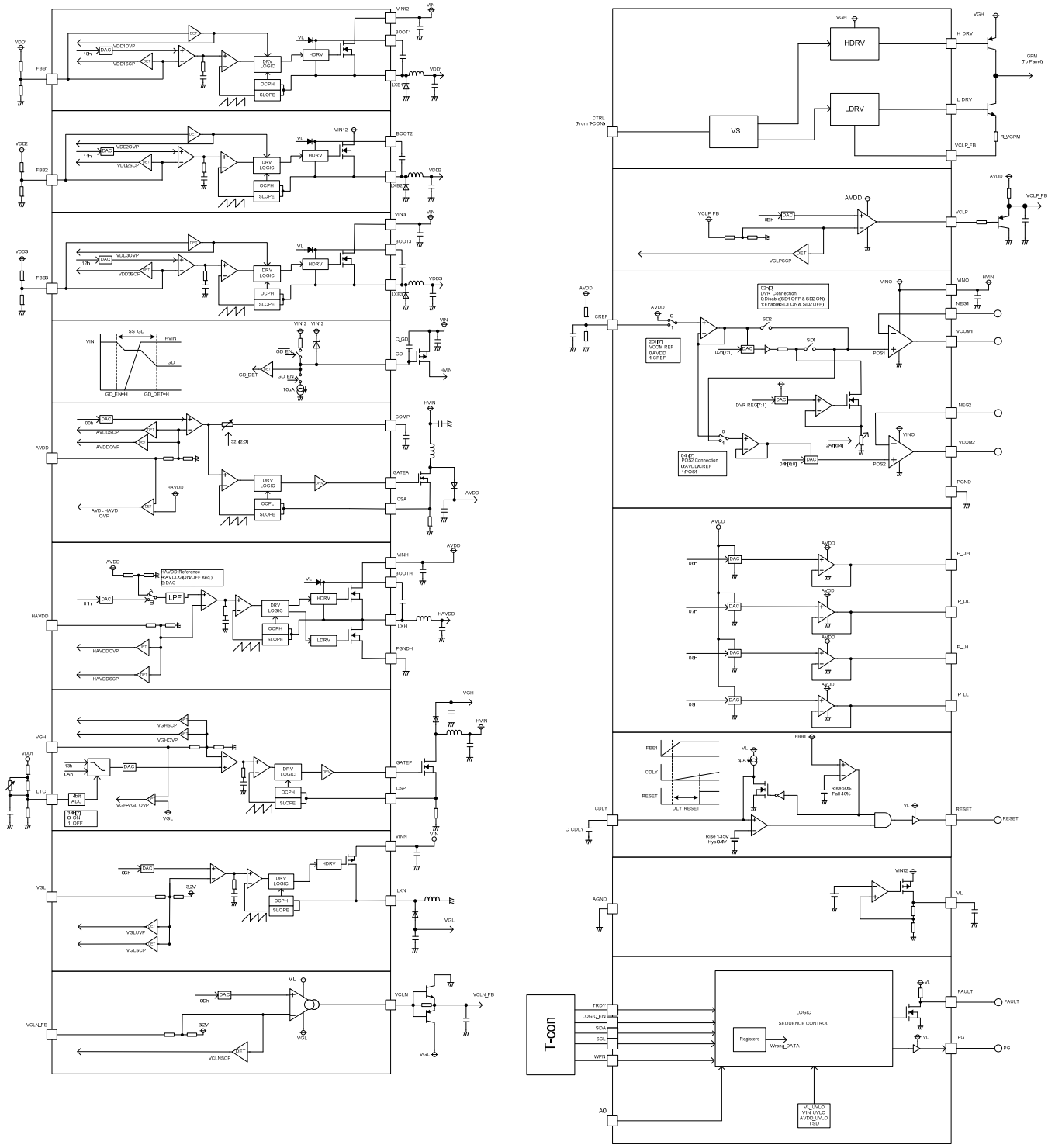


Figure 3. Block Diagram

Description of Block

1. Buck Converter (VDD1)

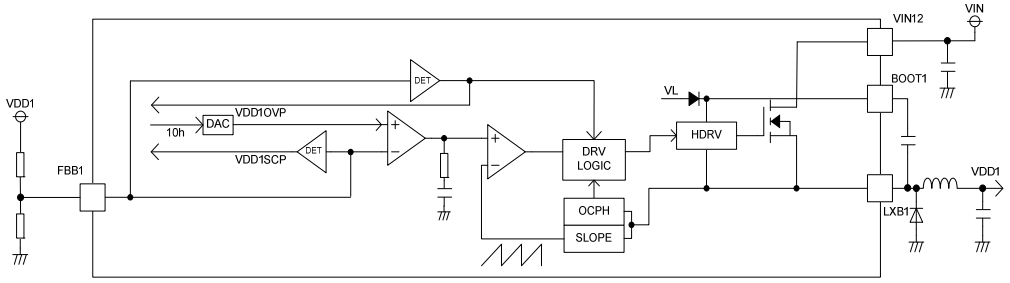


Figure 4. VDD1 Buck Converter Block Diagram

VDD1 is a current-mode asynchronous buck converter with built-in bootstrap type high-side NMOS.
FBB1 reference voltage can be set by Address:10h, Data:27h to C7h, with the range from 0.4V to 2.0V by 0.01V step.
VDD1 output voltage is decided by resistance division.

2. Buck Converter (VDD2)

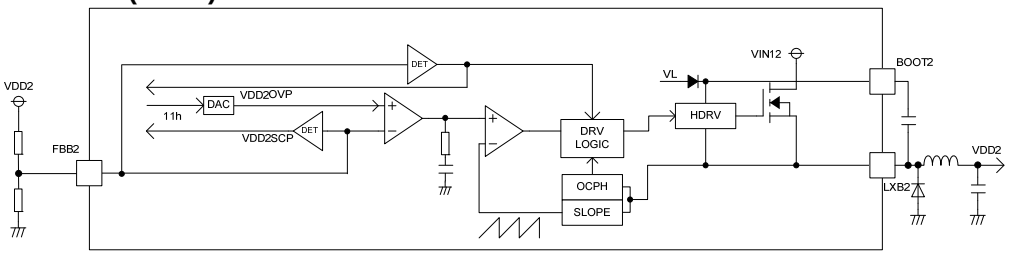


Figure 5. VDD2 Buck Converter Block Diagram

VDD2 is a current-mode asynchronous buck converter with built-in bootstrap type high-side NMOS.
FBB2 reference voltage can be set by Address:11h, Data:27h to C7h, with the range from 0.4V to 2.0V by 0.01V step.
VDD2 output voltage is decided by resistance division.

3. Buck Converter (VDD3)

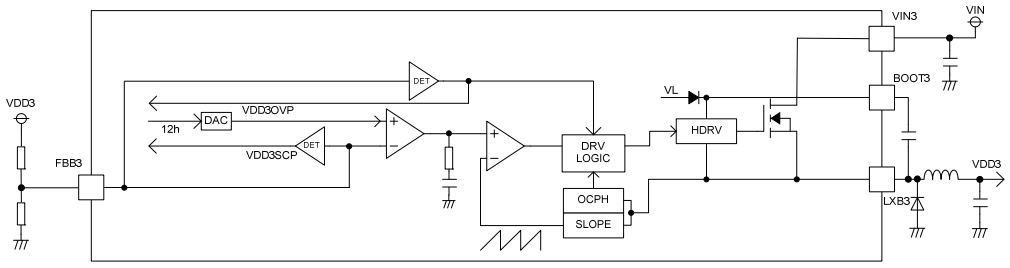


Figure 6. VDD3 Buck Converter Block Diagram

VDD3 is a current-mode asynchronous buck converter with built-in bootstrap type high-side NMOS.
FBB3 reference voltage can be set by Address:12h, Data:27h to C7h, with the range from 0.4V to 2.0V by 0.01V step.
VDD3 output voltage is decided by resistance division.

Description of Block – continued

4. Load Switch Gate Drive (GD)

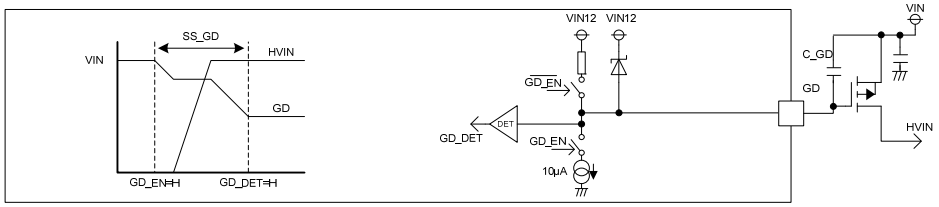


Figure 7. GD Block Diagram

GD is the gate drive pin for PMOS load switch.
When GD_EN=H, it drive PMOS load switch gate with a constant current to control inruch current.
When GD_EN=L, PMOS load switch is off by pull-up resistance.
SS_GD, the period from GD_EN=H to GD_DET=H, can be calculated as follows.

$$SS\_GD(Typ) = \frac{(C\_GD+Cg)\times 6V}{10\mu A}$$

Where:
Cg is load switch input capacitance.

5. Boost Converter (AVDD)

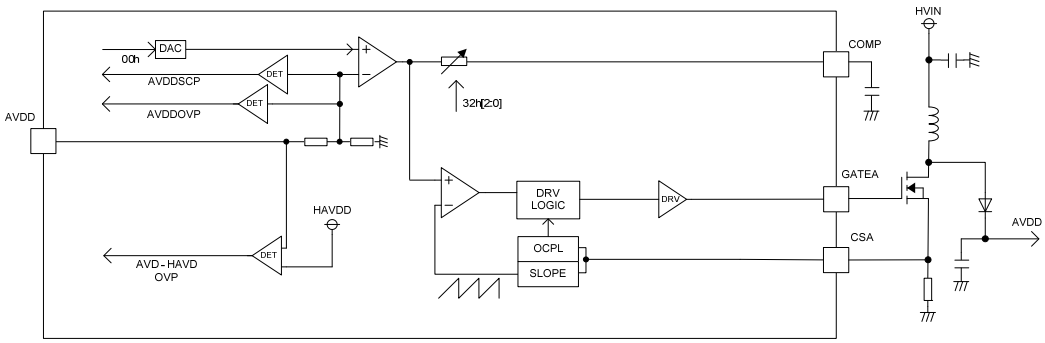


Figure 8. AVDD Boost Converter Block Diagram

AVDD is a current-mode asynchronous boost converter.
AVDD output voltage can be set by Address:00h, Data:86h to C1h, with the range from 13.5V to 19.4V by 0.1V step.
AVDD incorporates COMP resistance for phase compensation which can be set by Address:32h[2:0].

6. Buck Converter (HAVDD)

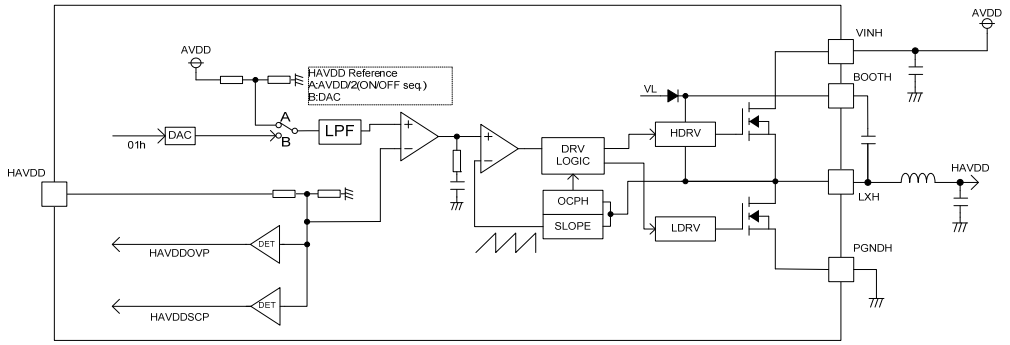


Figure 9. Buck Converter Block Diagram

HAVDD is a current-mode synchronous buck converter with built-in bootstrap type high-side NMOS and low-side NMOS.
HAVDD output voltage can be set by Address:01h, Data:86h to C1h, with the range from 6.75V to 9.7V by 0.05V step.

Description of Block – continued

7. Boost Converter (VGH)

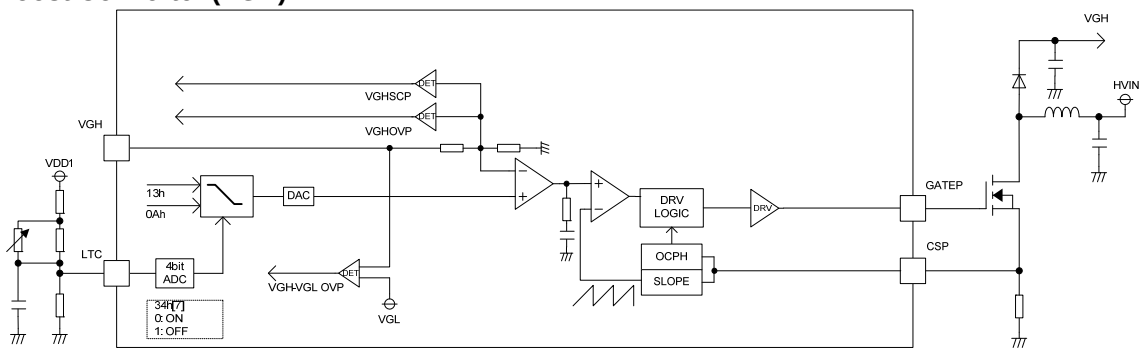


Figure 10. VGH Boost Converter Block Diagram

VGH is a current-mode asynchronous boost converter.
VGH output voltage can be set by Address:0Ah, Data:4Ah to E0h, with the range from 15V to 45V by 0.2V step.

8. Low Temperature Compensation (LTC)

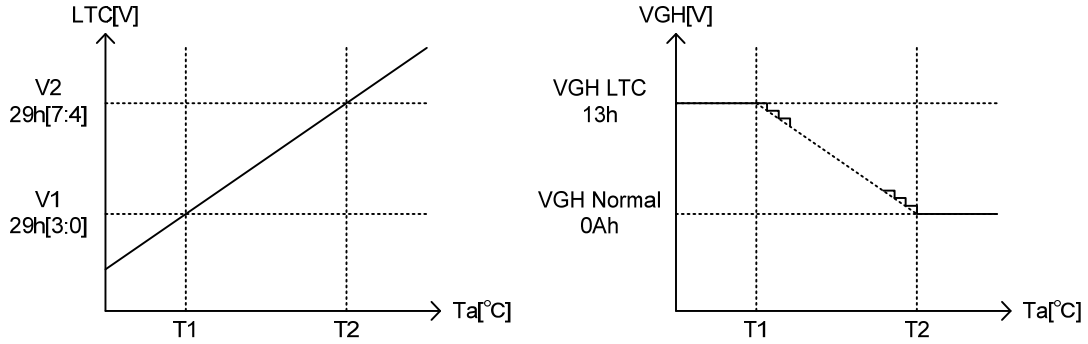


Figure 11. LTC function

The LTC pin voltage converted by ADC, LOGIC block control VGH output voltage. When LTC function enabled,
Low temperature VGH output voltage can be set by Address:13h, Data:4Ah to E0h, with the range from 15V to 45V by 0.2V step.
When LTC function disabled, make the LTC pin short to GND.

9. Inverting Converter (VGL)

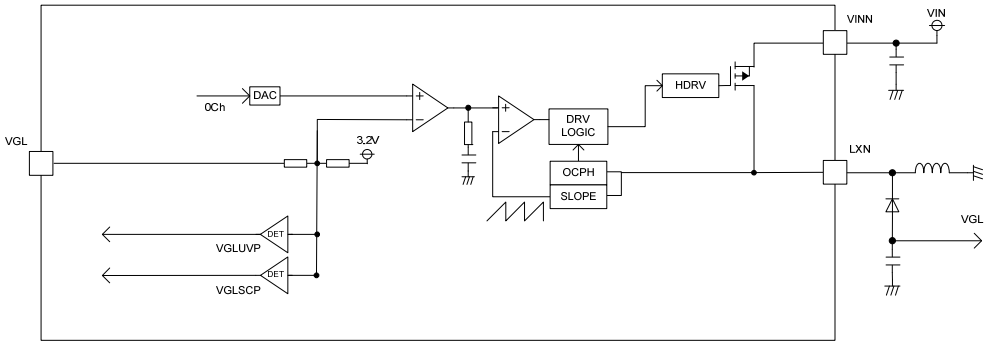


Figure 12. VGL Inverting Converter Block Diagram

VGL is an asynchronous inverting converter with built-in PMOS of VINN to LXN.
VGL output voltage can be set by Address:0Ch, Data:09h to 6Dh, with the range from -2V to -22V by 0.2V step.

Description of Block – continued

10. Negative Regulator (VCLN)

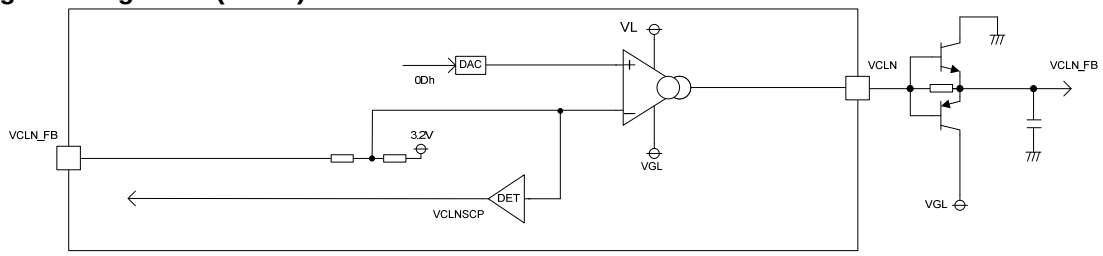


Figure 13. VCLN Block Diagram

VCLN is a regulator to drive the external buffer.
VCLN output voltage can be set by Address:0Dh, Data:09h to 63h, with the range from -2V to -20V by 0.2V step.
In case of NOT using VCLN, set Address:0Dh = 00h and make VCLN and VCLN_FB open.

11. Gate Pulse Modulation (GPM) / Positive Regulator (VCLP)

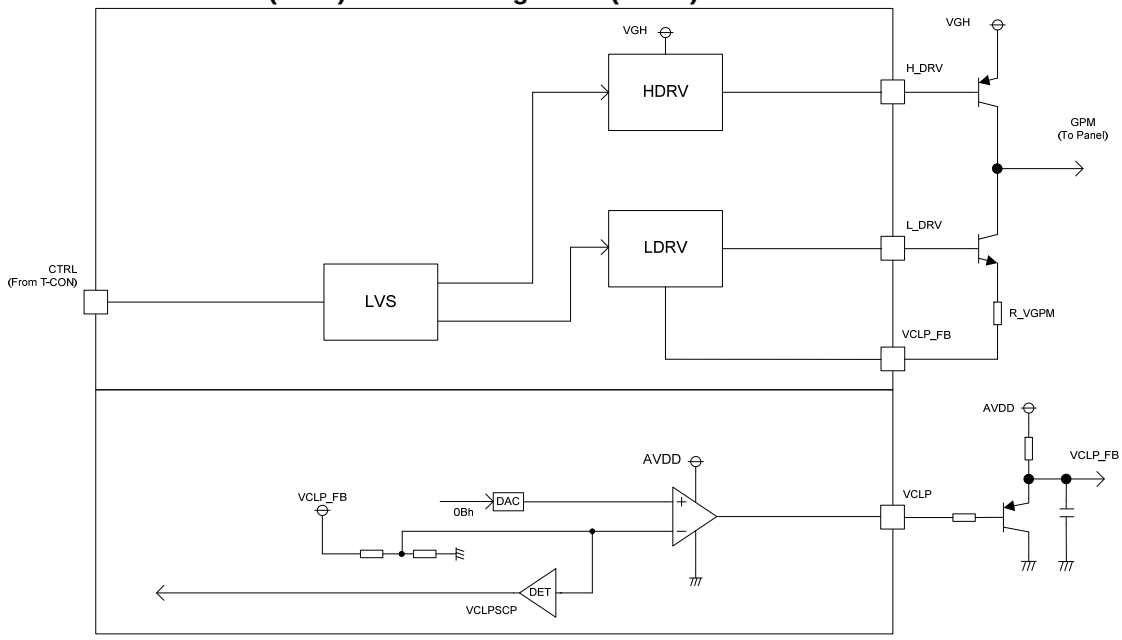


Figure 14. GPM/VCLP Block Diagram

GPM block drive the external Bip-Tr with the H_DRV and L_DRV pins.
When CTRL=H, GPM output is VGH level.
When CTRL=L, L_DRV-VCLP_FB voltage is regulated 1.6V(Typ) and the current of the low-side Bip-Tr is decided with R_VGPM.

VCLP is a regulator to drive the external buffer.
VCLP output voltage can be set by Address:0Bh, Data:0Eh to 63h, with the range from 3V to 20V by 0.2V step.
In case of NOT using VCLP, set Address:0Bh = 00h and make VCLP and VCLP_FB open.

Description of Block – continued

12. VCOM Amplifier / Digital Variable Range(DVR)

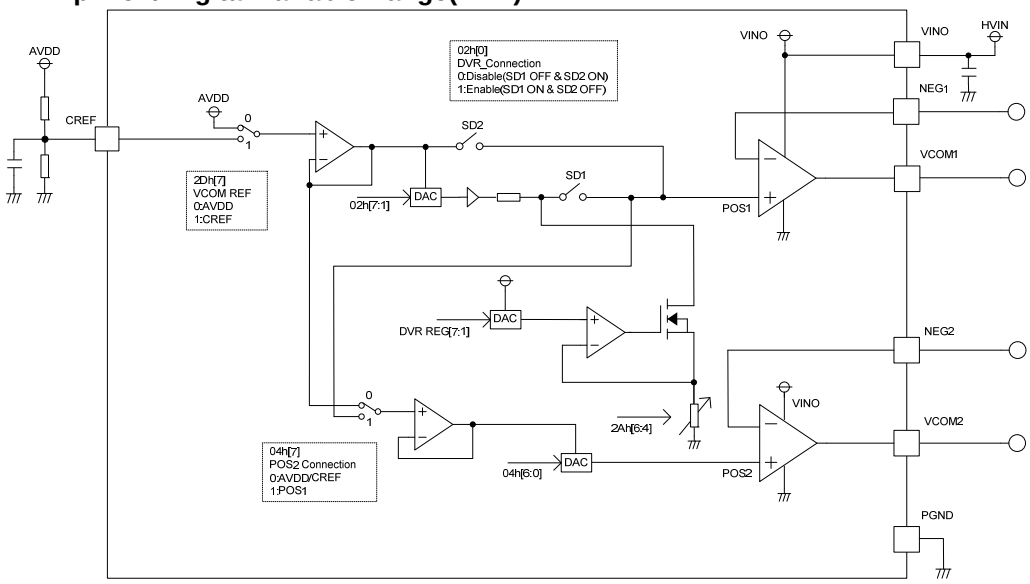


Figure 15. VCOM Amplifier / DVR Block Diagram

In VCOM amplifier block, the reference values POS1 and POS2 are selectable with register setting.
In case of using DVR functions, the reference voltage can be adjusted by DVR Register setting (DVR_REG[7:1]).
Internal EEPROM is available for DVR Register.
In case of NOT using VCOM amplifier, short the VCOM and NEG pins not to connect the other nodes.
In case of NOT using the CREF pin, set Address:2Dh[7] = 0 and make the CREF pin open.

POS1 setting

$$POS1 = VCOM\_REF \quad \text{(DVR\_Connection=0)}$$

$$POS1 = VCOM\_REF \times \frac{DVR\_MAX+1}{128} - DVR\_RANGE \times \frac{DVR\_REG+1}{128} \quad \text{(DVR\_Connection=1)}$$

VCOM_REF 2Dh[7]	DVR_MAX 02h[7:1]	DVR_RANGE 2Ah[6:4]	DVR_REG[7:1]	DVR_Connection 02h[0]
0: AVDD 1: CREF	0-127	0.5V to 4.0V	0-127	0: Disable 1: Enable

POS2 setting

$$POS = VCOM\_REF \times \frac{VCOM2\_DAC+1}{128} \quad \text{(POS2\_Connection=0)}$$

$$POS2 = POS1 \times \frac{VCOM2\_DAC+1}{128} \quad \text{(POS2\_Connection=1)}$$

VCOM2_DAC 04h[6:0]	POS2_Connection 04h[7]
0-127	0: AVDD/CREF 1: POS1

Description of Block – continued

13. Gamma Amplifier

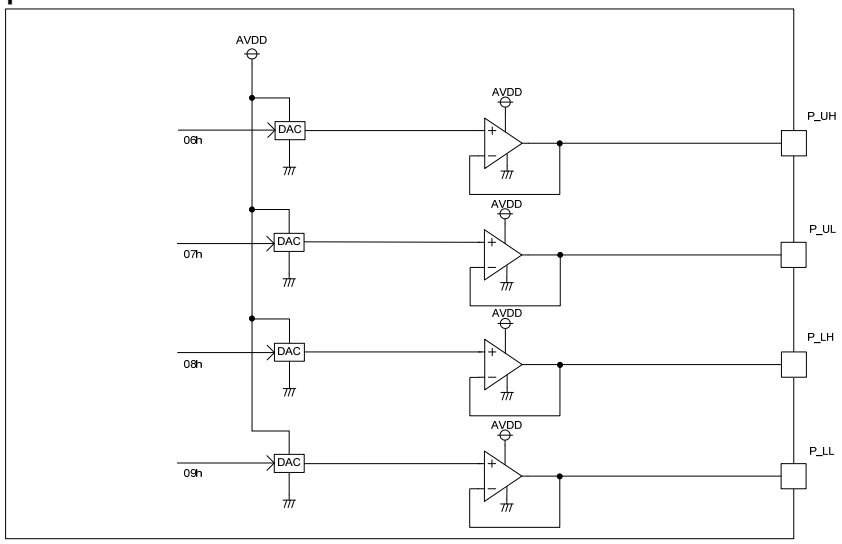


Figure 16. Gamma Amplifier Block Diagram

4 channel amplifiers for Gamma are incorporated. The reference voltage is AVDD.
Gamma output voltage can be set by Address:06h to 09h.

$$P\_xx = AVDD \times \frac{DAC+1}{256} \qquad \text{(DAC=0-255)}$$

14. RESET

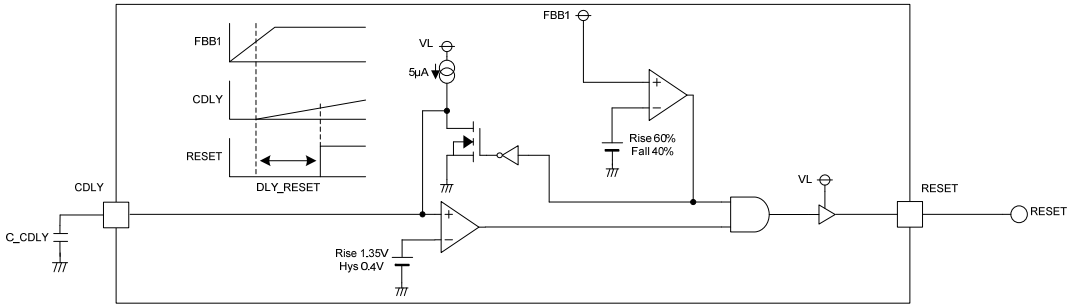


Figure 17. RESET Block Diagram

If FBB1 is more than 60%(Typ) of the register setting, RESET output is High after DLY_RESET.
If FBB1 is less than 40%(Typ) of the register setting, RESET output is Low.

CDLY setting	DLY_RESET(Typ)
Connect to C_CDLY	1.35V × C_CDLY / 5µA
Open	No delay
Short to VL	100ms fixed

Description of Block – continued

15. LOGIC/SEQUENCE CONTROL

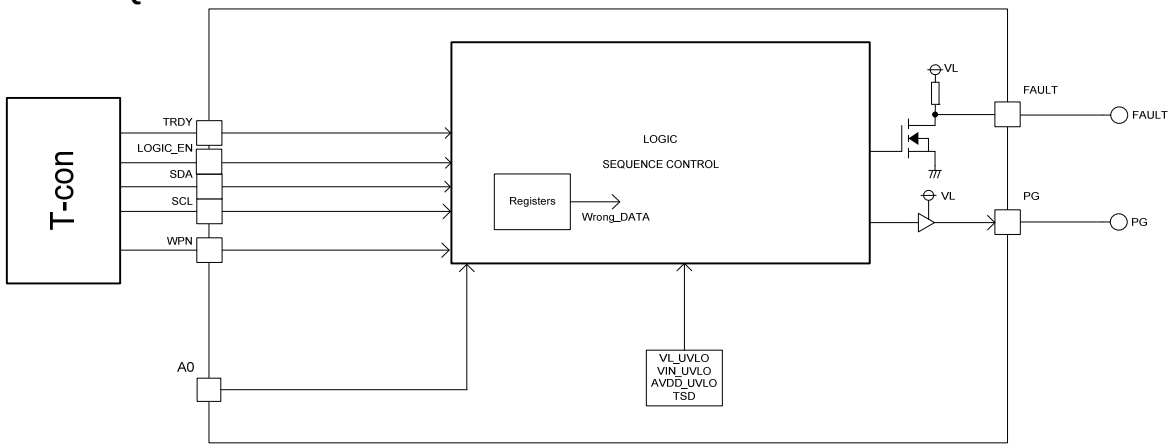


Figure 18. LOGIC/SEQUENCE CONTROL Block Diagram

LOGIC/SEQUENCE CONTROL decide IC operations depending on the protection functions.

BLOCK	Detect/Release Conditions(Typ)	Action
VL_UVLO	Detect 3.5V Release 4.1V	IC Reset
VIN_UVLO	Detect 6.5V Release 8.8V	All CH Shutdown Release to Reset
AVDD_UVLO	Detect 4.5V Release 5.0V	HAVDD Shutdown P_UH, P_UL Shutdown
TSD	Detect 165°C Hysteresis 20°C	All CH Shutdown Release to Reset
Wrong_DATA	Registers out of Range	All CH Shutdown VL_UVLO to Reset

16. FAULT

The FAULT pin is open drain output with internal pull up resistor. The output High / Low depends on protection functions. It also can be connected the external open drain circuits to control IC operations.

VIN_UVLO TSD Wrong_DATA HAVDD_OVP*(Note 1)* SCP*(Note 1)*	Start-up Enable 34h[0]	Fault Output	Fault Input	Action
Detect	-	L	-	Depends on Protect Functions
Release	0: Disable	L	-	All CH Except VDDx Shutdown
Release	-	H	L	All CH Except VDDx Shutdown
Release	1: Enable	H	H or Open	Normal

(Note 1) Refer to Protection List on the next page.

17. PG

The PG pin is output of inverter. The output become high after the ON sequence ends normally.

Description of Block – continued

18. Protection List

Timer-Latch Type Short Circuit Protection (SCP)

BLOCK	Detect/Release Conditions(Typ)	Action	Counter Enable
VDD1	Detect 85% Release 90%	All CH Latch-off after 3ms VL_UVLO to Reset	After Soft-start ends
VDD2			
VDD3			
AVDD	Detect 85% Release 90%	All CH except VDDx Latch-off after 3ms VL_UVLO to Reset	
HAVDD	Detect 70% Release 90%		
VGH	Detect 75% Release 80%		
VGL	Detect 75% Release 85%		
VCLP			After DLY3 ends
VCLN			After Soft-start ends
GD	GD_EN Rise	All CH except VDDx Latch-off after 4counts VL_UVLO to Reset	Before AVDD Soft-start ends (The counter is Reset after AVDD Soft-start ends)

Over Voltage Protection (OVP)

BLOCK	Detect/Release Conditions(Typ)	Action
VDD1	Detect 125% Hysteresis 10%	Switching Stop
VDD2		
VDD3		
AVDD	Detect 21.0V Hysteresis 1.1V	Switching Stop
	Detect 10.2V (Monitoring Differential Voltage between AVDD and HAVDD)	Lower AVDD Output
HAVDD	Detect 10.2V	All CH except VDDx Latch-off VL_UVLO to Reset
VGH	Detect 47.5V Hysteresis 1.0V	Switching Stop
	Detect 62V (Monitoring Differential Voltage between VGH and VGL)	Switching Stop
VGL	Detect -28.5V Hysteresis 1.0V	Switching Stop

Over Current Protection (OCP)

BLOCK	SYMBOL	Detect Conditions(Min)	Action
VDD1	I_{LXB1_Limit}	Detect 2A	Duty Limit
VDD2	I_{LXB2_Limit}	Detect 3A	
VDD3	I_{LXB3_Limit}	Detect 3A	
AVDD	V_{CSA}	Detect 0.235V at 5A Setting 5A, 8A Setting Available (Monitoring CSA Voltage)	
HAVDD	$I_{LXH\_Limit\_H}$	Detect +3.0A Source	
	$I_{LXH\_Limit\_L}$	Detect -3.0A Sink	
VGH	V_{CSP}	Detect 0.225V at 2.25A Setting 0.5A to 2.25A Setting Available (Monitoring CSP Voltage)	
VGL	I_{LXN_Limit}	I_{LXN_Limit} > 2.0A	
VCLN	I_{VCLN_Limit}	2.0mA	Output Current Limit
VCLP	I_{VCLP_Limit}	2.0mA	
VCOM	I_{VCOM_Source}	+500mA Source	Short Circuit Current Limit
	I_{VCOM_Sink}	-500mA Sink	
Gamma	I_{GAM_Source}	+50mA Source	
	I_{GAM_Sink}	-50mA Sink	

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{VIN12}, V_{VIN3}, V_{VINN}	-0.3 to +20	V
	V_{VINO}, V_{VINH}	-0.3 to +24	V
Input Voltage	V_{AVDD}, V_{CREF}, V_{VCLP_FB}, V_{NEG1}, V_{TS10}, V_{NEG2}	-0.3 to +24	V
	V_{COMP}, V_{CSA}, V_{LOGIC_EN}, V_{FBB3}, V_{FBB2}, V_{FBB1}, V_{TS3}, V_{SDA}, V_{SCL}, V_{WPN}, V_{CTRL}, V_{TRDY}, V_{TS4}, V_{LTC}, V_{CSP}, V_{A0}	-0.3 to +7	V
	V_{VGH}	-0.55 to +50	V
	V_{VGL}, V_{VCLN_FB}	-30 to +0.3	V
Output Voltage	V_{GATEA}, V_{VL}, V_{RESET}, V_{TO1}, V_{TO2}, V_{GATEP}, V_{FAULT}, V_{PG}, V_{CDLY}	-0.3 to +7	V
	V_{GD}, V_{LXB1}, V_{LXB2}, V_{LXB3}, V_{HAVDD}	-0.3 to +20	V
	V_{BOOT1}, V_{BOOT2}, V_{BOOT3}	-0.3 to V_{LXBx} +7	V
	V_{BOOTH}	-0.3 to V_{LXH} +7	V
	V_{LXH}, V_{VCLP}, V_{VCOM1}, V_{TO9}, V_{VCOM2}, V_{P_LL}, V_{P_LH}, V_{P_UL}, V_{P_UH}	-0.3 to +24	V
	V_{L_DRV}, V_{H_DRV}, V_{TO7}, V_{TO8}	-0.3 to +50	V
	V_{VCLN}, V_{TO5}, V_{TO6}	-30 to +7	V
	V_{LXN}	V_{VINN} -42 to V_{VINN} +0.3	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
UQFN68W8080A				
Junction to Ambient	θ_{JA}	84.8	34.2	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	21	16	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air).

*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

*(Note 3)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 4)*Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
VIN Input Voltage	V_{VIN12}, V_{VIN3}, V_{VINN}	9.1	12.0	14.7	V
AVDD Input Voltage	V_{VINH}, V_{VINO}	9.1	17.5	19.4	V
AVDD Output Voltage *(Note 1)*	V_{AVDD}	VIN×1.06	17.5	19.4	V
VGH Output Voltage	V_{VGH}	15	31	45	V
VGL Output Voltage	V_{VGL}	-22	-12	-2	V
Logic Input Voltage	V_{SDA}, V_{SCL}, V_{WPN}, V_{LOGIC_EN}, V_{CTRL}, V_{TRDY}, V_{A0}	-	VL	-	V
Operating Temperature	Topr	-40	+25	+105	°C

(Note 1) In case of VIN×1.06>AVDD, AVDD output can differ from the setting output.

Electrical Characteristics

Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
[Buck Converter (VDD1)]						
Output Voltage Range	V_{VDD1}	0.8	-	4.0	V	Step 0.01V
Maximum Duty Cycle	D_{MAX_VDD1}	81	90	99	%	
FBB1 Regulation Voltage	V_{FBB1_R}	1.617	1.650	1.683	V	No Load, ±2.0% Error
VDD1 SCP Threshold Voltage	$V_{VDD1SCP}$	V_{FBB1} ×0.816	V_{FBB1} ×0.85	V_{FBB1} ×0.884	V	FBB1 Falling
		V_{FBB1} ×0.866	V_{FBB1} ×0.90	V_{FBB1} ×0.934	V	FBB1 Rising
Over Voltage Protection	$V_{VDD1OVP}$	V_{FBB1} ×1.20	V_{FBB1} ×1.25	V_{FBB1} ×1.30	V	FBB1 Rising
Over Voltage Protection Hysteresis	$V_{VDD1OVP\_HYS}$	-	10	-	%	
LXB1 Current Limit *(Note 1)*	I_{LXB1_Limit}	2.0	3.3	4.6	A	
LXB1 Leakage Current	I_{LXB1_Leak}	-	-	5	μA	
LXB1 On Resistance High *(Note 1)*	R_{LXB1_H}	0.15	0.3	0.6	Ω	I_{LXB1}=200mA
VDD1 Discharge Resistance *(Note 1)*	R_{VDD1_DCHG}	0.3	0.6	1.2	kΩ	
Load Regulation *(Note 1)*	L_{RVDD1}	-1	-	+1	%	I_{LOAD}=1.0A
Line Regulation *(Note 1)*	dV_{VDD1}	-1	-	+1	%	
Soft Start Period	t_{SS_VDD1}	2.4	3.0	3.6	ms	
[Buck Converter (VDD2)]						
Output Voltage Range	V_{VDD2}	0.8	-	4.0	V	Step 0.01V
Maximum Duty Cycle	D_{MAX_VDD2}	81	90	99	%	
FBB2 Regulation Voltage	V_{FBB2_R}	0.882	0.900	0.918	V	No Load, ±2.0% Error
VDD2 SCP Threshold Voltage	$V_{VDD2SCP}$	V_{FBB2} ×0.816	V_{FBB2} ×0.85	V_{FBB2} ×0.884	V	FBB2 Falling
		V_{FBB2} ×0.866	V_{FBB2} ×0.90	V_{FBB2} ×0.934	V	FBB2 Rising
Over Voltage Protection	$V_{VDD2OVP}$	V_{FBB2} ×1.20	V_{FBB2} ×1.25	V_{FBB2} ×1.30	V	FBB2 Rising
Over Voltage Protection Hysteresis	$V_{VDD2OVP\_HYS}$	-	10	-	%	
LXB2 Current Limit *(Note 1)*	I_{LXB2_Limit}	3.0	4.3	5.6	A	
LXB2 Leakage Current	I_{LXB2_Leak}	-	-	5	μA	
LXB2 On Resistance High *(Note 1)*	R_{LXB2_H}	0.15	0.3	0.6	Ω	I_{LXB2}=200mA
VDD2 Discharge Resistance *(Note 1)*	R_{VDD2_DCHG}	0.3	0.6	1.2	kΩ	
Load Regulation *(Note 1)*	L_{RVDD2}	-1	-	+1	%	I_{LOAD}=1.0A
Line Regulation *(Note 1)*	dV_{VDD2}	-1	-	+1	%	
Soft Start Period	t_{SS_VDD2}	2.4	3.0	3.6	ms	
[Buck Converter (VDD3)]						
Output Voltage Range	V_{VDD3}	0.8	-	4.0	V	Step 0.01V
Maximum Duty Cycle	D_{MAX_VDD3}	81	90	99	%	
FBB3 Regulation Voltage	V_{FBB3_R}	0.882	0.900	0.918	V	No Load, ±2.0% Error
VDD3 SCP Threshold Voltage	$V_{VDD3SCP}$	V_{FBB3} ×0.816	V_{FBB3} ×0.85	V_{FBB3} ×0.884	V	FBB3 Falling
		V_{FBB3} ×0.866	V_{FBB3} ×0.90	V_{FBB3} ×0.934	V	FBB3 Rising
Over Voltage Protection	$V_{VDD3OVP}$	V_{FBB3} ×1.20	V_{FBB3} ×1.25	V_{FBB3} ×1.30	V	FBB3 Rising
Over Voltage Protection Hysteresis	$V_{VDD3OVP\_HYS}$	-	10	-	%	
LXB3 Current Limit *(Note 1)*	I_{LXB3_Limit}	3.0	4.3	5.6	A	
LXB3 Leakage Current	I_{LXB3_Leak}	-	-	5	μA	
LXB3 On Resistance High *(Note 1)*	R_{LXB3_H}	0.15	0.3	0.6	Ω	I_{LXB3}=200mA
VDD3 Discharge Resistance *(Note 1)*	R_{VDD3_DCHG}	0.3	0.6	1.2	kΩ	
Load Regulation *(Note 1)*	LR_{VDD3}	-1	-	+1	%	I_{LOAD}=1.0A
Line Regulation *(Note 1)*	dV_{VDD3}	-1	-	+1	%	
Soft Start Period	t_{SS_VDD3}	2.4	3.0	3.6	ms	

(Note 1) Design guarantee

Electrical Characteristics – continued

Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
[Load Switch Gate Drive(GD)]						
GD Clamp Voltage	V_{GD_CLP}	5	6	7	V	Differential Voltage between VIN12 and GD
GD Sink Current *(Note 1)*	I_{GD_Sink}	6	10	14	µA	
GD Pull-up Resistance	R_{GD}	5	10	15	kΩ	
[Boost Converter (AVDD)]						
Output Voltage Range	V_{AVDD}	VIN ×1.06	-	19.4	V	Step 0.1V
Maximum Duty Cycle	D_{MAX_AVDD}	81	95	99.9	%	
AVDD Regulation Voltage	V_{AVDD_R}	17.325	17.5	17.675	V	No Load, ±1.0% Error
AVDD SCP Threshold Voltage	$V_{AVDDSCP}$	V_{AVDD} ×0.816	V_{AVDD} ×0.85	V_{AVDD} ×0.884	V	AVDD Falling
		V_{AVDD} ×0.866	V_{AVDD} ×0.90	V_{AVDD} ×0.934	V	AVDD Rising
Over Voltage Protection	$V_{AVDDOVP}$	20.0	21.0	22.0	V	AVDD Rising
Over Voltage Protection Hysteresis	$V_{AVDDOVP\_HYS}$	0.6	1.1	1.6	V	
AVDD – HAVDD Over Voltage Protection *(Note 1)*	$V_{AVD\text{-}HAVOVP}$	9.9	10.2	10.5	V	Differential Voltage between AVDD and HAVDD
CSA Threshold Voltage	V_{CSA}	0.235	0.294	0.353	V	R_CSA =0.047Ω
GATEA On Resistance High *(Note 1)*	R_{GATEA_H}	-	10	-	Ω	I_{GATEA}=-10mA
GATEA On Resistance Low *(Note 1)*	R_{GATEA_L}	-	10	-	Ω	I_{GATEA}=10mA
AVDD Discharge Resistance *(Note 1)*	R_{AVDD_DCHG}	0.7	1.4	2.1	kΩ	
Load Regulation *(Note 1)*	LR_{AVDD}	-1	-	+1	%	I_{LOAD}=1.0A
Line Regulation *(Note 1)*	dV_{AVDD}	-1	-	+1	%	
Integral Non Linearity *(Note 1)*	INL_{AVDD}	-1	-	+1	LSB	
Differential Non Linearity *(Note 1)*	DNL_{AVDD}	-1	-	+1	LSB	
[Buck Converter (HAVDD)]						
Output Voltage Range	V_{HAVDD}	6.75	-	9.7	V	Step 0.05V
HAVDD Regulation Voltage	V_{HAVDD_R}	8.663	8.75	8.837	V	No Load, ±1.0% Error
HAVDD SCP Threshold Voltage	$V_{HAVDDSCP}$	V_{HAVDD} ×0.666	V_{HAVDD} ×0.70	V_{HAVDD} ×0.734	V	HAVDD Falling
		V_{HAVDD} ×0.866	V_{HAVDD} ×0.90	V_{HAVDD} ×0.934	V	HAVDD Rising
Over Voltage Protection	$V_{HAVDDOVP}$	9.9	10.2	10.5	V	HAVDD Rising
LXH Current Limit *(Note 1)*	$I_{LXH\_Limit\_H}$	3.0	3.75	4.5	A	
	$I_{LXH\_Limit\_L}$	-4.5	-3.75	-3.0	A	
LXH Leakage Current	$I_{LXH\_Leak\_H}$	-	-	5	µA	
	$I_{LXH\_Leak\_L}$	-	-	5	µA	
LXH On Resistance High *(Note 1)*	R_{LXH_H}	0.15	0.3	0.6	Ω	I_{LXH}=200mA
LXH On Resistance Low *(Note 1)*	R_{LXH_L}	0.15	0.3	0.6	Ω	I_{LXH}=-200mA
HAVDD Discharge Resistance *(Note 1)*	R_{HAVDD_DCHG}	3.5	7.0	14.0	kΩ	
Load Regulation *(Note 1)*	LR_{HAVDD_Source}	-1	-	+1	%	I_{LOAD}=1.0A
	LR_{HAVDD_Sink}	-1	-	+1	%	I_{LOAD}=-1.0A
Line Regulation *(Note 1)*	dV_{HAVDD}	-1	-	+1	%	
Integral Non Linearity *(Note 1)*	INL_{HAVDD}	-1	-	+1	LSB	
Differential Non Linearity *(Note 1)*	DNL_{HAVDD}	-1	-	+1	LSB	

(Note 1) Design guarantee

Electrical Characteristics – continued

Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
[Boost Converter (VGH)]						
Output Voltage Range	$V_{HAVDDVGH}$	15	-	45	V	Step 0.2V
VGH Regulation Voltage	V_{VGH_R}	30.07	31	31.93	V	No load, ±3.0% Error
VGH SCP Threshold Voltage	V_{VGHSCP}	V_{VGH} ×0.7125	V_{VGH} ×0.75	V_{VGH} ×0.7875	V	VGH Falling
		V_{VGH} ×0.7625	V_{VGH} ×0.80	V_{VGH} ×0.8375	V	VGH Rising
Over Voltage Protection	V_{VGHOVP}	-	47.5	-	V	VGH Rising
VGH OVP Hysteresis	V_{VGHOVP_HYS}	-	1.0	-	V	
VGH – VGL Over Voltage Protection *(Note 1)*	$V_{VGH-VGLOVP}$	-	62	-	V	Differential Voltage between VGH and VGL
CSP Threshold Voltage	V_{CSP}	225	-	-	mV	R_CSP =0.1Ω
GATEP On Resistance High *(Note 1)*	R_{GATEP_H}	-	10	-	Ω	I_{GATEP_H}=-10mA
GATEP On Resistance Low *(Note 1)*	R_{GATEP_L}	-	10	-	Ω	I_{GATEP_L}=10mA
VGH Discharge Resistance *(Note 1)*	R_{VGH_DCHG}	-	6	-	kΩ	
Integral Non Linearity *(Note 1)*	INL_{VGH}	-1	-	+1	LSB	
Differential Non Linearity *(Note 1)*	DNL_{VGH}	-1	-	+1	LSB	
[Inverting Converter (VGL)]						
Output Voltage Range	V_{VGL}	-22	-	-2	V	Step 0.2V
VGL Regulation Voltage	V_{VGL_R}	-12.36	-12	-11.64	V	No Load, ±3.0% Error
VGL SCP Threshold Voltage	V_{VGLSCP}	V_{VGL} ×0.7875	V_{VGL} ×0.75	V_{VGL} ×0.7125	V	VGL Rising
		V_{VGL} ×0.8875	V_{VGL} ×0.85	V_{VGL} ×0.8125	V	VGL Falling
Over Voltage Protection	V_{VGLOVP}	-30.0	-28.5	-27.0	V	
VGL OVP Hysteresis	V_{VGLOVP_HYS}	-	1.0	-	V	
LXN Current Limit *(Note 1)*	I_{LXN_Limit}	2.0	2.5	3.0	A	
LXN Leakage Current	I_{LXN_Leak}	-	-	5	μA	
LXN On Resistance *(Note 1)*	R_{LXN}	0.5	1.0	2.0	Ω	I_{LXN}=200mA
VGL Discharge Resistance *(Note 1)*	R_{VGL_DCHG}	-	1.2	-	kΩ	
Integral Non Linearity *(Note 1)*	INL_{VGL}	-1	-	+1	LSB	
Differential Non Linearity *(Note 1)*	DNL_{VGL}	-1	-	+1	LSB	
Soft Start Period	t_{SS_VGL}	4	5	6	ms	
[Negative Regulator (VCLN)]						
Output Voltage Range	V_{VCLN}	-20	-	-2	V	Step 0.2V, VCLN>VGL
VCLN Regulation Voltage	V_{VCLN_R}	-7.828	-7.6	-7.372	V	No Load, ±3.0% Error
VCLN SCP Threshold Voltage	$V_{VCLNSCP}$	V_{VCLN} ×0.7875	V_{VCLN} ×0.75	V_{VCLN} ×0.7125	V	VCLN Rising
		V_{VCLN} ×0.8875	V_{VCLN} ×0.85	V_{VCLN} ×0.8125	V	VCLN Falling
Current Limit *(Note 1)*	I_{VCLN_Limit}	2.0	3.5	5.0	mA	
Integral Non Linearity *(Note 1)*	INL_{VCLN}	-1	-	+1	LSB	
Differential Non Linearity *(Note 1)*	DNL_{VCLN}	-1	-	+1	LSB	

(Note 1) Design guarantee

Electrical Characteristics – continued

Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
[Gate Pulse Modulation (GPM)]						
CTRL to GPM Propagation Delay Rise	t_{VGPM_Delay}	-	100	250	ns	No Capacitive Load (CTRL to L_DRV,H_DRV)
CTRL Input Frequency	f_{CTRL}	-	-	500	KHz	-
H_DRV Current Ability *(Note 1)*	I_{HDRV}	1.5	3.0	6.0	mA	
L_DRV Current Ability *(Note 1)*	I_{LDRV}	1.5	3.0	6.0	mA	
[Positive Regulator (VCLP)]						
Output Voltage Range	V_{VCLP}	3	-	20	V	Step 0.2V, VCLP < AVDD
VCLP Regulation Voltage	V_{VCLP_R}	7.37	7.6	7.83	V	No Load, ±3.0% Error
VCLP SCP Threshold Voltage	$V_{VCLPSCP}$	V_{VCLP} ×0.7125	V_{VCLP} ×0.75	V_{VCLP} ×0.7875	V	VCLP Falling
		V_{VCLP} ×0.8125	V_{VCLP} ×0.85	V_{VCLP} ×0.8875	V	VCLP Rising
Current Limit *(Note 1)*	I_{VCLP_Limit}	2.0	3.5	5.0	mA	
Integral Non Linearity *(Note 1)*	INL_{VCLP}	-1	-	+1	LSB	
Differential Non Linearity *(Note 1)*	DNL_{VCLP}	-1	-	+1	LSB	
[VCOM Amplifier]						
VINO Supply Current	I_{VINO}	-	3.1	-	mA	
CREF Input Range	V_{VCOM_CREF}	3	-	V_{VINO} -0.8	V	
Output Error *(Note 1)*	V_{VCOM_Error}	-20	-	20	mV	VCOMx = CREF
Output Voltage High *(Note 1)*	V_{VCOM_H}	V_{VINO} -0.8	V_{VINO} -0.4	V_{VINO} -0.2	V	
Output Voltage Low *(Note 1)*	V_{VCOM_L}	0.2	0.4	0.8	V	
Continuous Current *(Note 1)*	I_{VCOM_Cont}	-	250	-	mA	
Short Circuit Current *(Note 1)*	I_{VCOM_Souce}	500	-	-	mA	
	I_{VCOM_Sink}	-	-	-500	mA	
CREF Input Current	I_{VCOM_CREF}	-0.5	0	+0.5	µA	
NEG Input Bias Current	I_{VCOM_NEG}	-0.5	-	+0.5	µA	
Load Regulation *(Note 1)*	LR_{VCOM}	-3	-	+3	%	
Integral Non Linearity *(Note 1)*	INL_{VCOM}	-1	-	+1	LSB	
Differential Non Linearity *(Note 1)*	DNL_{VCOM}	-1	-	+1	LSB	
VCOM Slew Rate *(Note 1)*	SR_{VCOM}	40	-	-	V/µs	
VCOM Propagation Delay *(Note 1)*	t_{VCOM_Delay}	-	-	100	ns	
[VCOM Calibrator]						
DVR Voltage Range	V_{DVR}	0.5	-	4.0	V	Step 0.5V
DVR Regulation Voltage	V_{DVR_R}	0.23	0.25	0.27	V	0.5V Setting, DAC = 63
DVR Integral Non Linearity *(Note 1)*	INL_{DVR}	-1	-	+1	LSB	
DVR Differential Non Linearity *(Note 1)*	DNL_{DVR}	-1	-	+1	LSB	
DVR Writing Cycle Time *(Note 1)*	t_{DVR_EEP}	-	10	20	ms	
DVR Setting Time *(Note 1)*	t_{DVR_Set}	-	20	-	µs	

(Note 1) Design guarantee

Electrical Characteristics – continued

Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
[Gamma Amplifier]						
P_UH, P_UL Output Voltage Range	V_{GAM_U}	3.0	-	V_{AVDD}	V	
P_LH, P_LL Output Voltage Range	V_{GAM_L}	0	-	V_{AVDD} -3.0	V	
P_UH Regulation Voltage *(Note 1)*	$V_{GAM\_UH\_R}$	16.796	16.816	16.836	V	V_{AVDD} =17.5V, DAC=F5h
P_UL Regulation Voltage *(Note 1)*	$V_{GAM\_UL\_R}$	9.277	9.297	9.317	V	V_{AVDD} =17.5V, DAC=87h
P_LH Regulation Voltage *(Note 1)*	$V_{GAM\_LH\_R}$	8.251	8.271	8.291	V	V_{AVDD} =17.5V, DAC=78h
P_LL Regulation Voltage *(Note 1)*	$V_{GAM\_LL\_R}$	1.142	1.162	1.182	V	V_{AVDD} =17.5V, DAC=10h
Output Voltage High *(Note 1)*	V_{GAM_H}	-	V_{AVDD} -0.2	-	V	No Load
Output Voltage Low *(Note 1)*	V_{GAM_L}	-	0.2	-	V	No Load
Short Circuit Current *(Note 1)*	I_{GAM_Source}	50	-	-	mA	
	I_{GAM_Sink}	-	-	-50	mA	
Load Regulation *(Note 1)*	LR_{GAM}	-3	-	+3	%	V_{OUT}=129/256 x V_{AVDD}, -10mA<I_{OUT}<+10mA
Integral Non Linearity *(Note 1)*	INL_{GAM}	-1	-	+1	LSB	
Differential Non Linearity *(Note 1)*	DNL_{GAM}	-1	-	+1	LSB	
[RESET]						
RESET Threshold Voltage	V_{RESET}	-	V_{FBB1} ×0.4	-	V	FBB1 Falling
		-	V_{FBB1} ×0.6	-	V	FBB1 Rising
CDLY Source Current	I_{CDLY}	4.25	5	5.75	µA	
CDLY Threshold Voltage	V_{CDLY}	1.215	1.35	1.485	V	CDLY Rising
CDLY Threshold Voltage Hysteresis	V_{CDLY_HYS}	0.3	0.4	0.5	V	
[VL Regulator]						
VL Regulation Voltage	V_{VL_R}	4.5	5.0	5.5	V	
VL Under Voltage Lockout Threshold Voltage	V_{VL_UVLO}	3.2	3.5	3.8	V	VL Falling
		3.8	4.1	4.4	V	VL Rising
VL Current Ability	I_{VL}	50	-	-	mA	
[General]						
VIN Under Voltage Lockout Threshold Voltage	V_{VIN_UVLO}	6.0	6.5	7.0	V	VIN12 Falling
		8.5	8.8	9.1	V	VIN12 Rising
AVDD Under Voltage Lockout Threshold Voltage	V_{AVDD_UVLO}	-	4.5	-	V	AVDD Falling
		-	5.0	-	V	AVDD Rising
Switching Frequency	f_{SW}	600	750	900	kHz	
VINH Quiescent Current	I_{QVINH}	-	0.3	-	mA	No Switching
VIN12 Quiescent Current	I_{QVIN12}	-	17	-	mA	No Switching
VIN3 Quiescent Current	I_{QVIN3}	-	0.2	-	mA	No Switching
VINN Quiescent Current	I_{QVINN}	-	0.2	-	mA	No Switching
EEPROM Write Cycles *(Note 1)*	EWC	1000	-	-	Times	
[Fault, PG]						
Pull Up Resistance	R_{FAULT}	100	-	-	kΩ	
High-level Input Voltage	V_{FAULT_IH}	2	-	-	V	
Low-level Input Voltage	V_{FAULT_IL}	-	-	1	V	
ON Voltage	V_{FAULT_L}	-	-	0.4	V	I_{IN} = 3mA
PG High Voltage	V_{PG_H}	VL-0.4	VL-0.1	VL-0.01	V	I_{OUT}=2mA
PG Low Voltage	V_{PG_L}	0.01	0.1	0.4	V	I_{OUT}=-2mA

(Note 1) Design guarantee

Electrical Characteristics – continued

Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
[Logic Input (TRDY, CTRL, WPN, LOGIC_EN, A0, SCL, SDA)]						
Logic Input High Voltage	V_{IH}	1.5	-	-	V	
Logic Input Low Voltage	V_{IL}	-	-	0.8	V	
TRDY Pull-down Resistance	R_{TRDY}	100	-	-	kΩ	
CTRL Pull-down Resistance	R_{CTRL}	100	-	-	kΩ	
WPN Pull-down Resistance	R_{WPN}	100	-	-	kΩ	
LOGIC_EN Pull-up Resistance	R_{LOGIC_EN}	100	-	-	kΩ	
A0 Pull-up Resistance	R_{A0}	100	-	-	kΩ	
SCL Input Current	I_{SCL}	-2	-	+2	μA	
SDA Input Current	I_{SDA}	-2	-	+2	μA	
SDA_ACK ON Voltage	V_{SDA_L}	-	-	0.4	V	I_{IN} = 3mA
[I^2C Interface]						
SCL Frequency	f_{SCL}	-	-	1000	kHz	
SCL High Time	t_{HIGH}	0.3	-	-	μs	
SCL Low Time	t_{LOW}	0.4	-	-	μs	
Rise Time	t_R	-	-	120	ns	Dependent on Load
Fall Time	t_F	-	-	120	ns	Dependent on Load
Start Condition Hold Time	$t_{HD:STA}$	0.25	-	-	μs	
Start Condition Setup Time	$t_{SU:STA}$	0.25	-	-	μs	
SDA Hold Time	$t_{HD:DAT}$	50	-	-	ns	
SDA Setup Time	$t_{SU:DAT}$	50	-	-	ns	
Acknowledge Delay Time	t_{PD}	-	-	0.35	μs	
Acknowledge Hold Time	t_{DH}	-	0.1	-	μs	
Stop Condition Setup Time	$t_{SU:STO}$	0.25	-	-	μs	
Bus Release Time	t_{BUF}	0.5	-	-	μs	
Noise Spike Width	t_I	-	50	-	ns	
I^2C Bus Capacitive Load *(Note 1)*	C_B	-	-	400	pF	

(Note 1) Design guarantee

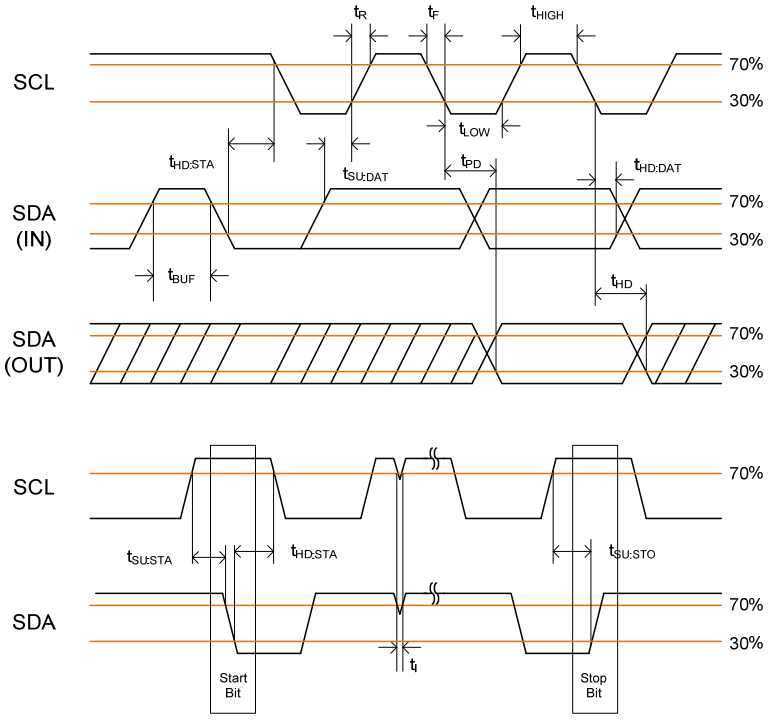


Figure 19. I2C Timing Diagram

Typical Performance Curves
Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

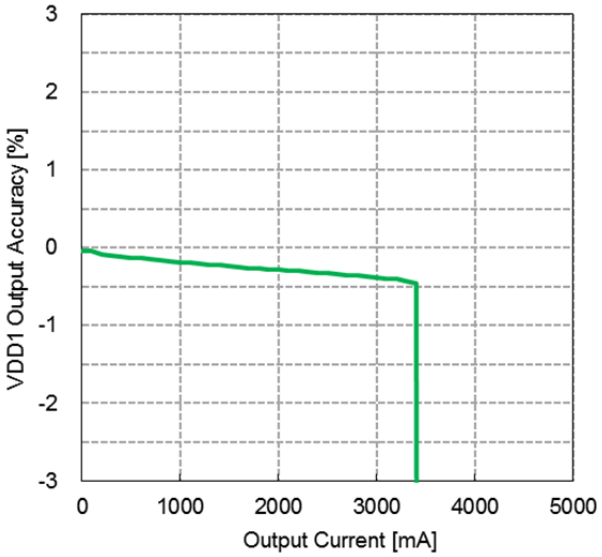


Figure 20. VDD1 Output Accuracy vs Output Current
("VDD1 Load Regulation", VDD1=3.3V)

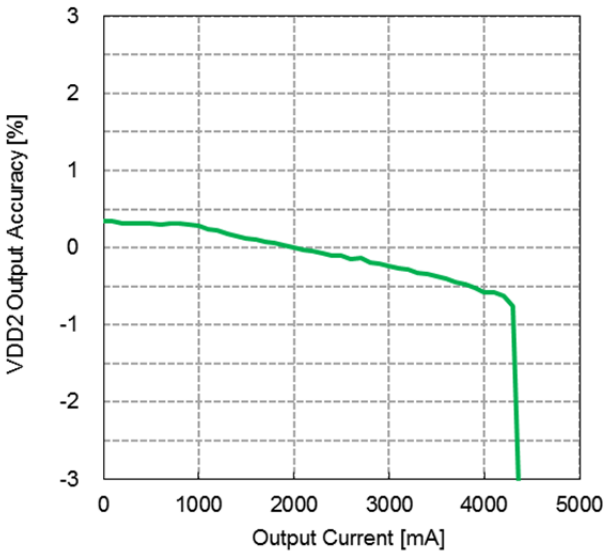


Figure 21. VDD2 Output Accuracy vs Output Current
("VDD2 Load Regulation", VDD2=1.8V)

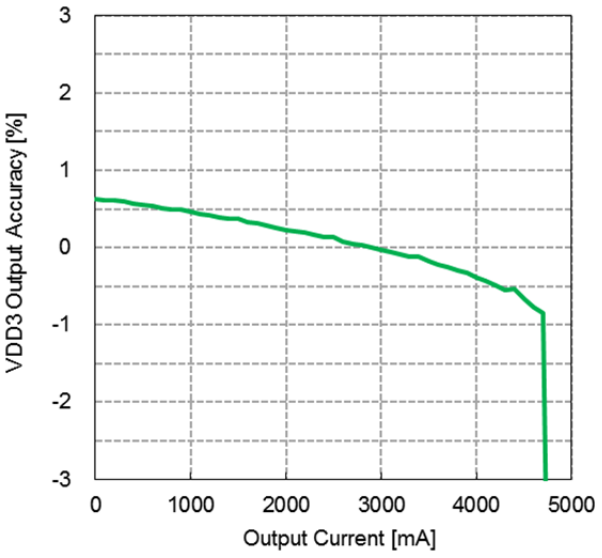


Figure 22. VDD3 Output Accuracy vs Output Current
("VDD3 Load Regulation", VDD3=1.0V)

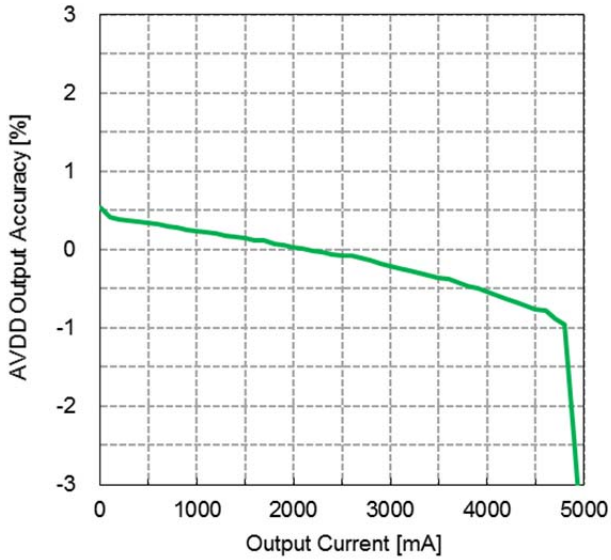


Figure 23. AVDD Output Accuracy vs Output Current
("AVDD Load Regulation", AVDD=17.5V, OCP 8A Setting)

Typical Performance Curves – continued

Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

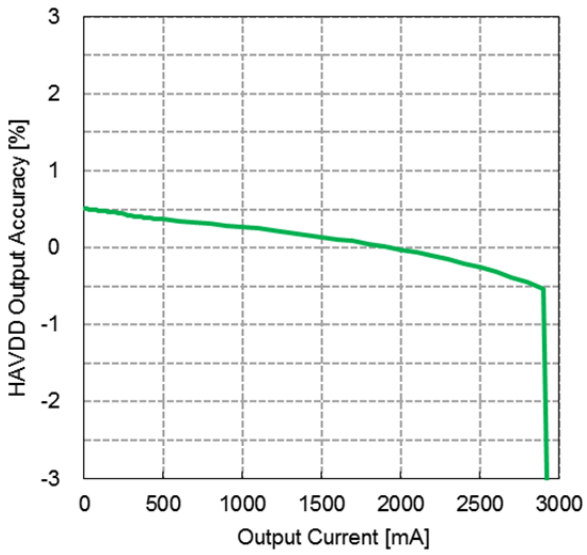


Figure 24. HAVDD Output Accuracy vs Output Current
("HAVDD Load Regulation", AVDD=17.5V, HAVDD=8.75V)
(Source)

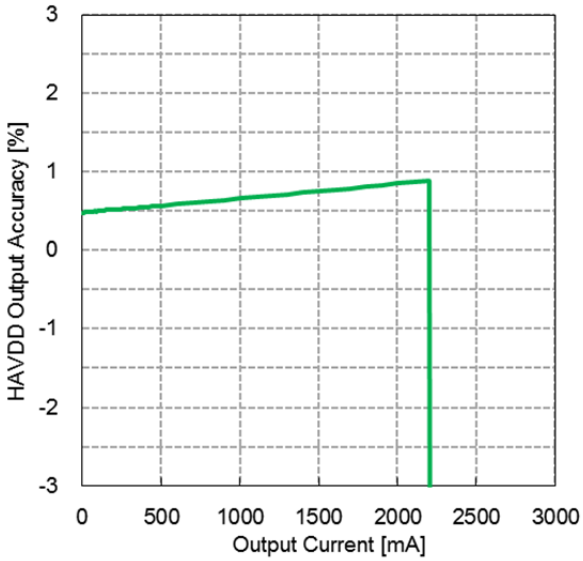


Figure 25. HAVDD Output Accuracy vs Output Current
("HAVDD Load Regulation", AVDD=17.5V, HAVDD=8.75V)
(Sink)

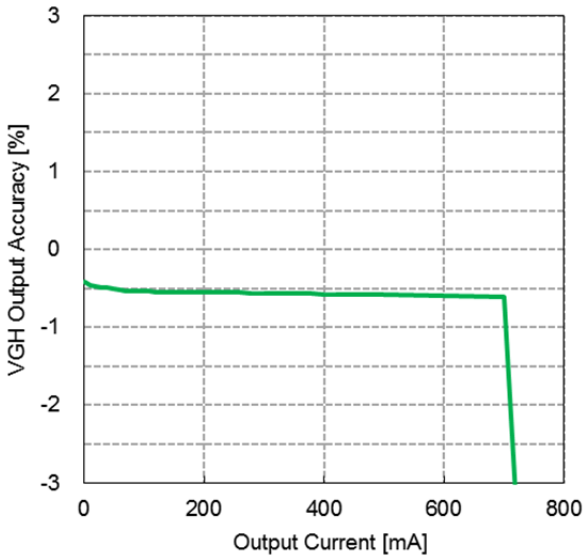


Figure 26. VGH Output Accuracy vs Output Current
("VGH Load Regulation", VGH=31.0V)

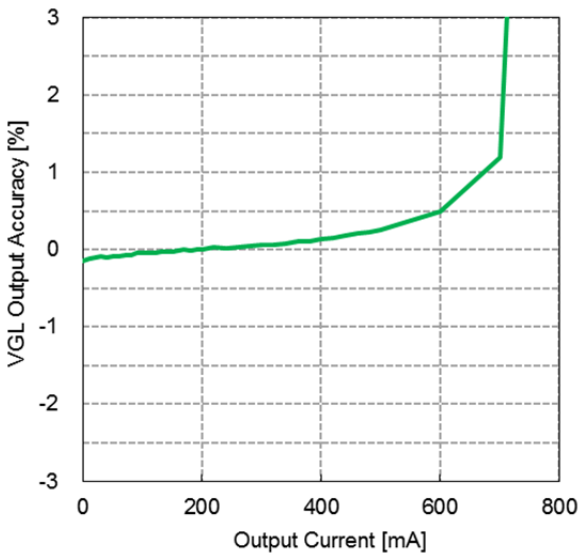


Figure 27. VGL Output Accuracy vs Output Current
("VGL Load Regulation", VGL=-12.0V)

Typical Performance Curves – continued
Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

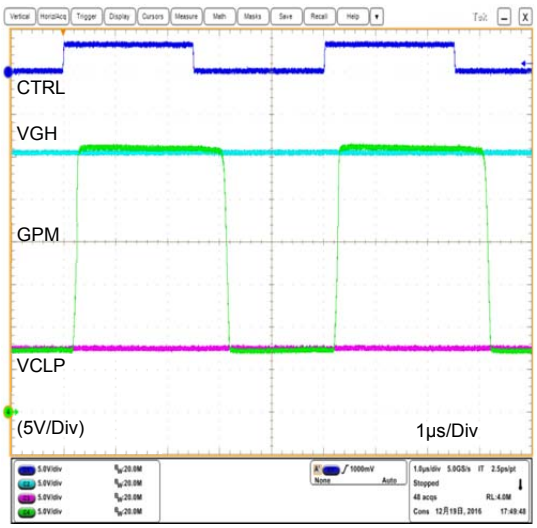


Figure 28. GPM Waveform(No Capacitance Load)

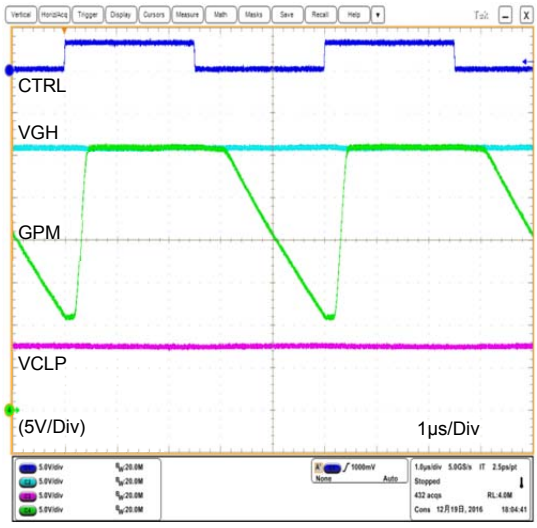


Figure 29. GPM Waveform(Capacitance Load 10nF)

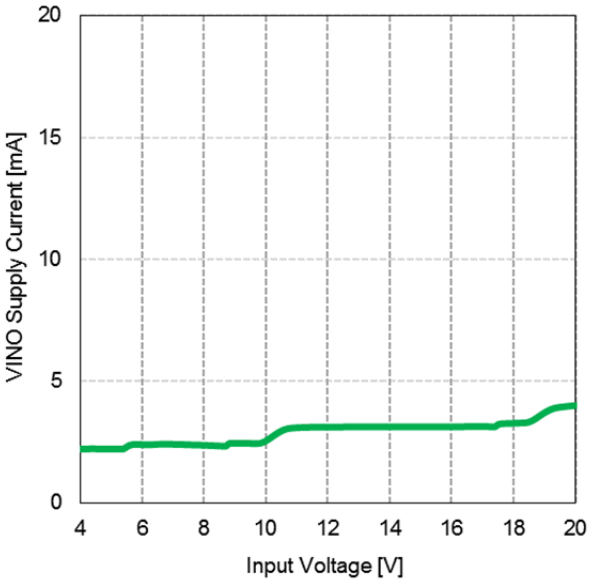


Figure 30. VINO Supply Current vs Input Voltage
(AVDD = 17.5V)

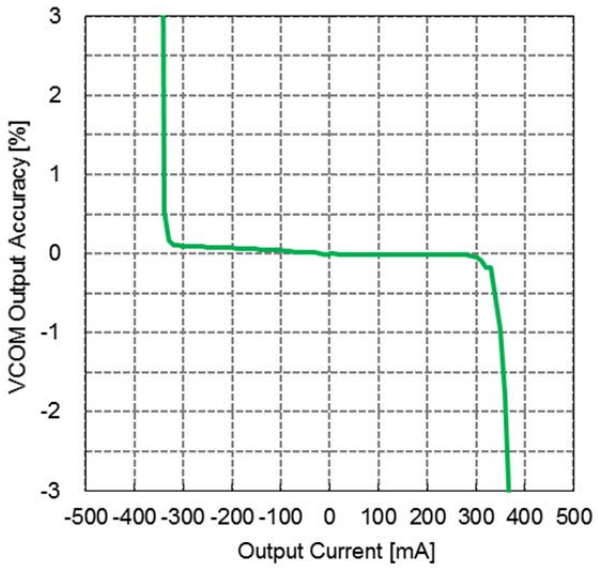


Figure 31. VCOM Output Accuracy vs Output Current
("VCOM Load Regulation", AVDD=17.5V, VCOM=AVDD/2)

Typical Performance Curves – continued
Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

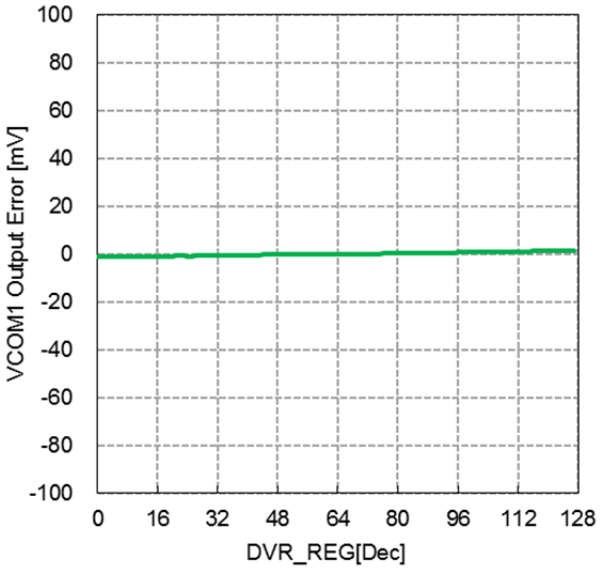


Figure 32. VCOM1 Output Error vs DVR_REG
(CREF=10.0V, DVR_RANGE=0.5V)

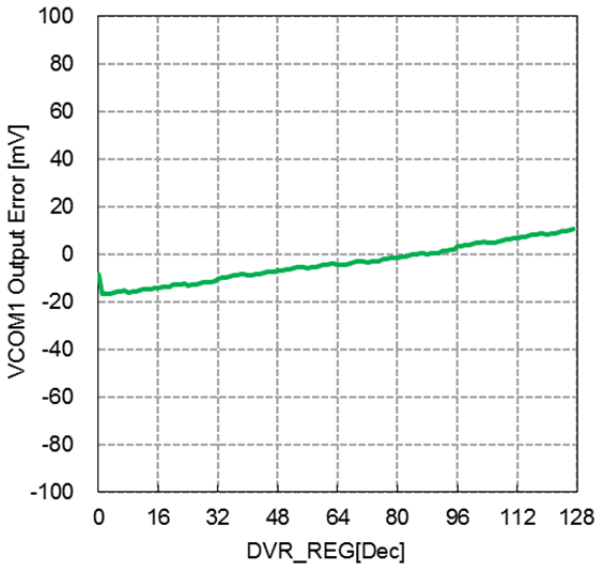


Figure 33. VCOM1 Output Error vs DVR_REG
(CREF=10.0V, DVR_RANGE=4.0V)

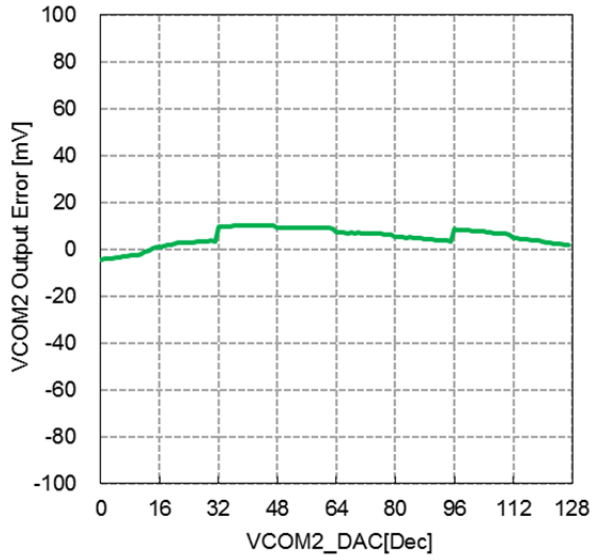


Figure 34. VCOM2 Output Error vs VCOM2_DAC
(CREF=10.0V, no DVR)

Typical Performance Curves – continued
Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

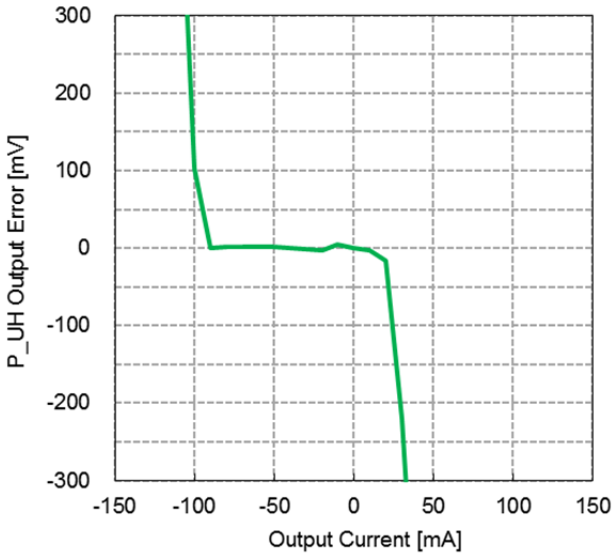


Figure 35. P_UH Output Error vs Output Current
("P_UH Load Regulation", AVDD=17.5V, P_UH=F5h)

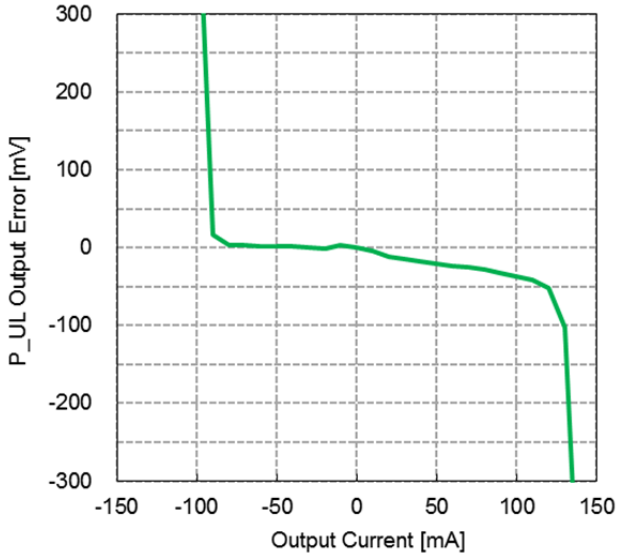


Figure 36. P_UL Output Error vs Output Current
("P_UL Load Regulation", AVDD=17.5V, P_UL=87h)

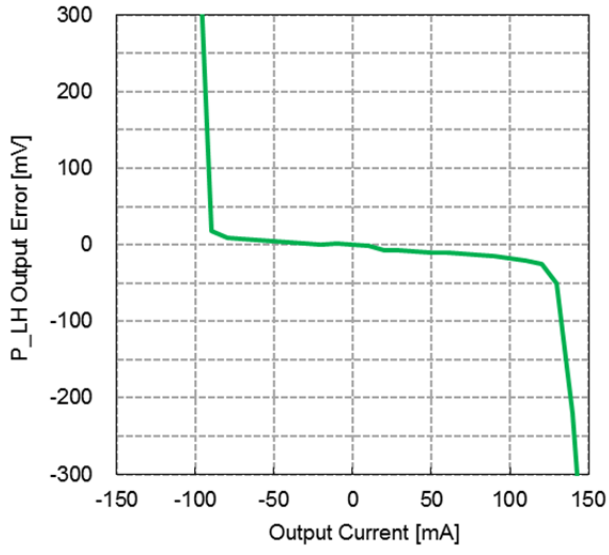


Figure 37. P_LH Output Error vs Output Current
("P_LH Load Regulation", AVDD=17.5V, P_LH=78h)

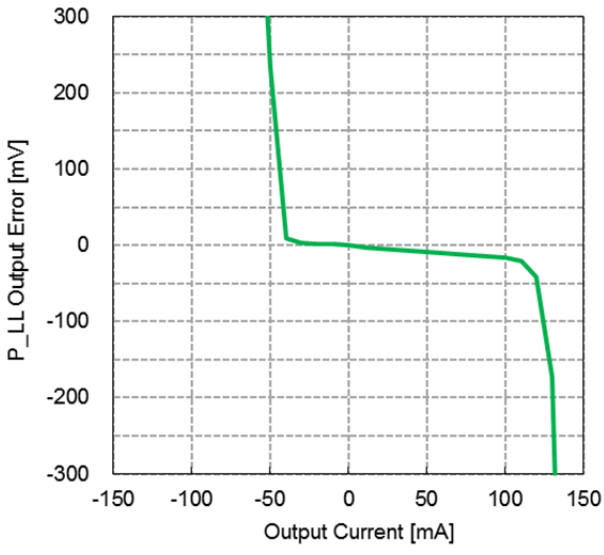


Figure 38. P_LL Output Error vs Output Current
("P_LL Load Regulation", AVDD=17.5V, P_LL=10h)

Typical Performance Curves – continued
Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

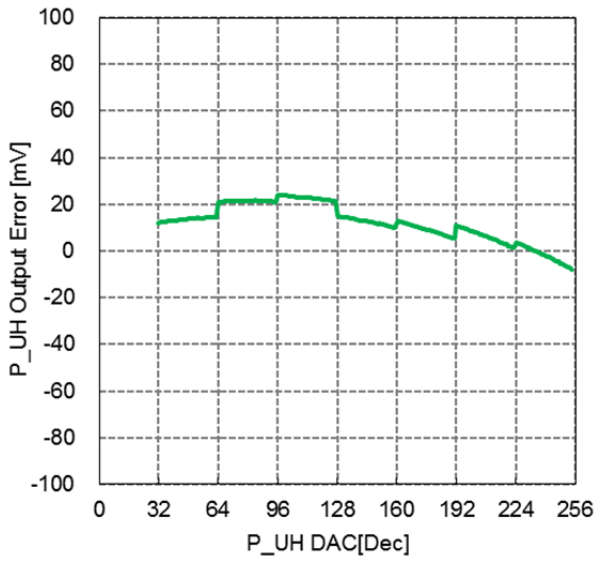


Figure 39. P_UH Output Error vs P_UH DAC
(AVDD=17.5V)

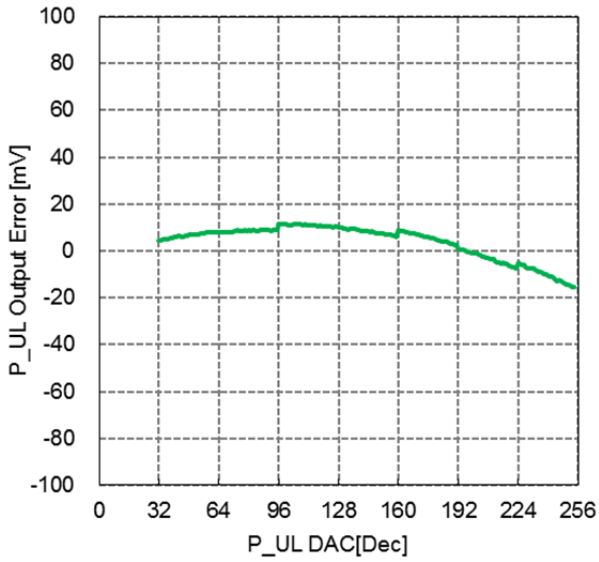


Figure 40. P_UL Output Error vs P_UL DAC
(AVDD=17.5V)

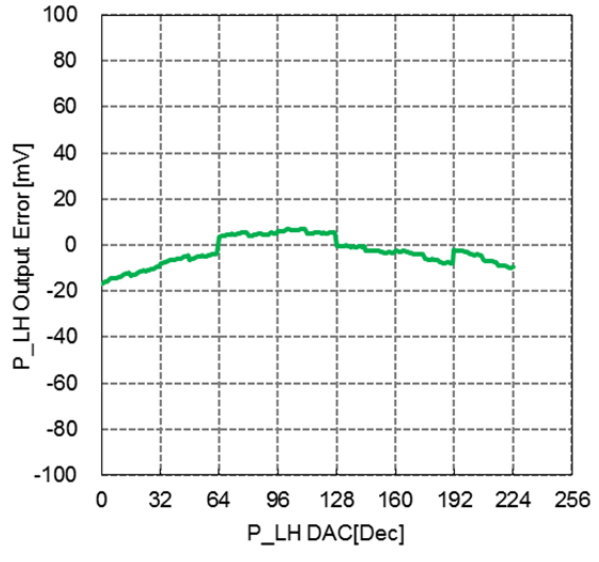


Figure 41. P_LH Output Error vs P_LH DAC
(AVDD=17.5V)

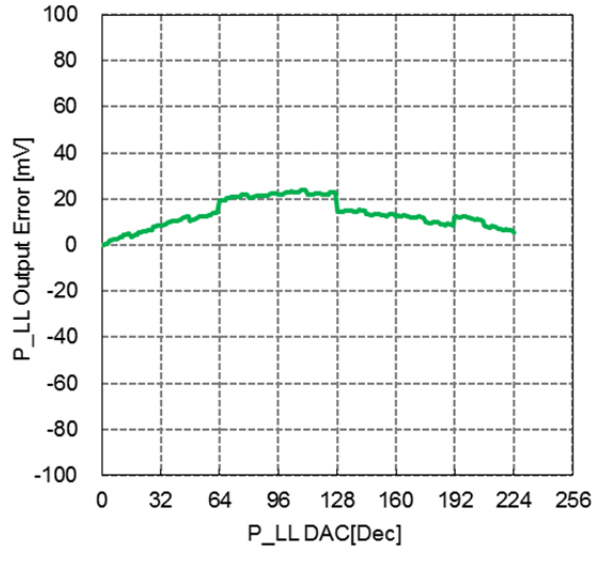


Figure 42. P_LL Output Error vs P_LL DAC
(AVDD=17.5V)

Typical Performance Curves – continued
Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

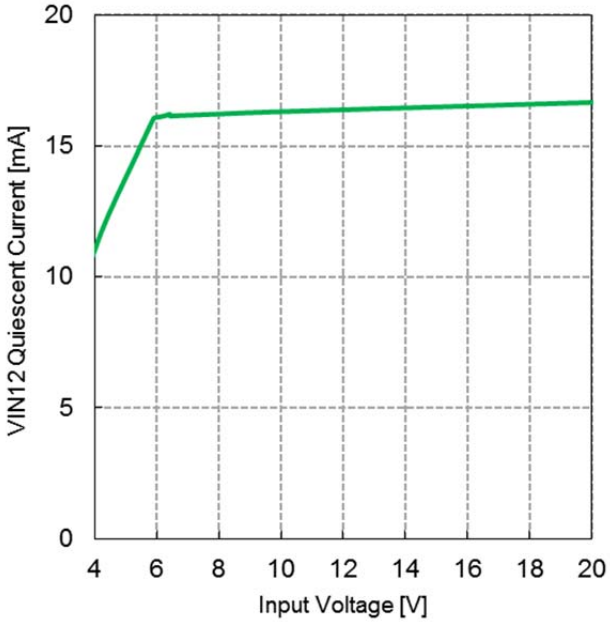


Figure 43. VIN12 Quiescent Current vs Input Voltage (No Switching)

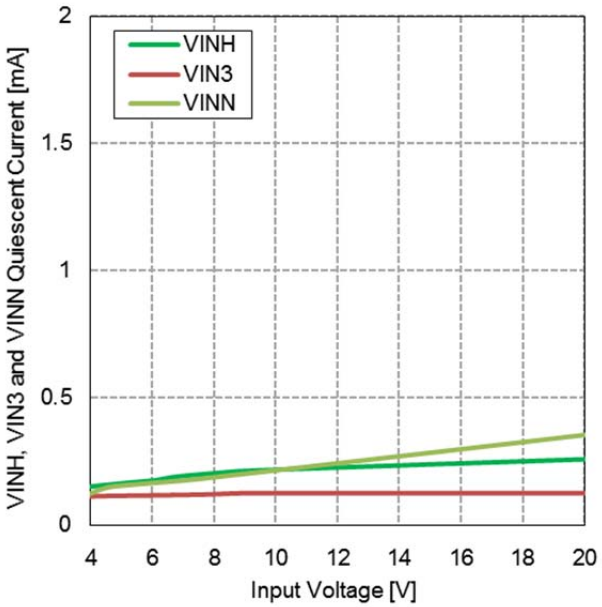


Figure 44. VINH, VIN3 and VINN Quiescent Current vs Input Voltage (No Switching)

Typical Performance Curves – continued
Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

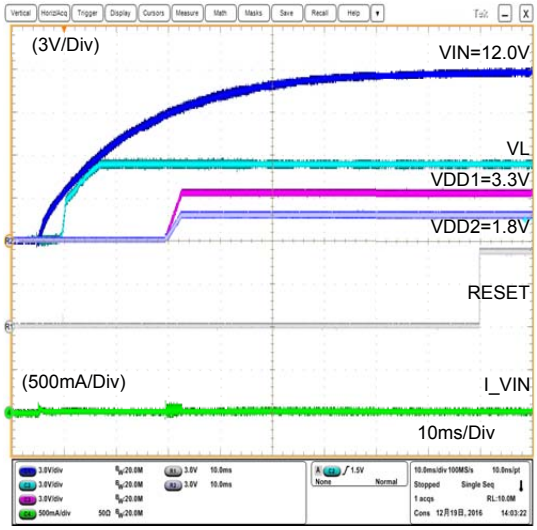


Figure 45. ON Waveform (VDD, RESET)

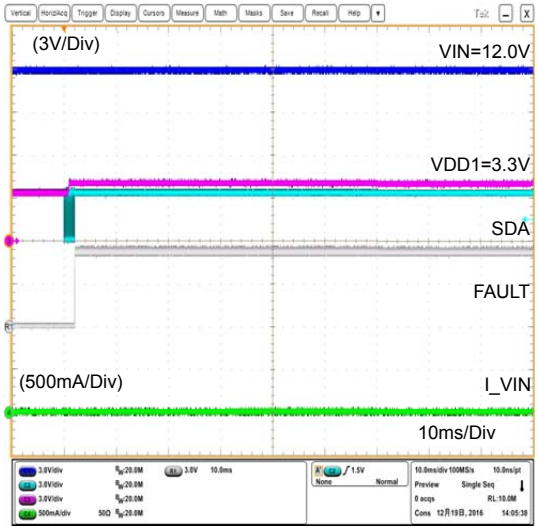


Figure 46. ON Waveform (FAULT)

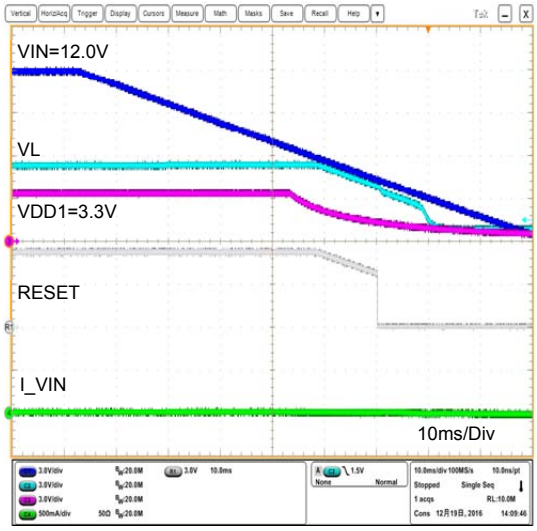


Figure 47. OFF Waveform (VDD, RESET)

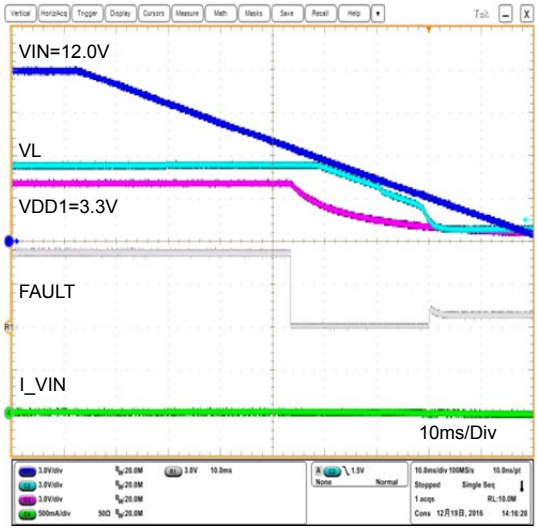


Figure 48. OFF Waveform (FAULT)

Typical Performance Curves – continued
Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

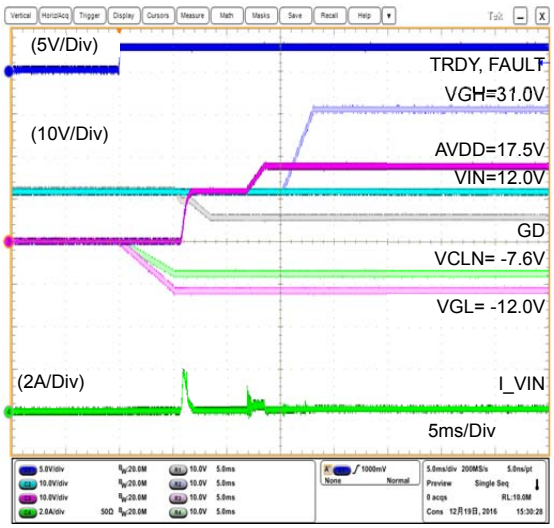


Figure 49. ON Waveform (AVDD, VGH, VGL)

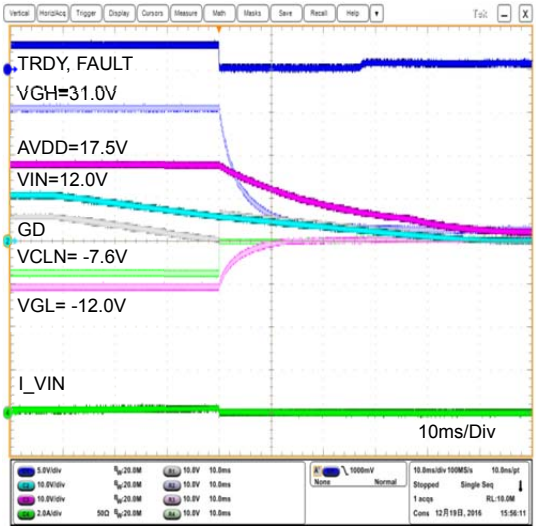


Figure 50. OFF Waveform (AVDD, VGH, VGL)

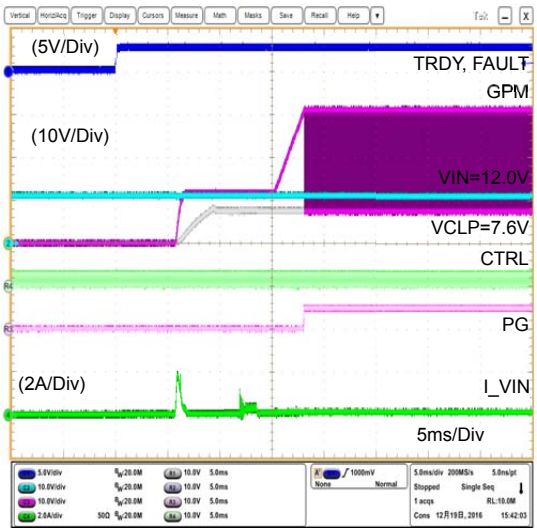


Figure 51. ON Waveform (GPM, PG)

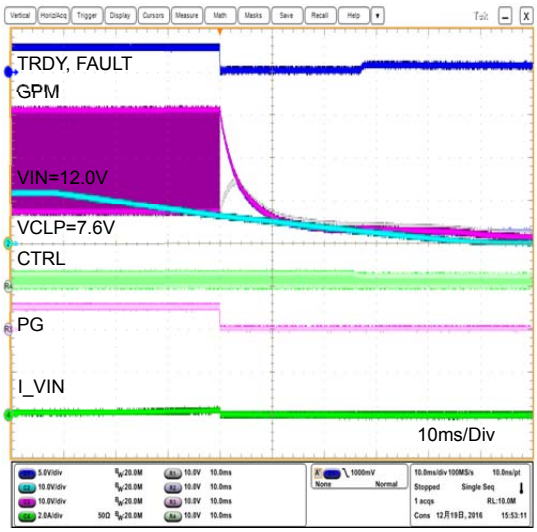


Figure 52. OFF Waveform (GPM, PG)

Typical Performance Curves – continued
Unless otherwise noted, VIN12=VIN3=VINN=VINO=12V and Ta=25°C

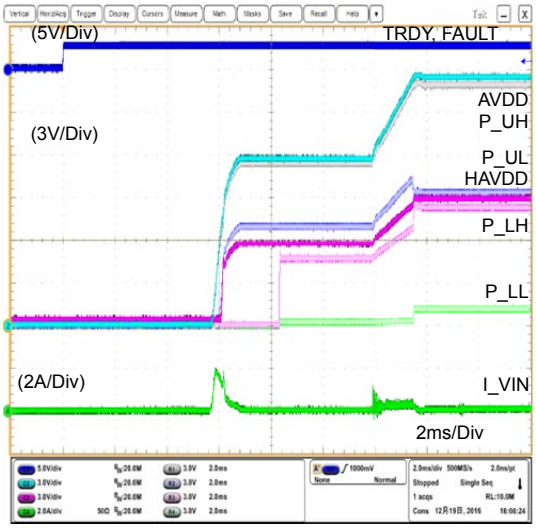


Figure 53. ON Waveform (Gamma)

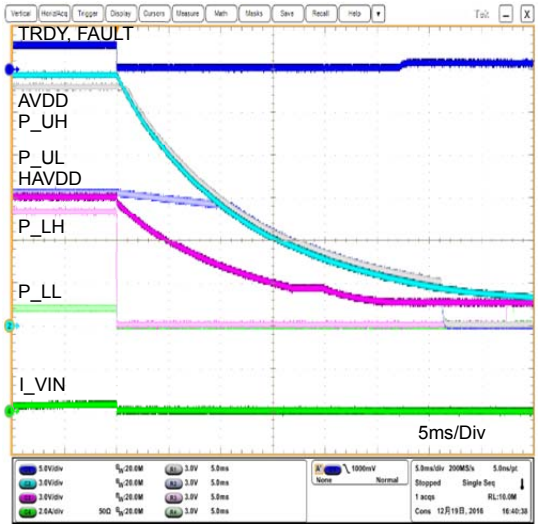


Figure 54. OFF Waveform (Gamma, HiZ)

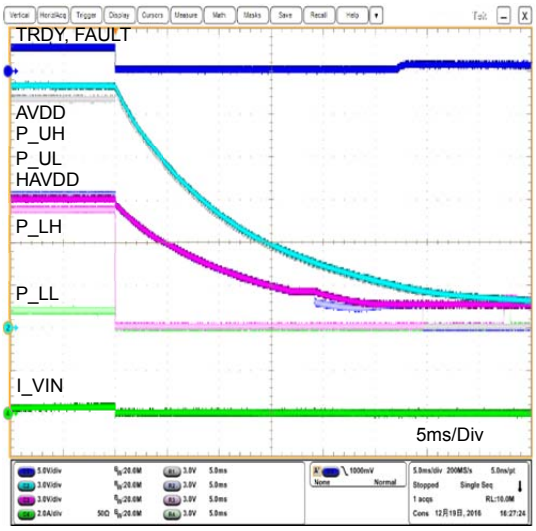


Figure 55. OFF Waveform (Gamma, Discharge)

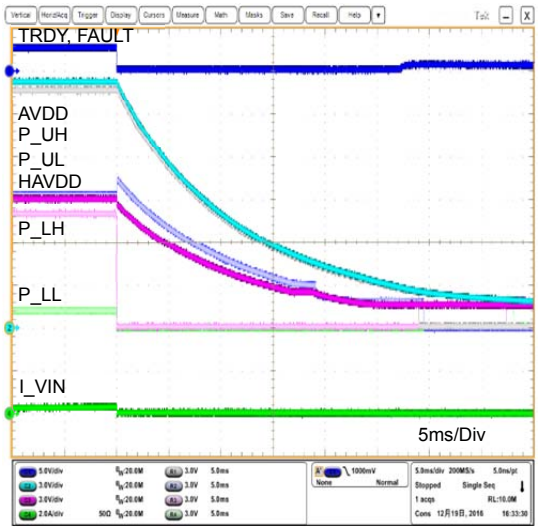


Figure 56. OFF Waveform (Gamma, Clamp)

Timing Chart

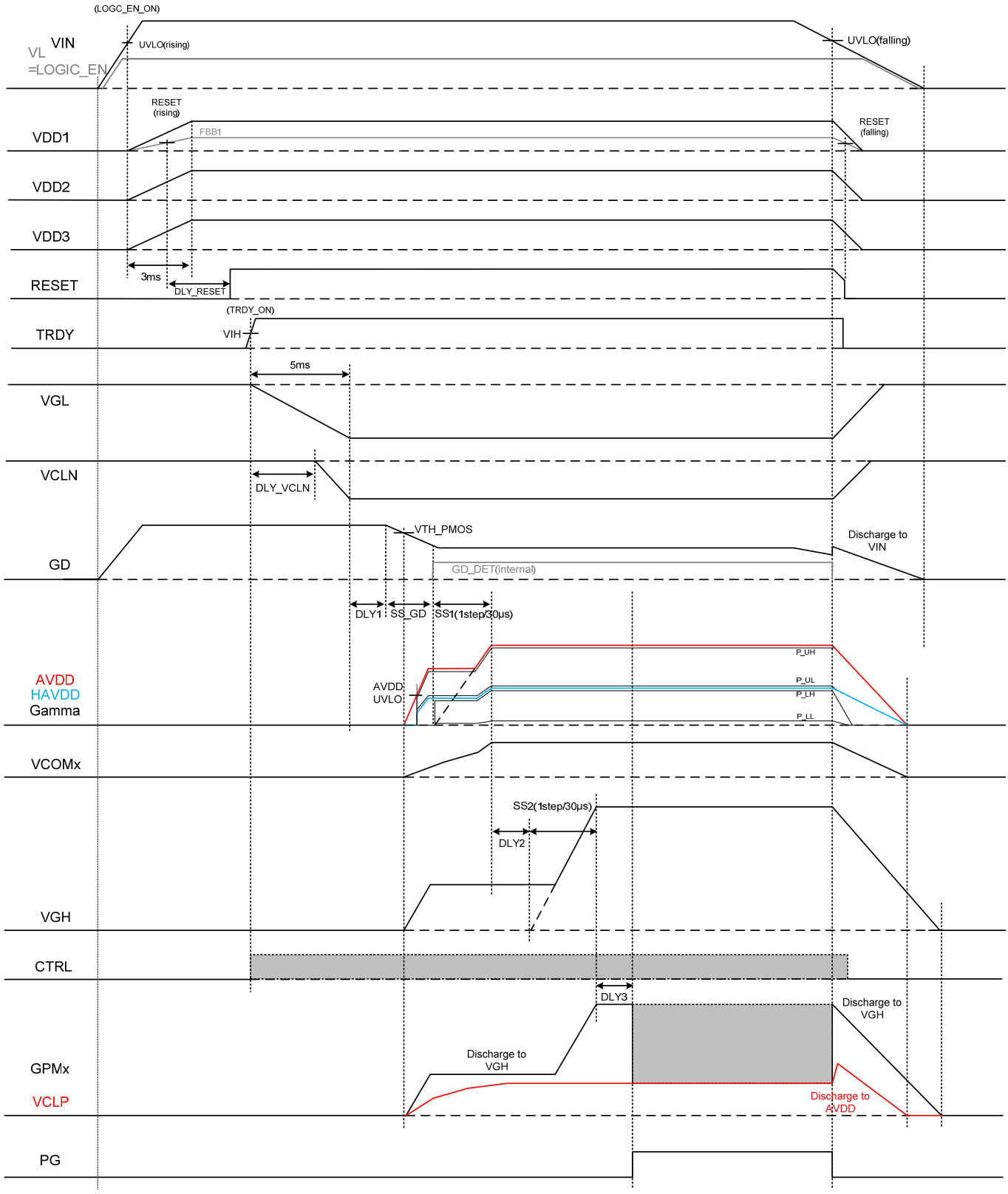


Figure 57. ON/OFF Sequence

Timing Chart – continued

ON Sequence

Once VIN supplied, VL activates. After VL_UVLO released, internal logic activates.
After VIN_UVLO is released and LOGIC_EN=H, VDD1, VDD2 and VDD3 activates.
The soft-start time of VDD1, VDD2 and VDD3 is 3ms(Typ). After soft-start ends, the output is default setting.
If setting is changed with I2C command, VDD1, VDD2 and VDD3 goes to the setting value with 10µs/step.

With conditons of FAULT=H and TRDY=H, the outputs except VDD1, VDD2, VDD3 activate. (TRDY_ON state)
VGL activates immediately in TRDY_ON state and reaches the setting value after soft-start time of 5ms(Typ).
VCLN activates after DLY_VCLN and reaches the setting value in 5ms(Typ) of TRDY_ON state.

After DLY1 from VGL soft-start ends, PMOS load switch activates.
After the GD pin voltage falls and GD-VIN voltage reaches Vth level of PMOS load switch,
AVDD and VGH output start rising. Finally, AVDD and VGH output is the same level of VIN via the inductance and diode.
After the GD pin is clamped by the internal circuit and GD_DET =H,
AVDD internal reference activates and reaches the setting value after soft-start time of SS1.
SS1 depends on the output setting. For example, when AVDD=17V, SS1 is 17V / 0.1V × 30µs = 5.1ms(Typ).
VCLP and VCOM operate following AVDD output.

After AVDD output rises and AVDD_UVLO is released, P_UH, P_UL and HAVDD activates.
P_UH start with 97% of AVDD and goes to the setting value after SS1 ends.
P_UL start with 60% of AVDD and goes to the setting value after SS1 ends.
HAVDD start with 50% of AVDD and goes to the setting value after SS1 ends.
(Each P_UH and P_UL output at the start timing is resister diveder valule between AVDD and HAVDD.)

After GD_DET=H, P_LH and P_LL activates.
P_LH start with 40% of AVDD and goes to the setting value after SS1 ends.
P_LL start with 2% of AVDD and goes to the setting value after SS1 ends.
(Each P_LH and P_LL output at the start timing is resister diveder valule between HAVDD and GND.)

After DLY2 from AVDD soft-start ends, VGH internal reference activates and reaches the setting value after soft-start time of SS2. SS2 depends on the output setting. For example, when VGH=31V, SS2 is 31V / 0.2V × 30µs = 4.65ms(Typ).

After DLY3 from VGH soft-start ends, GPM function activates and PG=H.

OFF Sequence

The outputs except P_UH, P_UL and HAVDD are shutdown when VIN_UVLO is detected.

BLOCK	Discharge to
VDD1	GND
VDD2	
VDD3	
VCLN	
VGL	
GD	VIN
AVDD	GND
P_LH	
P_LL	
VGH	
GPM	VGH
VCLP	AVDD

P_UH, P_UL and HAVDD keep operating until AVDD_UVLO is detected.
HAVDD output is 50% of AVDD. P_UH and P_UL operations depends on the register setting.
At the end of the sequence, when AVDD_UVLO is detected, these output are discharged to GND with output load and internal discharge resistors.

P-Gamma Discharge 30h[6]	P-Gamma Option 2Dh[6]	P_UH	P_UL
0: Disable	-	HiZ	HiZ
1: Enable	0: Discharge	Discharge to AVDD	Discharge to HAVDD
1: Enable	1: Clamp	97% of AVDD	60% of AVDD

Serial Communication

BM81006MWW slave addresses are shown below.

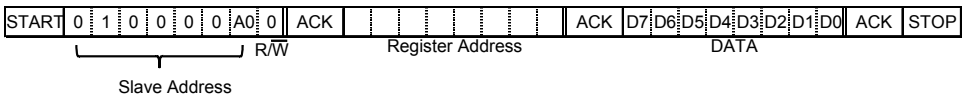
Slave Address	Function
40h, 41h, 42h, 43h	Write or Read to Main Register
9Eh, 9Fh	Write or Read to DVR Register
52h, 53h, 6Ah, 6Bh	Write or Read to Test Register*(Note 1)*

(Note 1) IC returns Acknowledgement (ACK) but no change to IC operations.

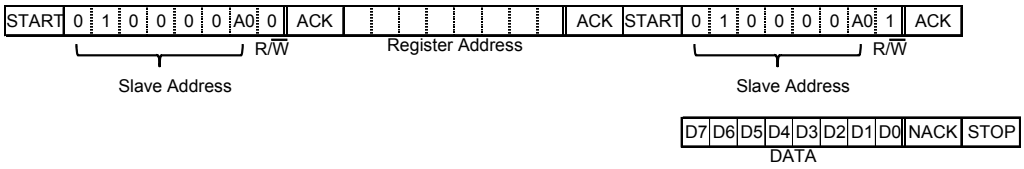
1. Communication Protocol (Main Register)

Single Mode

<Single I2C Register Write Protocol >

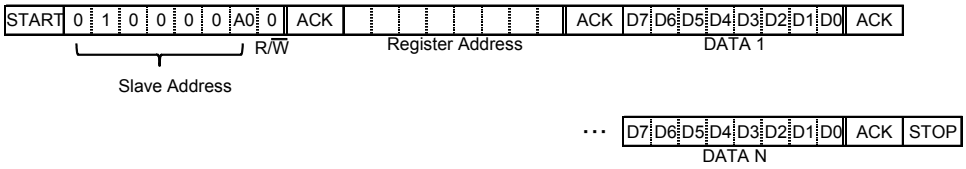


<Single I2C Register Read Protocol >

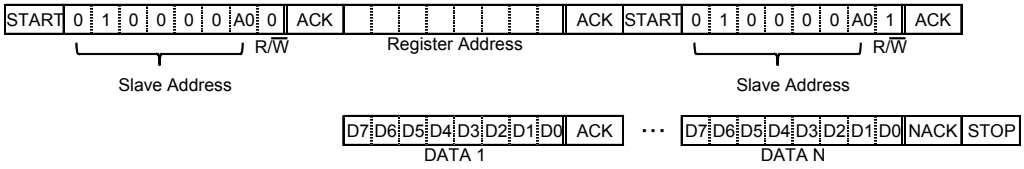


Multiple Mode

< Multiple I2C Register Write Protocol >

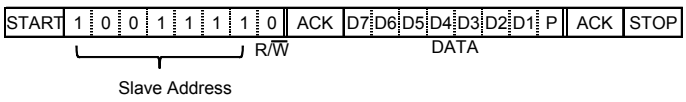


< Multiple I2C Register Read Protocol >



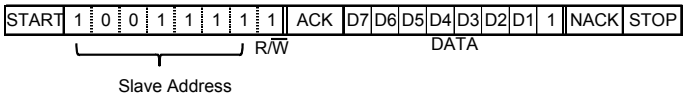
2. Communication Protocol (DVR Register)

< I2C Register Write Protocol>



P=1 : Write to Register ONLY
WPN=H & P=0 : Write to Register and EEPROM

< I2C Register Read Protocol >



Main Register Map

Register Address	Bits	Register	Resolution / Range	Default
00h	8	AVDD	0.1V(13.5V to 19.4V) (86h to C1h)	00h
01h	8	HAVDD	0.05V(6.75V to 9.7V) (86h to C1h)	00h
02h	8	[7:1] DVR_MAX [0] DVR Connection	[7:1] AVDD/128 [AVDD to AVDD/128] [0] 0: Disable 1: Enable	00h
03h	8	-	FFh	00h
04h	8	[7] POS2 Connection [6:0] VCOM2_DAC	[7] 0: AVDD/CREF 1: POS1 [6:0] POS2/128 (POS2/128 to POS2)	00h
05h	8	-	7Eh	7Eh
06h	8	Gamma U_H	AVDD/256 [AVDD/256 to AVDD]	00h
07h	8	Gamma U_L	AVDD/256 [AVDD/256 to AVDD]	00h
08h	8	Gamma L_H	AVDD/256 [AVDD/256 to AVDD]	00h
09h	8	Gamma L_L	AVDD/256 [AVDD/256 to AVDD]	00h
0Ah	8	VGH	0.2V (15V to 45V) (4Ah to E0h)	00h
0Bh	8	VCLP	VCLP, GPM Disable (00h) 0.2V (3V to 20V) (0Eh to 63h)	00h
0Ch	8	VGL	0.2V(-2V to -22V) (09h to 6Dh)	00h
0Dh	8	VCLN	VCLN Disable (00h) 0.2V(-2V to -20V) (09h to 63h)	00h
0Eh	8	-	00h	00h
0Fh	8	-	00h	00h
10h	8	FBB1	0.01V (0.4V to 2.0V) (27h to C7h), default: 1.65V	A4h
11h	8	FBB2	0.01V (0.4V to 2.0V) (27h to C7h), default: 0.90V	59h
12h	8	FBB3	0.01V (0.4V to 2.0V) (27h to C7h), default: 0.90V	59h
13h	8	VGH Low Temp	0.2V (15V to 45V) (4Ah to E0h)	00h
14h	8	-	63h	00h
15h	8	-	2Ch	00h
16h	8	-	18h	00h
17h	8	-	AEh	00h
18h	8	-	AEh	00h
19h	8	-	7Eh	00h
1Ah	8	-	3Fh	00h
1Bh	8	-	3Fh	00h
1Ch	8	-	7Eh	7Eh
1Dh	8	-	F5h	00h
1Eh	8	-	87h	00h
1Fh	8	-	78h	00h
20h	8	-	10h	00h
21h	8	-	9Ah	00h
22h	8	-	25h	00h
23h	8	-	3Bh	00h
24h	8	-	25h	00h
25h	8	-	31h	00h
26h	8	-	00h	00h
27h	8	-	00h	0Dh
28h	8	-	F0h	F0h
29h	8	[7:4] LTC Voltage High V2 [3:0] LTC Voltage Low V1	133mV x 2 x FBB1 / 3.3V 133mV x 2 x FBB1 / 3.3V If FBB1 =1.65V, 133mV step 0.5V to 2.5V. If V1≥V2, Wrong_DATA function.	F0h
2Ah	8	[7] - [6:4] DVR_RANGE [3:0] AVDD Delay 1 time	[7] 0 [6:4] 0.5V (0.5V to 4.0V) [3:0] 20ms (0ms to 300ms)	00h
2Bh	8	[7:4] VGH Delay 2 time [3:0] GPM Delay 3 time	[7:4] 5.0ms (0ms to 75ms) [3:0] 5.0ms (0ms to 75ms)	00h

Main Register Map – continued

Register Address	Bits	Register	Resolution / Range	Default
2Ch	8	[7:4] VCLN Delay Time [3:0] -	[7:4] 0.3ms(0ms to 4.5ms) [3:0] 0000	00h
2Dh	8	[7] VCOM_REF [6] P-Gamma Discharge Option [5:4] AVDD External Slew Rate [3:2] AVDD Slew Control Select [1:0] VGH External FET Slew Rate	[7] 0: AVDD 1: CREF [6] 0: Discharge 1: Clamp [5:4] 00: 10Ω 01: 20Ω 10: 40Ω 11: 80Ω [3:2] 00: Both 01: Rising 10: Falling 11: Both [1:0] 00: 10Ω 01: 20Ω 10: 40Ω 11: 80Ω	00h
2Eh	8	[7:6] VGL Switching Slew Rate [5:4] VDD1 Switching Slew Rate [3:2] VDD2 Switching Slew Rate [1:0] VDD3 Switching Slew Rate	[7:6] 00: 100%(default) 01: 85% 10: 70% 11: 55% [5:4] 00: 100%(default) 01: 85% 10: 70% 11: 55% [3:2] 00: 100%(default) 01: 85% 10: 70% 11: 55% [1:0] 00: 100%(default) 01: 85% 10: 70% 11: 55%	00h
2Fh	8	-	20h	20h
30h	8	[7] - [6] P-Gamma Discharge [5:0] -	[7] 0 [6] 0: Disable 1: Enable [5:0] 01_0000	50h
31h	8	[7:5] VGH OCP Level [4:0] -	[7:5] 0.25A (0.5A to 2.25A) [4:0] 0_0001	00h
32h	8	[7] - [6] AVDD OCP Select [5:3] - [2:0] AVDD COMP Resister Select	[7] 0 [6] 0: 5A(Min) 1: 8A(Min) [5:3] 111 [2:0] 000: 0kΩ 001: 10kΩ 010: 14kΩ 011: 18kΩ 100: 24kΩ 101: 30kΩ 110: 44kΩ 111: 60kΩ	3Ch
33h	8	-	00h	00h
34h	8	[7] VGH LTC [6:1] - [0] Start-up Enable	[7] 0: ON 1: OFF [6:1] 111_111 [0] 0: Disable 1: Enable	02h

Application Example

(TOP VIEW)

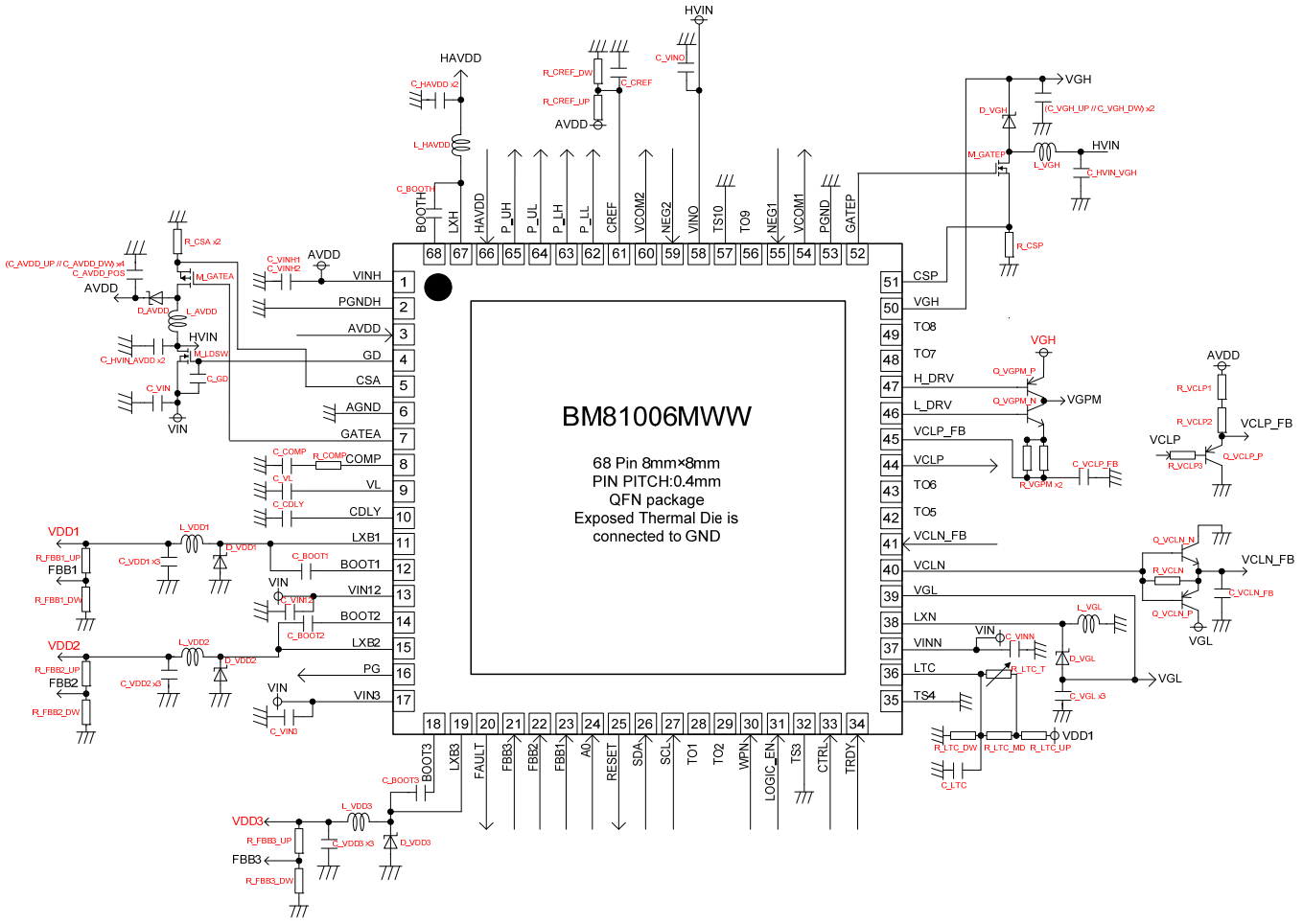


Figure 58. Application Example

Block	Symbol	Value	Size	Maker	Part Number
VDD1	C_VIN12	10μF	2012	murata	GRM21BR61E106KA73
	C_VDD1_1	22μF	1608	murata	GRM188B30J226MEA0
	C_VDD1_2	22μF	1608	murata	GRM188B30J226MEA0
	C_VDD1_3	22μF	1608	murata	GRM188B30J226MEA0
	L_VDD1	10μH	6.0 x 6.0 x 2.8	Taiyo Yuden	NRS6028T100MMGK
	D_VDD1	-	PMDS	ROHM	RSX301L-30TE25
	R_FBB1_UP	10kΩ	1608	ROHM	MCR03EZPFX1002
	R_FBB1_DW	10kΩ	1608	ROHM	MCR03EZPFX1002
	C_BOOT1	0.1μF	1005	murata	GRM155B31H104KE14
VDD2	C_VDD2_1	22μF	1608	murata	GRM188B30J226MEA0
	C_VDD2_2	22μF	1608	murata	GRM188B30J226MEA0
	C_VDD2_3	22μF	1608	murata	GRM188B30J226MEA0
	L_VDD2	10μH	6.0 x 6.0 x 2.8	Taiyo Yuden	NRS6028T100MMGK
	D_VDD2	-	PMDS	ROHM	RSX301L-30TE25
	R_FBB2_UP	10kΩ	1608	ROHM	MCR03EZPFX1002
	R_FBB2_DW	10kΩ	1608	ROHM	MCR03EZPFX1002
	C_BOOT2	0.1μF	1005	murata	GRM155B31H104KE14

Application Example – continued

Block	Symbol	Value	Size	Maker	Part Number
VDD3	C_VIN3	10μF	2012	murata	GRM21BR61E106KA73
	C_VDD3_1	22μF	1608	murata	GRM188B30J226MEA0
	C_VDD3_2	22μF	1608	murata	GRM188B30J226MEA0
	C_VDD3_3	22μF	1608	murata	GRM188B30J226MEA0
	L_VDD3	10μH	6.0 x 6.0 x 2.8	Taiyo Yuden	NRS6028T100MMGK
	D_VDD3	-	PMDS	ROHM	RSX301L-30TE25
	R_FBB3_UP	10kΩ	1608	ROHM	MCR03EZPFX1002
	R_FBB3_DW	10kΩ	1608	ROHM	MCR03EZPFX1002
	C_BOOT3	0.1μF	1005	murata	GRM155B31H104KE14
AVDD	C_AVDD_UP1	10μF	2012	murata	GRM21BR61E106KA73
	C_AVDD_DW1	10μF	2012	murata	GRM21BR61E106KA73
	C_AVDD_UP2	10μF	2012	murata	GRM21BR61E106KA73
	C_AVDD_DW2	10μF	2012	murata	GRM21BR61E106KA73
	C_AVDD_UP3	10μF	2012	murata	GRM21BR61E106KA73
	C_AVDD_DW3	10μF	2012	murata	GRM21BR61E106KA73
	C_AVDD_UP4	10μF	2012	murata	GRM21BR61E106KA73
	C_AVDD_DW4	10μF	2012	murata	GRM21BR61E106KA73
	C_AVDD_POS	33μF	7343	Panasonic	25TQC33MYF
	C_VIN	10μF	2012	murata	GRM21BR61E106KA73
	C_GD	0.1μF	1005	murata	GRM155B31H104KE14
	M_LDSW	Pch FET	HSMT8	ROHM	RQ3E120AT
	C_HVIN_AVDD1	10μF	2012	murata	GRM21BR61E106KA73
	C_HVIN_AVDD2	10μF	2012	murata	GRM21BR61E106KA73
	L_AVDD	10μH	11.2 x 10.0 x 4.0	murata	FDVE1040-H-100M
	M_GATEA	Nch FET	HSOP8	ROHM	RS1E130GNTB
	D_AVDD	-	CPD	ROHM	RBR10BM40
	R_CSA1	0.1Ω	3216	ROHM	MCR18EZHFLR100
	R_CSA2	0.1Ω	3216	ROHM	MCR18EZHFLR100
	R_COMP	short	-	-	-
	C_COMP	2.2nF	1608	murata	GRM188B11H222KA01
HAVDD	C_VINH1	10μF	2012	murata	GRM21BR61E106KA73
	C_VINH2	10μF	2012	murata	GRM21BR61E106KA73
	C_HAVDD1	10μF	2012	murata	GRM21BR61E106KA73
	C_HAVDD2	10μF	2012	murata	GRM21BR61E106KA73
	L_HAVDD	6.8μH	6.0 x 6.0 x 2.8	Taiyo Yuden	NRS6028T6R8MMGJ
	C_BOOTH	0.1μF	1608	murata	GRM188B11E104KA01

Application Example – continued

Block	Symbol	Value	Size	Maker	Part Number
VGH	C_VGH_UP1	10µF	2012	murata	GRM21BR61E106KA73
	C_VGH_DW1	10µF	2012	murata	GRM21BR61E106KA73
	C_VGH_UP2	10µF	2012	murata	GRM21BR61E106KA73
	C_VGH_DW2	10µF	2012	murata	GRM21BR61E106KA73
	C_HVIN_VGH	10µF	2012	murata	GRM21BR61E106KA73
	L_VGH	22µH	6.0 x 6.0 x 2.8	Taiyo Yuden	NRS6028T220MMGJ
	M_GATEP	Nch FET	TSMT3	ROHM	RSR030N06TL
	D_VGH	-	TUMD2M	ROHM	RB160VAM-60TR
	R_CSP	0.1Ω	3216	ROHM	MCR18EZHFLR100
LTC	R_LTC_DW	15kΩ	1608	ROHM	MCR03EZPFX1502
	R_LTC_MD	30kΩ	1608	ROHM	MCR03EZPFX3002
	R_LTC_UP	Short	-	-	-
	R_LTC_T	33kΩ	1608	murata	NCP18WB333J03RB
	C_LTC	0.1µF	1608	murata	GRM188B11E104KA01
VGL	C_VINN	10µF	2012	murata	GRM21BR61E106KA73
	C_VGL1	1µF	1608	murata	GRM188B31E105KA75*(Note 1)*
	C_VGL2	10µF	2012	murata	GRM21BB31E106KA73*(Note 1)*
	C_VGL3	10µF	2012	murata	GRM21BB31E106KA73*(Note 1)*
	D_VGL	-	TUMD2M	ROHM	RB160VAM-60TR
	L_VGL	22µH	6.0 x 6.0 x 2.8	Taiyo Yuden	NRS6028T220MMGJ
VCLN	Q_VCLN_N	NPN Bip	MPT3	ROHM	2SCR513P5T100
	Q_VCLN_P	PNP Bip	MPT3	ROHM	2SAR513P5T100
	R_VCLN	1kΩ	1608	ROHM	MCR03EZPFX1001
	C_VCLN_FB	2.2µF	1608	murata	GRM188R61E225KA12
VGPM	Q_VGPM_P	PNP Bip	TO-252	ROHM	2SAR573D3TL1
	Q_VGPM_N	NPN Bip	TO-252	ROHM	2SCR573D3TL1
	R_VGPM1	10Ω	2012	ROHM	MCR10EZPF10R0
	R_VGPM2	10Ω	2012	ROHM	MCR10EZPF10R0
VCLP	R_VCLP1	1kΩ	1608	ROHM	MCR03EZPFX1001
	R_VCLP2	510Ω	1608	ROHM	MCR03EZPFX5100
	R_VCLP3	100Ω	1608	ROHM	MCR03EZPFX1000
	C_VCLP_FB	1µF	1608	murata	GRM188B31E105KA75
	Q_VCLP_P	PNP Bip	TO-252	ROHM	2SAR573D3TL1
VCOM	C_VINO	10µF	2012	murata	GRM21BR61E106KA73
	R_CREF_UP	10kΩ	1608	ROHM	MCR03EZPFX1002
	R_CREF_DW	10kΩ	1608	ROHM	MCR03EZPFX1002
	C_CREF	1µF	1608	murata	GRM188B31E105KA75
RESET	C_CDLY	0.22µF	1608	murata	GRM188B31H224KAC4
Common	C_VL	2.2µF	1608	murata	GRM188B31C225KE14

(Note 1) It is necessary to change ratings, depending on output voltage setting

Selection of Components Externally Connected

1. Buck Converter(VDD1/VDD2/VDD3/HAVDD)

Selecting the Output Inductance

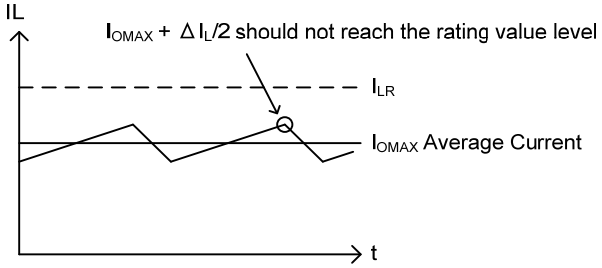


Figure 59. Inductor Current Waveform (Buck Converter)

The output inductance (L) is decided by the rated current (I_{LR}) and maximum input current (I_{OMAX}) of the inductance. Select the inductance so that I_{OMAX} + ΔI_L / 2 will not exceed the rated current value. ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (V_{IN} - V_O) \times \frac{V_O}{V_{IN}} \times \frac{1}{f} \text{ [A]}$$

Where:
f is the switching frequency.

Set with sufficient margin because the inductance value may have a dispersion of ±30%.
If the inductance current exceeds the rated current (I_{LR}), the IC may be damaged.

Selecting the Input and Output Capacitor

The output capacitor (Co) smoothens the ripple voltage at the output. Output ripple voltage V_{PP} can be obtained by the following equation.

$$V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2\,Co} \times \frac{V_O}{V_{IN}} \times \frac{1}{f} \text{ [V]}$$

For the drop voltage V_{DR} during sudden load change, please perform the rough estimate by the following equation.

$$V_{DR} = \frac{\Delta I_L}{Co} \times 10\mu s \text{ [V]}$$

However, 10μs is the rough estimate value of the DC/DC response speed.
Please set the capacitance so that these two values are within the specifications.

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the Input side. For the reason, the low ESR capacitor is recommended as an input capacitor with 10μF or more capacitance and 10mΩ or less ESR. If an out of range capacitor is selected, the excessive ripple voltage is superimposed on the input voltage, thus, it may cause the malfunction of the IC.

However, these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform margin check using the actual product.

Selecting the Output Rectifier Diode

A schottky barrier is recommended as rectifier diode to be used at the output stage of the DC/DC converter. Select carefully in consideration of the maximum inductor current and maximum input voltage.

Maximum Inductor Current	$I_{OMAX} + \frac{\Delta I_L}{2}$	<	Diode Maximum Absolute Current
Maximum Input Voltage	V_{IN}	<	Diode Maximum Absolute Voltage

Provide sufficient design margins for a tolerance of 30% to 40% for each parameter.

Selection of Components Externally Connected – continued

2. Load Switch Gate Drive(GD)

Selecting the Load Switch FET

Select carefully in consideration of the the conditions below.

Maximum Input Current	I_{INMAX}	<	Constant Current of FET
Power Supply Voltage	V_{IN}	<	Constant Voltage of FET
GD Clamp Voltage	$6V$	<	Gate-Source Max Voltage of FET
Power Dissipation	$R_{LDSW} \times I_{INMAX} \times I_{INMAX}$	<	Power Dissipation of FET

Where:
R_{LDSW} is the load swtich on resistance.

3. Boost Converter(AVDD, VGH)

Selecting the Output Inductance

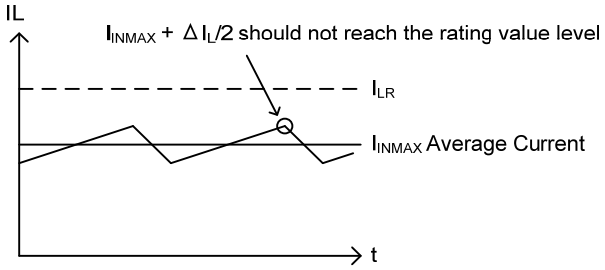


Figure 60. Inductor Current Waveform (Boost Converter)

The output inductance (L) is decided by the rated current (I_{LR}) and maximum input current (I_{INMAX}) of the inductance.
Select the inductance so that $I_{INMAX} + \Delta I_L / 2$ will not exceed the rated current value.
ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} V_{IN} \times \frac{V_O - V_{IN}}{V_O} \times \frac{1}{f} \text{ [A]}$$

Where:
f is the switching frequency.

Set with sufficient margin because the inductance value may have a dispersion of ±30%.
If the inductance current exceeds the rated current (I_{LR}), the IC may be damaged.

Selecting the Input and Output Capacitor

Output ripple voltage V_{PP} can be obtained by the following equation.

$$V_{PP} = I_{LMAX} \times R_{ESR} + \frac{1}{f \times Co} \times \frac{V_{IN}}{V_O} \times \left(I_{LMAX} - \frac{\Delta I_L}{2}\right) \text{ [V]}$$

Select a capacitor that will regulate the output ripple voltage within the specifications.

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the Input side. For the reason, the low ESR capacitor is recommended as an input capacitor with 10μF or more capacitance and 10mΩ or less ESR. If an out of range capacitor is selected, the excessive ripple voltage is superimposed on the input voltage, thus, it may cause the malfunction of the IC.

However, these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform margin check using the actual product.

Selection of Components Externally Connected – continued

Selecting the Output Rectifier Diode

A schottky barrier is recommended as rectifier diode to be used at the output stage of the DC/DC converter. Select carefully in consideration of the maximum inductor current, maximum output voltage.

Maximum Inductor Current	$I_{INMAX} + \frac{\Delta I_L}{2}$	<	Diode Maximum Absolute Current
Maximum Output Voltage	V_{OMAX}	<	Diode Maximum Absolute Voltage

Provide sufficient design margins for a tolerance of 30% to 40% for each parameter.

Setting Phase Compensation

Stable negative feedback condition is achieved as follows:

- When the gain is set to 1 (0 dB), phase delay should not be more than 150°.Consequently, phase margin should not be less than 30°.

Also, since DC/DC converter applications are sampled according to the switching frequency, the whole system GBW should be set to not more than 1/10 of the switching frequency. The target characteristics of the applications can be summarized as follows:

- When the gain is set to 1 (0 dB), the phase delay should not be more than 150°.
And phase margin should not be less than 30°.
- The frequency when the gain is set to 0 dB should not be more than 1/10 of the switching frequency.

The responsiveness is determined by the GBW limitation. Consequently, to increase the circuit response, higher switching frequencies are required.
AVDD is in current mode control. The current mode control is a two-pole single-zero system. The poles are formed by the error amplifier and load while added zero is for phase compensation.
By placing poles appropriately, the circuit can maintain good stability and transient load response.
Bode plot diagram of general DC/DC converter is described below. At point (a), gain starts falling because of a pole formed by the output impedance of the error amplifier and capacitor Ccp. When point (b) is reached, a zero is formed by resistor Rcp and capacitor Ccp to cancel the pole by loading and balance variation of Gain and Phase.
The GBW (i.e., frequency when the gain is 0 dB) is determined by phase compensation capacitor connected to the error amplifier. If GBW is to be reduced, increase the capacitance of the capacitor.

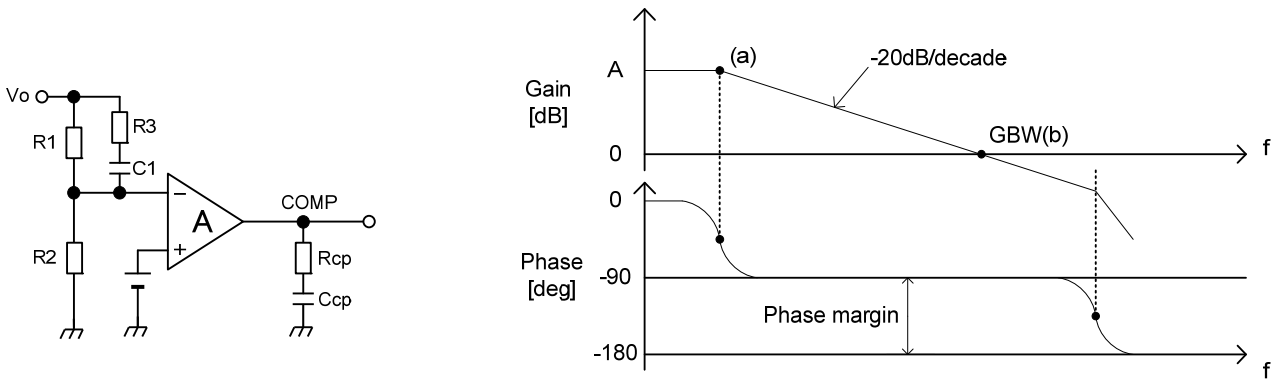


Figure 61. Setting Phase Compensation

Formed Zero (fz1) by Rcp resistor and Ccp capacitor are shown by using the following equation.
And also, Feed-forward capacitor C1 and R1 resistor both create Formed Zero (fz2) and it is used as boosting phase margin in the limited frequency area.

Phase Boost $fz1 = \frac{1}{2\pi CcRcp}$ [Hz]

Phase Boost $fz2 = \frac{1}{2\pi C1R1}$ [Hz]

$fz2$ is formed by the constants in the IC.

Selection of Components Externally Connected – continued

4. Inverting Converter(VGL)

Selecting the Output Inductance

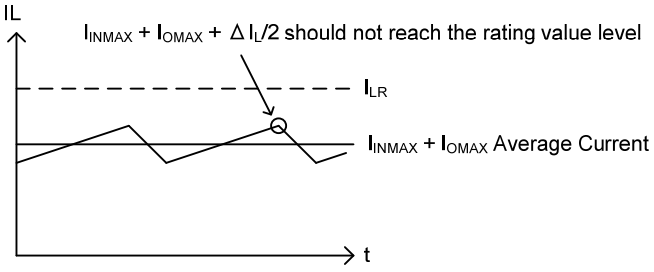


Figure 62. Inductor Current Waveform (Inverting Converter)

The output inductance (L) is decided by the rated current (I_{LR}) and maximum input/output current (I_{INMAX}, I_{OMAX}) of the inductance.
Select the inductance so that I_{IN}+I_{OMAX} + ΔI_L / 2 will not exceed the rated current value. ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times \frac{V_{IN} \times V_O}{V_O - V_{IN}} \times \frac{1}{f} \quad [A]$$

Where:
f is the switching frequency.

Set with sufficient margin because the inductance value may have a dispersion of ±30%.
If the inductance current exceeds the rated current (I_{LR}), the IC may be damaged.

Selecting the Input and Output Capacitor

Output ripple voltage V_{PP} can be obtained by the following equation.

$$V_{PP} = \Delta I_L \times R_{ESR} + \frac{-V_{IN}}{V_O - V_{IN}} \times \frac{1}{f \times Co} \times \left(I_{LMAX} - \frac{\Delta I_L}{2}\right) \text{ [V]}$$

Select a capacitor that will regulate the output ripple voltage within the specifications.

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the Input side. For the reason, the low ESR capacitor is recommended as an input capacitor with 10μF or more capacitance and 10mΩ or less ESR. If an out of range capacitor is selected, the excessive ripple voltage is superimposed on the input voltage, thus, it may cause the malfunction of the IC.

However, these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform margin check using the actual product.

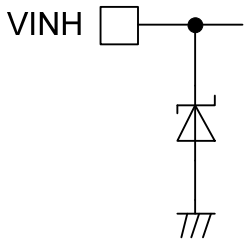
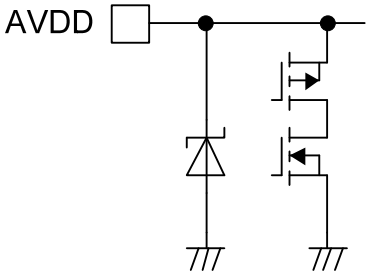
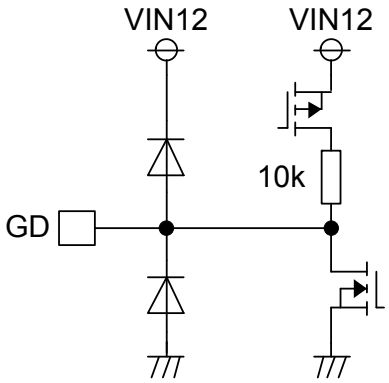
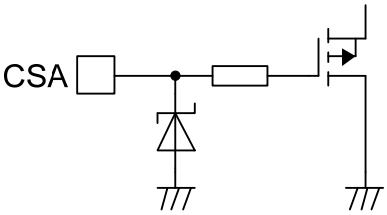
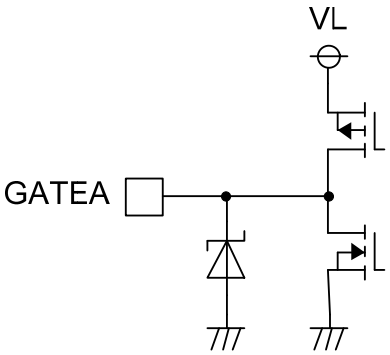
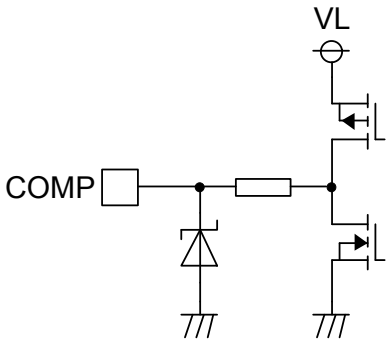
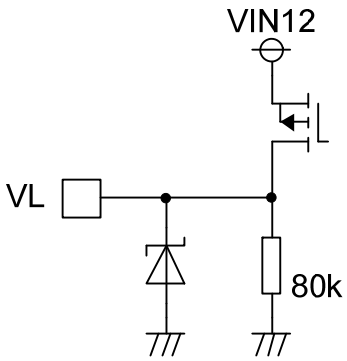
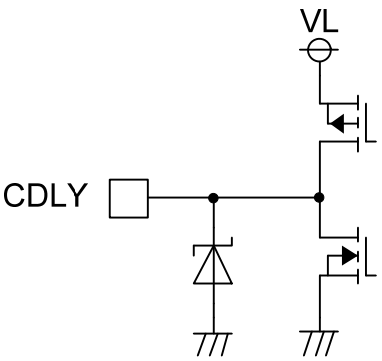
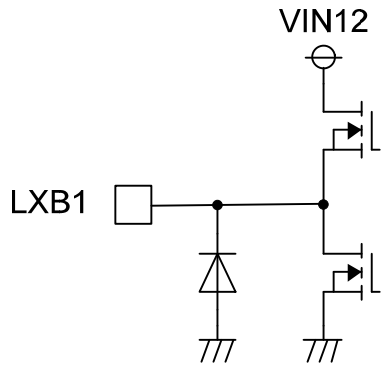
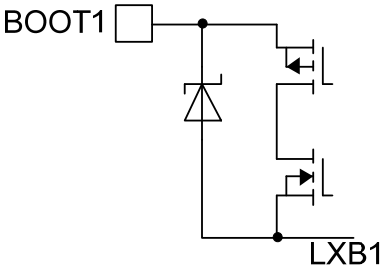
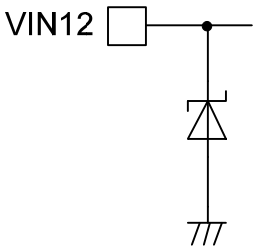
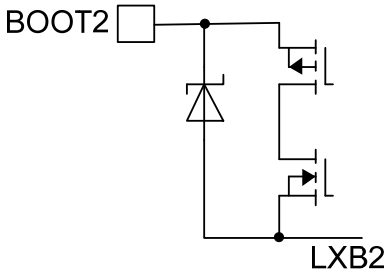
Selecting the Output Rectifier Diode

A schottky barrier is recommended as rectifier diode to be used at the output stage of the DC/DC converter. Select carefully in consideration of the maximum inductor current, maximum input/output voltage.

Maximum Inductor Current	$I_{IN} + I_{IOMAX} + \frac{\Delta I_L}{2}$	<	Diode Maximum Absolute Current
Maximum Input/Output Voltage	$V_{IN} - V_O$	<	Diode Maximum Absolute Voltage

Provide sufficient design margins for a tolerance of 30% to 40% for each parameter.

I/O Equivalence Circuits

1. VINH	3. AVDD	4. GD
		
5. CSA	**7. GATEA**	**8. COMP**
		
9. VL	**10. CDLY**	**11. LXB1**
		
12. BOOT1	**13. VIN12**	**14. BOOT2**
		

I/O Equivalence Circuits – continued

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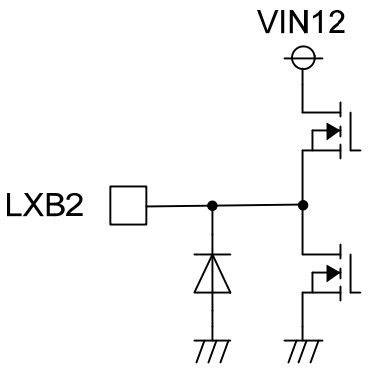	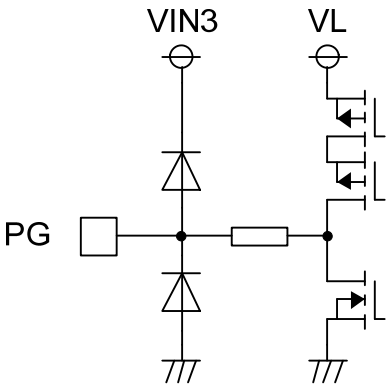	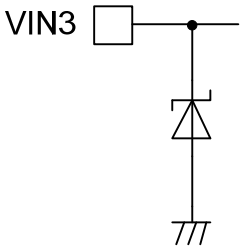
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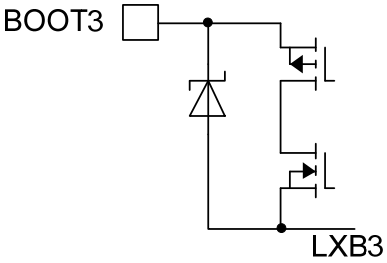
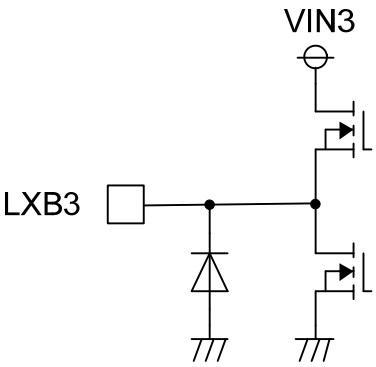
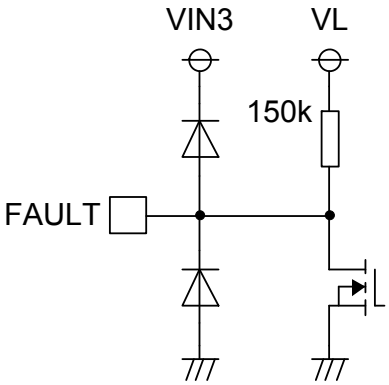
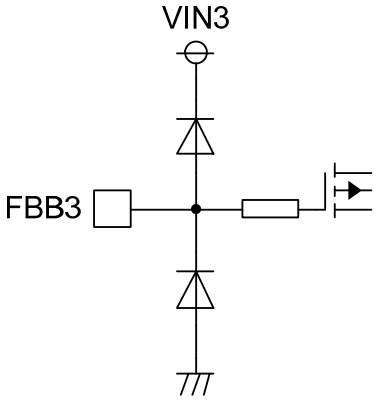
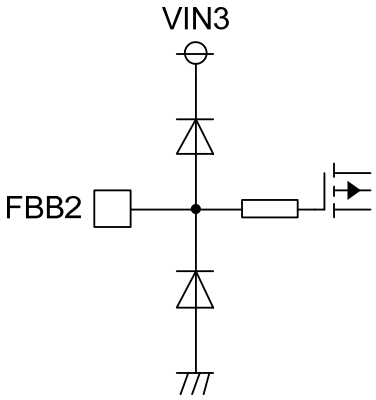
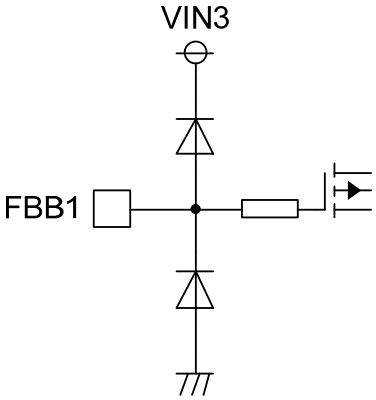
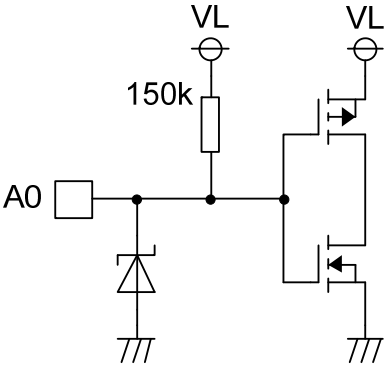
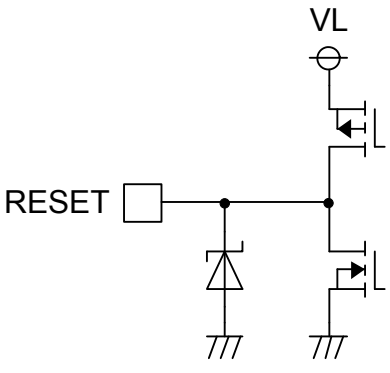
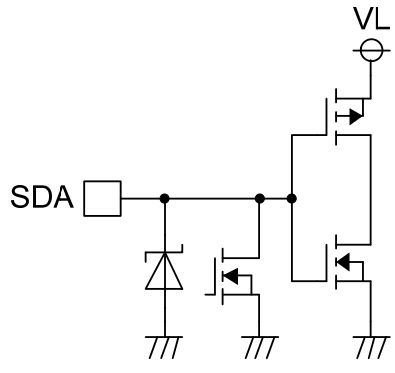
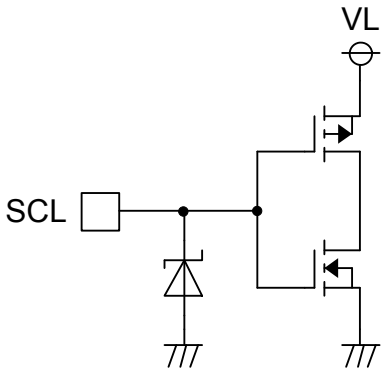
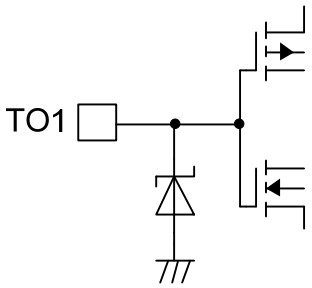
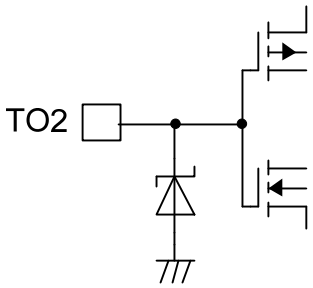
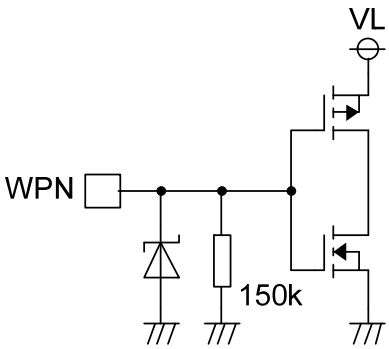
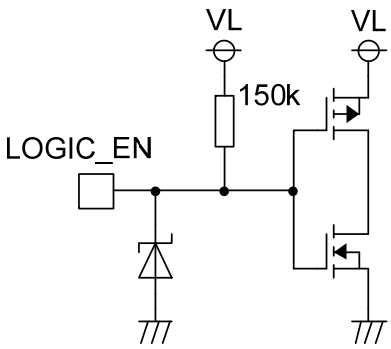
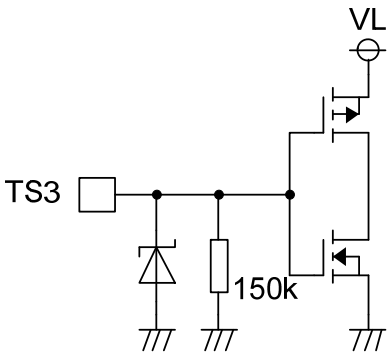
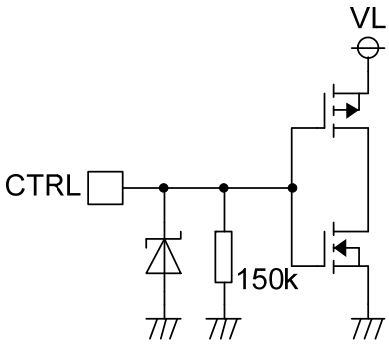
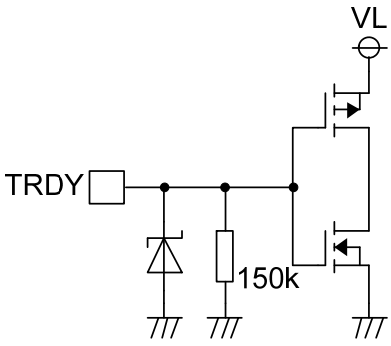
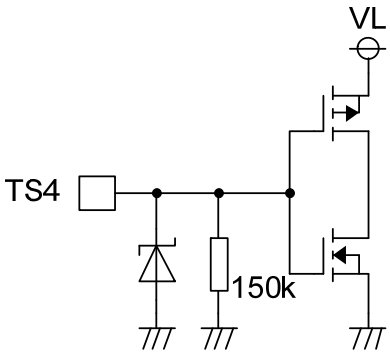
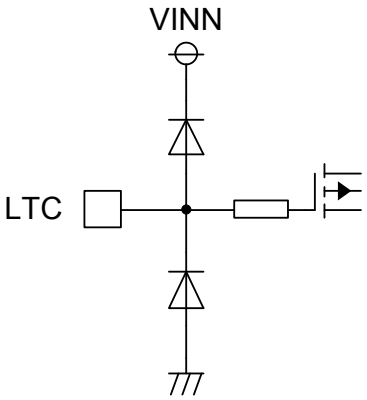
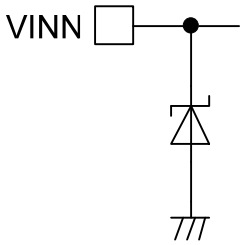
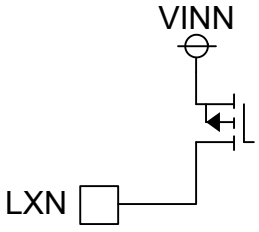
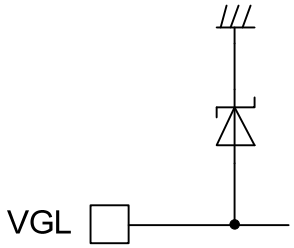
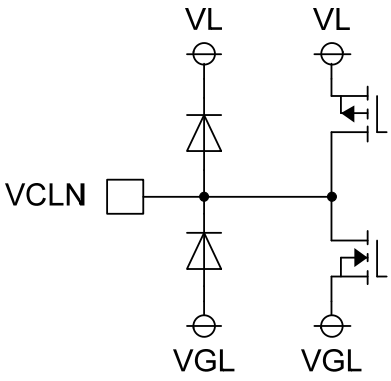
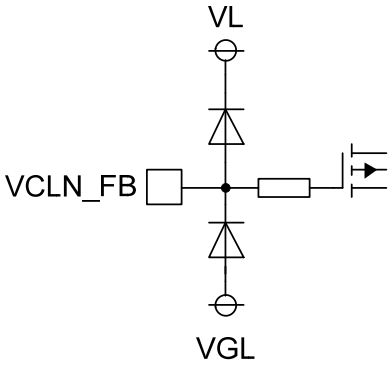
		
21. FBB3	**22. FBB2**	**23. FBB1**
		
24. A0	**25. RESET**	**26. SDA**
		

I/O Equivalence Circuits – continued

27. SCL	28. TO1	29. TO2
		
30. WPN	**31. LOGIC_EN**	**32. TS3**
		
33. CTRL	**34. TRDY**	**35. TS4**
		
36. LTC	**37. VINN**	**38. LXN**
		

I/O Equivalence Circuits – continued

39. VGL	40. VCLN	41. VCLN_FB
		
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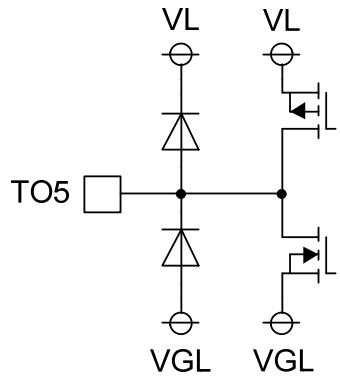
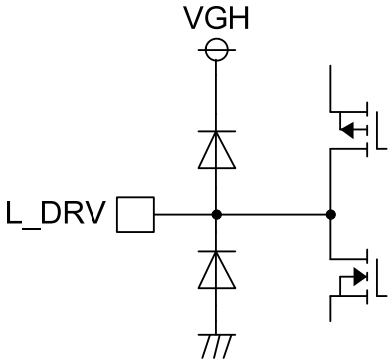
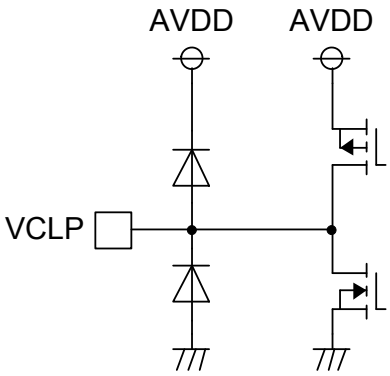
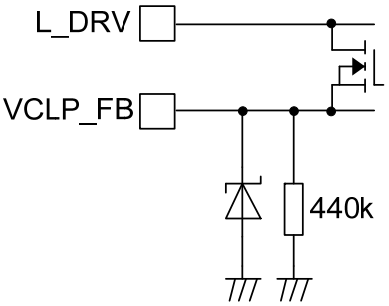
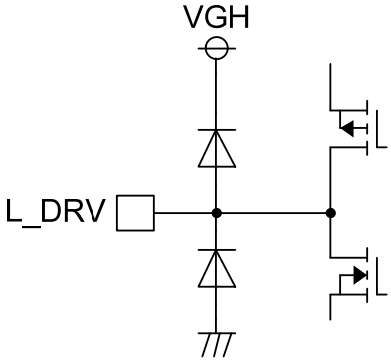
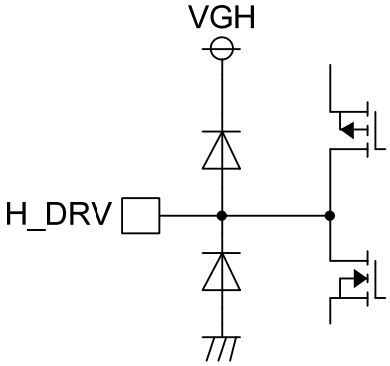
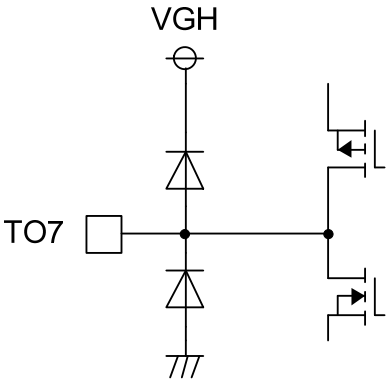
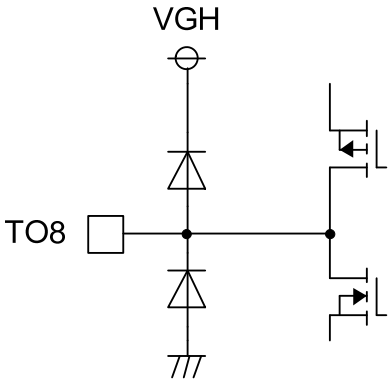
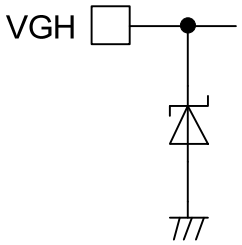
		
45. VCLP_FB	46. L_DRV	47. H_DRV
		
48. TO7	49. TO8	50. VGH
		

I/O Equivalence Circuits – continued

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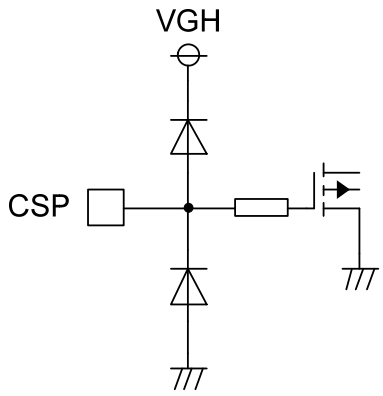	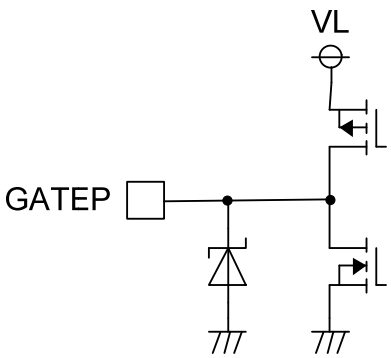	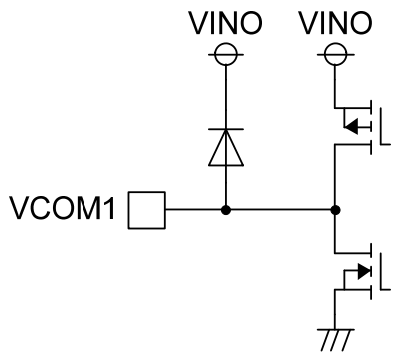
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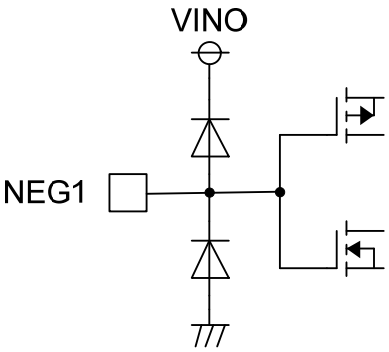
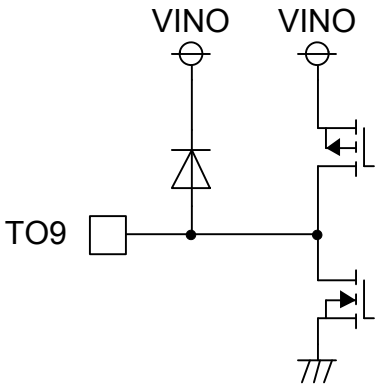
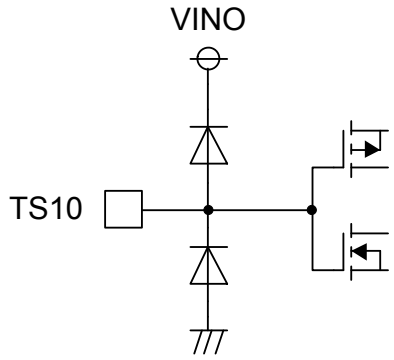
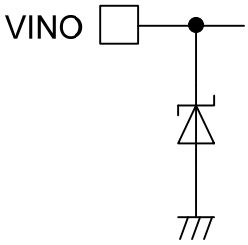
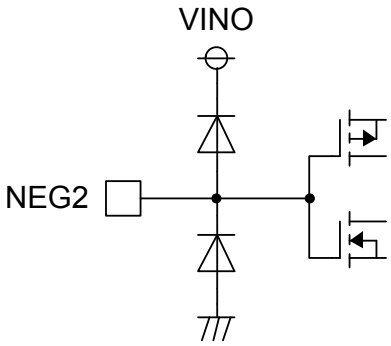
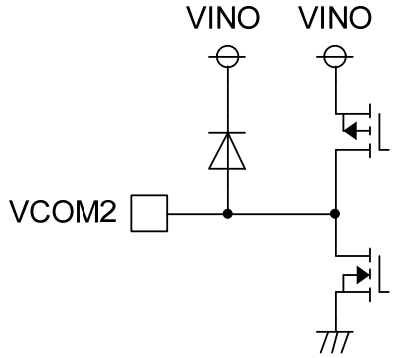
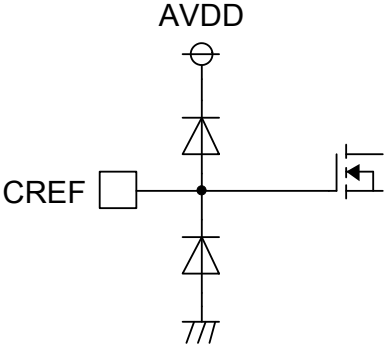
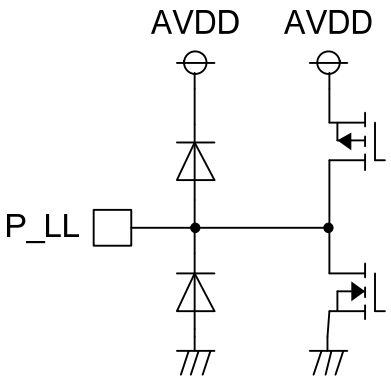
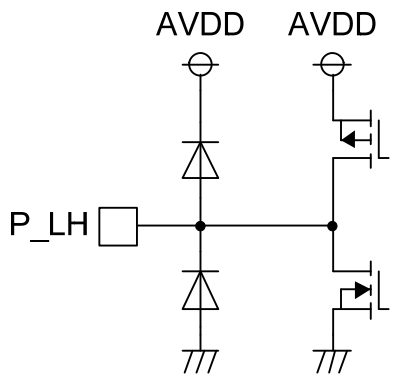
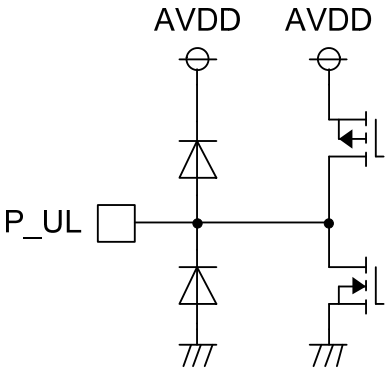
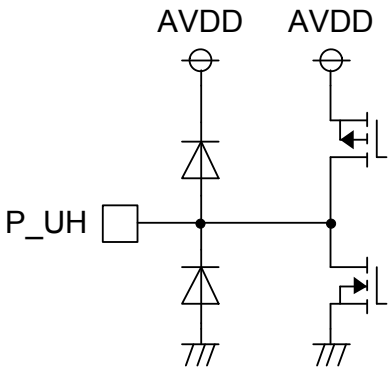
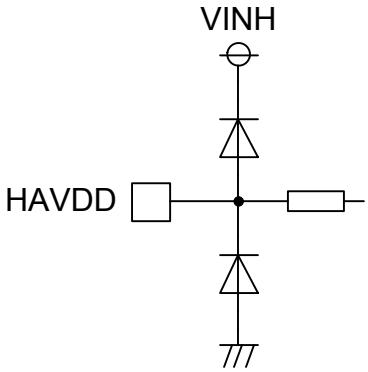
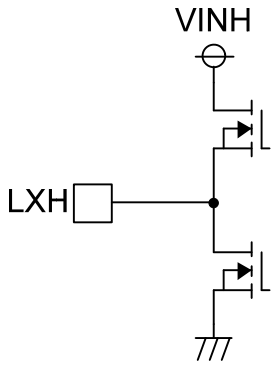
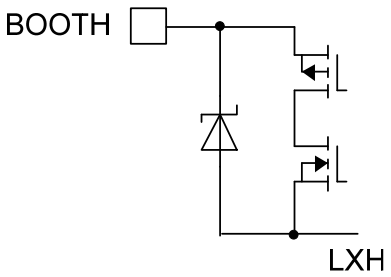
		
58. VINO	**59. NEG2**	**60. VCOM2**
		
61. CREF	**62. P_LL**	**63. P_LH**
		

I/O Equivalence Circuits – continued

64. P_UL	65. P_UH	66. HAVDD
		
67. LXH	**68. BOOTH**	**-**
		-

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

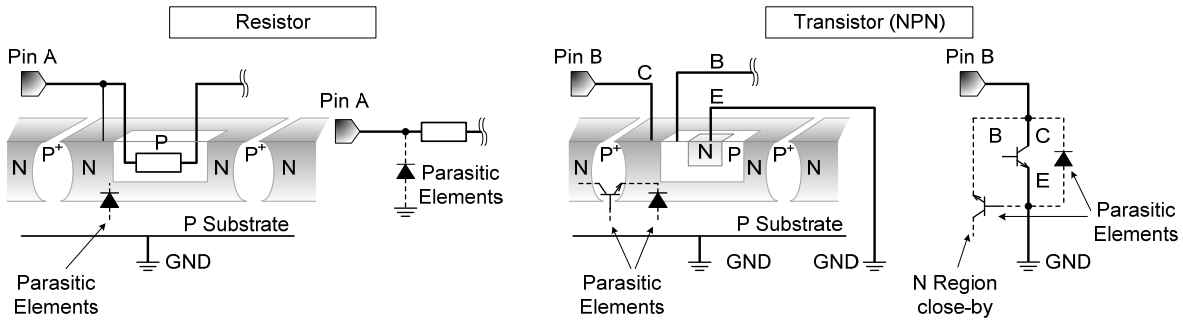


Figure 63. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit(TSD)

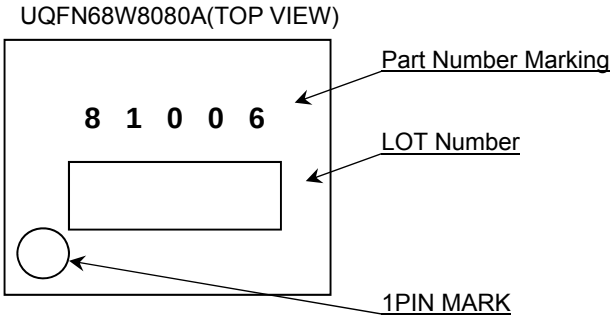
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage

15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

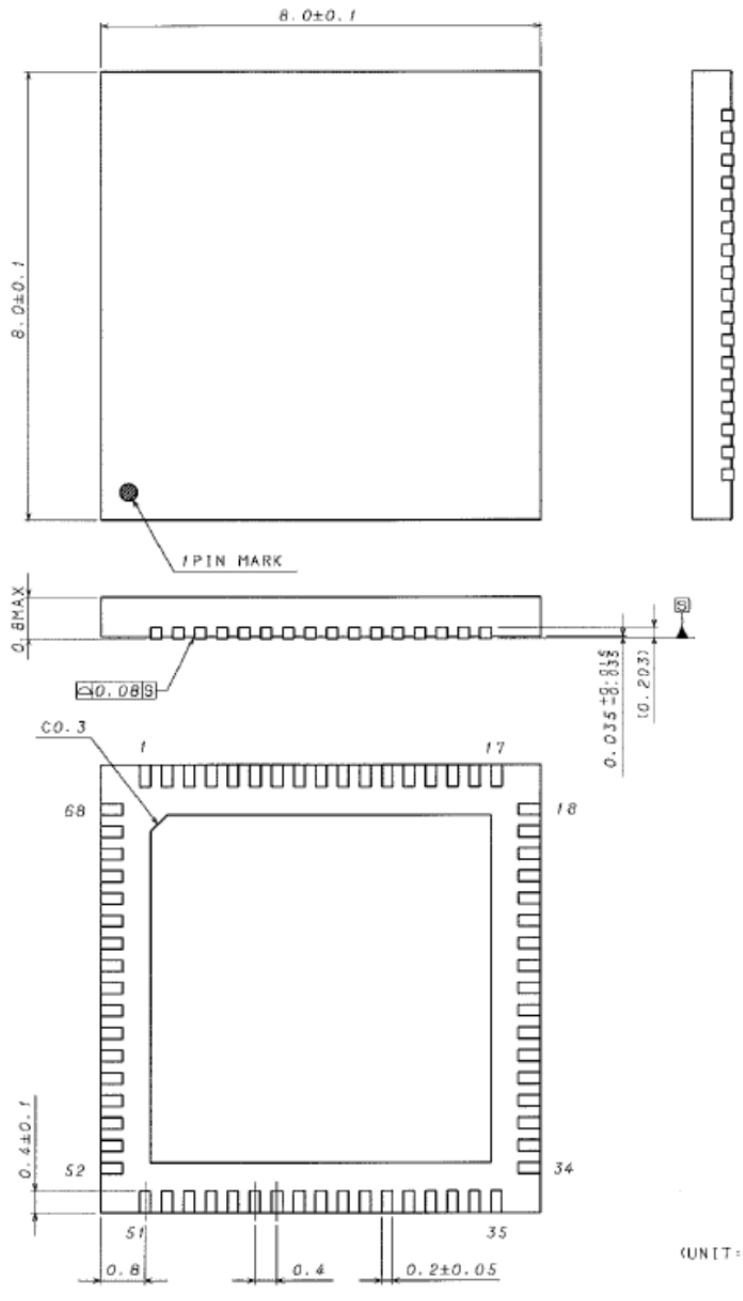
Ordering Information

Marking Diagram



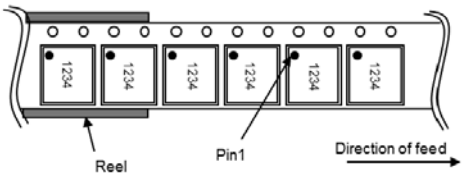
Physical Dimension Tape and Reel Information

Package Name	UQFN68W8080A



< Tape and Reel Information >

Tape	Embossed carrier tape with dry pack
Quantity	1000pcs
Direction of feed	ZE2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
17.Apr.2017	001	New Release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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