

# Audio 1-Chip SOC

## BM94715EKU

### General Description

BM94715EKU is 1-Chip SOC for multimedia audio systems, which supports the USB memory, SD memory card, and CD. This IC has a built-in ARM946ES processor, SDRAM, and various peripherals. It is designated to download programs from external Serial Flash ROM and execute system control, file system management, Audio CODEC, and a wide range of media control.

BM94715EKU supports USB Full-Speed and Bluetooth A2DP.

### Key Features

This IC includes the following blocks:

#### Processor

- ARM946ES Microprocessor Core

#### Memory

- SDRAM
- Initial Program ROM
- Program SRAM
- Data SRAM
- SDRAM Controller

#### System

- Multilayer AHB
- Interrupt Controller
- DMA Controller

#### Serial, Media I/F

- GPIO
- Pin Controller
- USB2.0 Dual Role(Host/Device) Controller
- SD I/F
- Quad SPI I/F
- SPI I/F (Master/Slave)
- I2C I/F (Master/Slave)
- UART I/F
- I2S Input I/F
- I2S Output I/F
- CD Servo Controllers
- CD-ROM Decoder
- General Purpose A/D Converter

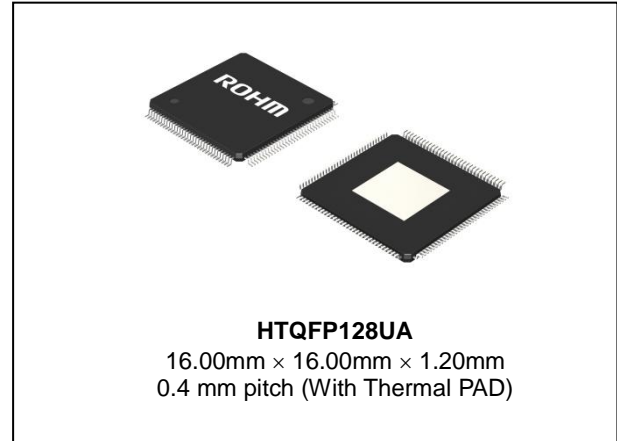
#### Timer

- Timer
- Watchdog Timer
- Real Time Clock

#### Other

- Clock Generator
- Reset Generator
- PLL

### Package



### Application

Component Stereo

### Application Block

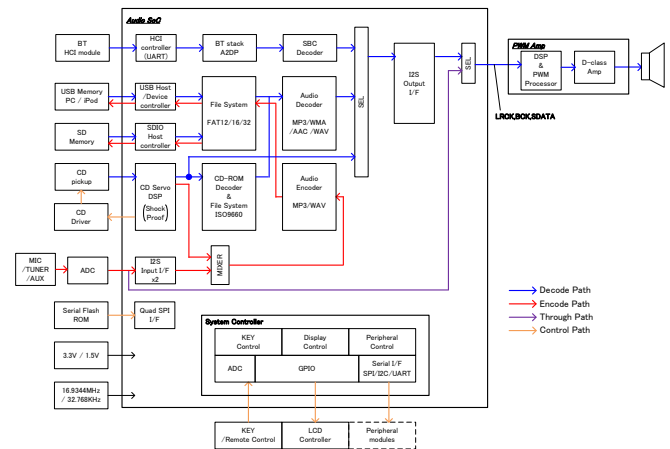


Figure 1. Application Block

### Lineup

| Type       | Package         | Orderable Type |
|------------|-----------------|----------------|
| BM94715EKU | HTQFP128UA Tray | BM94715EKU-Z   |

## Feature

|                |                                  | BM94801KUT                        | BM94803AEKU                                   | BM94715EKU                |
|----------------|----------------------------------|-----------------------------------|---|---------------------------|
| Package        |                                  | TQFP128UM                         | HTQFP128UA                                    | HTQFP128UA                |
| Processor      | ARM946ES                         | 96MHz                             | 108MHz  | 108MHz                    |
|                | ICache/Dcache                    | 4kB/4kB                           | 4kB/4kB                                       | 4kB/4kB                   |
| Memory         | SDRAM                            | 16Mbit                            | 16Mbit  | 16Mbit                    |
|                | Initial Program ROM              | 2kByte                            | 2kByte  | 2kByte                    |
|                | Program SRAM                     | 64kByte                           | 64kByte                                       | 64kByte                   |
|                | Data SRAM                        | 64kByte                           | 64kByte                                       | 64kByte                   |
| System         | Multilayer AHB                   | support                           | support                                       | support                   |
|                | Interrupt Controller             | support                           | support                                       | support                   |
|                | DMA Controller                   | 2ch                               | 1ch   | 1ch                       |
| Peripheral I/F | GPIO                             | support                           | support                                       | support                   |
|                | Pin Controller                   | support                           | support                                       | support                   |
|                | USB2.0 Controller                | HS 1port                          | HS 1port                                      | FS 1port                  |
|                | SD I/F                           | 1ch                               | 1ch   | 1ch                       |
|                | Quad SPI I/F                     | 1ch                               | 1ch   | 1ch                       |
|                | SPI I/F (Master)                 | 1ch                               | 1ch   | 1ch                       |
|                | SPI I/F (Slave)                  | 1ch                               | 1ch   | 1ch                       |
|                | I2C I/F (Master/Slave)           | 2ch                               | 2ch   | 2ch                       |
|                | UART I/F                         | 2ch                               | 2ch   | 2ch                       |
|                | I2S Input I/F                    | 2ch 2series                       | 2ch 2series                                   | 2ch 2series               |
|                | I2S Output I/F                   | I2S:stereo + mono<br>192kHz/24bit | I2S:stereo<br>192kHz/24bit<br>DSD : 5.6448MHz | I2S:stereo<br>48kHz/16bit |
|                | CD Servo Controllers             | support                           | support                                       | support                   |
|                | CD-ROM Decoder                   | support                           | support                                       | support                   |
|                | RemoteControll                   | support                           | support                                       | support                   |
|                | General purpose<br>A/D Converter | 1.5V x 8ch                        | 3.3V x 8ch                                    | 3.3V x 8ch                |
| Timer          | Timer                            | 5ch                               | 5ch   | 5ch                       |
|                | Watchdog Timer                   | 1ch                               | 1ch   | 1ch                       |
|                | Real Time Clock                  | 1ch                               | 1ch   | 1ch                       |
| Entertainment  | DSP                              | -                                 | -   | -                         |
|                | PWM out                          | -                                 | -   | -                         |
| Accelerator    | FLAC/ALAC                        | -                                 | -   | -                         |
| Clock          | Clock Generator                  | support                           | support                                       | support                   |
|                | Reset Generator                  | support                           | support                                       | support                   |

Note: Specification of BM94801KUT and BM94803AEKU are correct for the Datasheet of BM94801KUT and BM94803AEKU respectively.

**Feature – continued**

## ARM946ES Microprocessor Core

- ◇ 32Bit RISC Processor
- ◇ Operating Frequency: 108MHz
- ◇ 8kByte Cache
  - Data Cache 4kByte
  - Instruction Cache 4kByte

## SDRAM

- ◇ 16Mbit
- ◇ SDRAM with built-in MSM56V16160N from LAPIS Semiconductor
- ◇ 2Bank x 524,288-word x 16Bit

## Initial Program ROM

- ◇ ITCM ROM Size: 2kByte (512Word x 32Bit)
- ◇ boot program
- ◇ No-wait access

## REMAP

- ◇ Remapping can be implemented by writing to internal registers.

## SHADOW SRAM

- ◇ RAM Size: 512Byte (128-Word x 32-Bit)
- ◇ No-wait access

## Program SRAM

- ◇ ITCM RAM Size: 64kByte (16,384-Word x 32-Bit)
- ◇ No-wait access

## Data SRAM

- ◇ DTCM RAM Size: 64kByte (16,384-Word x 32-Bit)
- ◇ No-wait access

## SDRAM Controller

- ◇ Supports SDRAM
- ◇ Supports 11Bit row address, 8-bit column address, and 1-bit bank address to SDRAM

## AMBA

- ◇ 32Bit Data Bus
- ◇ Arbitrates ARM and DMA access with an arbiter

## Interrupt Controller

- ◇ 23 IRQ Interrupt Lines
- ◇ 1 FIQ Interrupt Line
- ◇ Allows programmable setting of interrupt priority levels
- ◇ Allows setting of 16 vector addresses

## DMA Controller

- ◇ Supports 1 Channel
- ◇ Channel FIFO Depth Up to 16 Bytes
- ◇ Allows programmable setting of transfer data width in the range of 1Byte to 4Bytes
- ◇ Allows programmable setting of channel priority levels
- ◇ Maximum Block Length Up to 4,095 Words
- ◇ Includes 12 handshake interfaces available for assignment to channels with software
- ◇ Supports multiblock transfers
- ◇ Connects the master board to system bus

## GPIO

- ◇ GPIO0(32 pins), GPIO1(32 pins), GPIO2(13pins)
- ◇ 4 of 17 pins assigned GPIO2 are not available because of analog pin. (See P9 Pin Description)
- ◇ Supports a maximum of 77 I/O pins (including 16 GPIO pins for exclusive use)
- ◇ Supports the interrupt function
- ◇ Supports external level-sensitive interrupt

**Feature – continued**

## Pin Controller

- ✧ Controls connection settings between pins and blocks

## USB2.0 Dual Role (Host/Device) controller

- ✧ USB 2.0 conformance
- ✧ Bit rate: Full-Speed(12Mbps)
- ✧ Configurable for up to five transmit endpoint FIFOs and four receive endpoint FIFOs (including endpoint 0)
- ✧ Each endpoint FIFO supports bulk transfer, interrupt transfer, and isochronous transfer.
- ✧ 4096-Byte RAM for Endpoint FIFO

## SD I/F

- ✧ Supports SDHC, and SD cards
- ✧ Provide access to SD card in SD Bus mode
- ✧ Allows control from the AMBA-AHB Bus
- ✧ Includes 512 Byte data transmit/receive FIFOs

## Quad SPI I/F

- ✧ Supports quad serial flash ROM
- ✧ Supports serial flash ROM address up to 24 bits
- ✧ Allows the setting of control registers from the AMBA-AHB bus
- ✧ Allows direct access from the memory map of the AMBA-AHB bus to serial flash ROM
- ✧ Includes 32 byte transmit/receive FIFOs

## SSI Master

- ✧ FIFO Depth Up to 16 Words and FIFO Data Width Up to 16Bits
- ✧ Selectable Data Size from 4 Bits to 16 Bits
- ✧ Serial protocol supports SPI from Motorola
- ✧ Includes DMA handshake interface

## SSI Slave

- ✧ FIFO Depth Up to 16 Words and FIFO Data Width Up to 16 Bits
- ✧ Selectable Data Size from 4 Bits to 16 Bits
- ✧ Serial protocol supports SPI from Motorola
- ✧ Includes DMA handshake interface

## I2C I/F (Master/Slave)

- ✧ 2 Ch I2C Serial Interface
- ✧ Supports two speed modes
- ✧ Standard mode (100Kb/s)
- ✧ Fast mode (400Kb/s)
- ✧ Supports I2C Master and Slave operation
- ✧ Allows 7 and 10 bit address generation
- ✧ Has built-in 32 stage transmit and receive FIFOs
- ✧ Includes DMA handshake interface

## UART I/F

- ✧ IS16550-Based
- ✧ Allows various baud rate settings with software (up to 6Mbps)
- ✧ No Support for IrDA
- ✧ FIFO Depth Up to 32 Words and FIFO Data Width Up to 8 Bits
- ✧ Incorporates a function to invert output
- ✧ Includes DMA handshake interface

## Feature – continued

## I2S Input I/F

- ◇ Two Lines of 2-Ch Digital Audio Input
- ◇ I2S, EIAJ format
- ◇ 16-Bit Data
- ◇ Selectable Bit Clock from 32fs, 48fs, and 64fs
- ◇ Selectable Input Sample Rate from 32kHz, 44.1kHz, and 48kHz
- ◇ One Line of Internal Input from the CD Servo Controller
- ◇ Maximum Input Rate Up to 4x
- ◇ Supports detection of CD-DA link
- ◇ Supports detection of CD-ROM sync
- ◇ Supports CD-ROM data descrambling
- ◇ Acquires Sub-Q data
- ◇ Acquires CD-Text data
- ◇ Built-in DMA 2ch
- ◇ Supports I2S Input at CD Play

## I2S Output I/F

- ◇ 2-Ch Digital Audio Output x 1 ( 2ch from Decoder)
- ◇ I2S, EIAJ format
- ◇ Selectable PCM Output Sample Rate from 32k, 44.1k, 48kHz
- ◇ Selectable PCM Data Width from 16 bits
- ◇ 64 fs PCM Bit Clock
- ◇ Supports pitch control (x0.5 - x2.0, 25step)

## CD servo controller

- ◇ Supports rotation speed of CD up to 4x
- ◇ Built-in Preservo-Amplifier with Power Save Mode, which supports Playback of CD-RW
- ◇ Allows independent offset adjustment of AC, BD, E, and F amplifiers
- ◇ Built-in Auto-Tracking and Focus Adjustment Function
- ◇ Built-in PLL and CLV with a Wide Lock Range
- ◇ Built-in Asymmetry Correction Function

## CD-ROM Decoder

- ◇ Supports Mode1, Mode2 form1, Mode2 form2
- ◇ Supports ECC, EDC
- ◇ Built-in DMA

## General Purpose A/D Converter

- ◇ 10-Bit SAR ADC, 8 Ch ADC
- ◇ Analog Input Voltage range: VDD\_ADC x10% to VDD\_ADC x 90%
- ◇ Maximum A/D Conversion frequency Ch=88.2ksps

## Timer

- ◇ Supports five independent programmable timer functions
- ◇ Each timer supports time width up to 32 bits
- ◇ Each timer supports independent interrupt signal

## Watchdog Timer

- ◇ Composed of a counter having a set cycle to monitor the occurrence of timeout event
- ◇ Counter Width Up to 32 Bits
- ◇ The counter counts down from the set value and sets timeout occurrence when it reaches zero

## Realtime clock

- ◇ 32 Bit Programmable Timer
- ◇ Supports interrupt signals
- ◇ External 32.768 kHz Crystal Oscillator

**Feature – continued**

## Remote Controller Receiver (RCR)

- ◇ Converts infrared remote control signal to code
- ◇ Compatible with the signal format of the Association for Electric Home Appliances
- ◇ Supports Sony format
- ◇ Enables to setup permissible value of input signal cycle to adjust the Duty deviation of input signal

## Clock Generator

- ◇ Supplies clocks to individual internal blocks
- ◇ Allows on/off control of clocks to individual blocks
- ◇ Generates master audio clocks
- ◇ At the normal operation, supports three modes (High-Speed mode, Middle Speed mode, Low-Speed mode)
- ◇ Supports Standby Mode

## Reset Generator

- ◇ Generates a pulse to be supplied to individual blocks

## PLL

- ◇ Generates 216MHz / 240MHz clock used to generate system clocks
- ◇ Generates 135.4752 MHz and 147.456 MHz clocks used to generate audio clocks

## Power Supply Voltage

- ◇ I/O Power Supply Voltage : 3.3V(3.0V to 3.6V)
- ◇ Analog Power Supply Voltage: 3.3V(3.0V to 3.6V)  
(Used for SDRAM, CD servo, USB, and ADC)
- ◇ Digital Core Power Supply Voltage : 1.5V(1.45V to 1.65V)  
(Used for Digital Core)

Pin Assignment

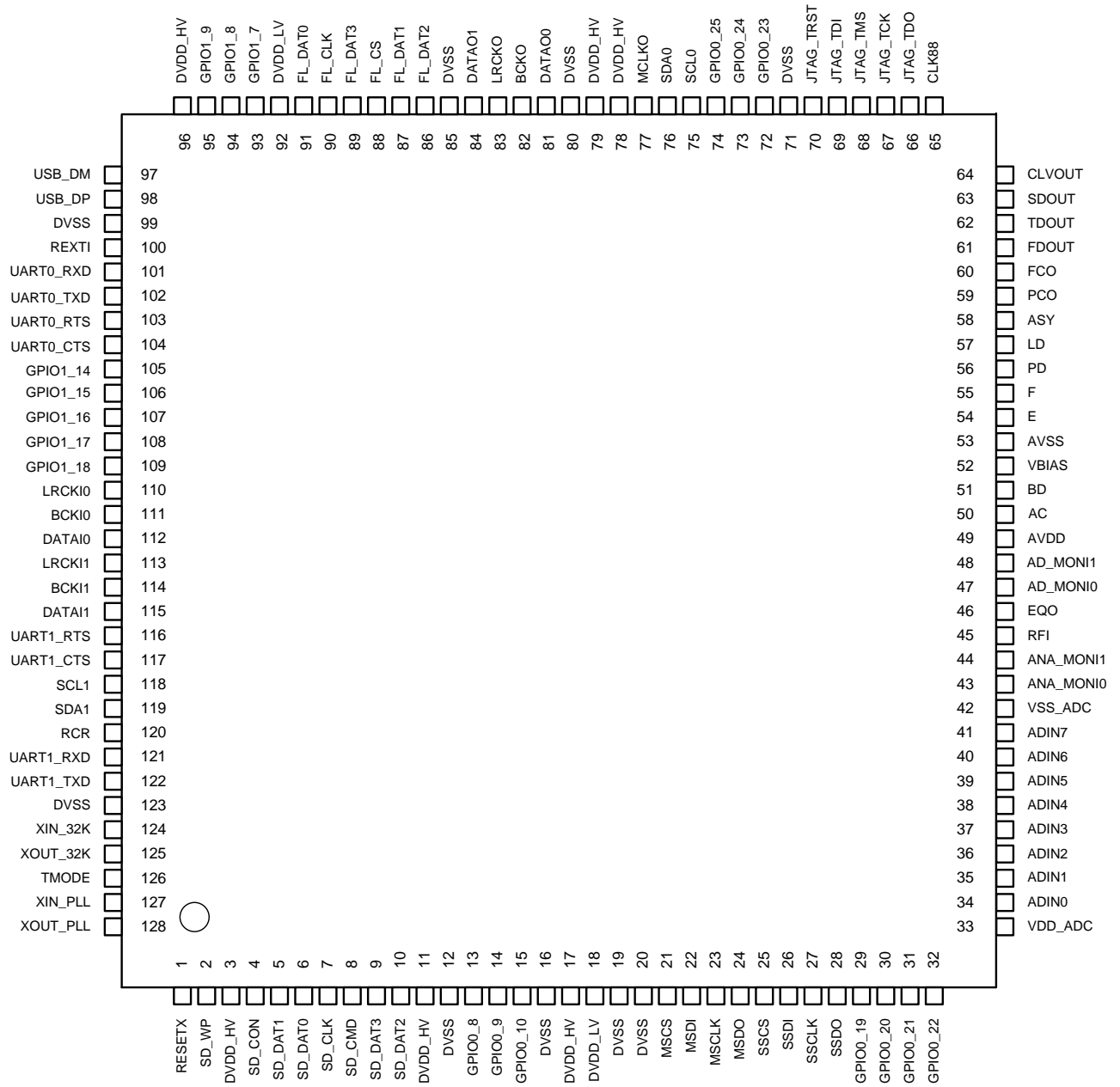


Figure 2. Pin Assignment

## Pin Description

| No | Block | Pin Name  | GPIO      | I/O | Function   |
|----|-------|-----------|-----------|-----|--|
| 1  | RESET | RESETX    |           | I   | H: Release RESET, L: RESET   |
| 2  | SD    | SD_WP     | GPIO0[0]  | I/O | SD Card I/F WP Detect  |
| 3  | POWER | DVDD_HV   |           | -   | 3.3V Power Supply  |
| 4  | SD    | SD_CON    | GPIO0[1]  | I/O | SD Card I/F Connection Detect  |
| 5  | SD    | SD_DAT1   | GPIO0[2]  | I/O | SD Card I/F Data I/O (1)   |
| 6  | SD    | SD_DAT0   | GPIO0[3]  | I/O | SD Card I/F Data I/O (0)   |
| 7  | SD    | SD_CLK    | GPIO0[4]  | I/O | SD Card I/F Clock Output   |
| 8  | SD    | SD_CMD    | GPIO0[5]  | I/O | SD Card I/F Command Output   |
| 9  | SD    | SD_DAT3   | GPIO0[6]  | I/O | SD Card I/F Data I/O (3)   |
| 10 | SD    | SD_DAT2   | GPIO0[7]  | I/O | SD Card I/F Data I/O (2)   |
| 11 | POWER | DVDD_HV   |           | -   | 3.3V Power Supply  |
| 12 | POWER | DVSS      |           | -   | GND  |
| 13 | GPIO  | GPIO0_8   | GPIO0[8]  | I/O | GPIO for exclusive use   |
| 14 | GPIO  | GPIO0_9   | GPIO0[9]  | I/O | GPIO pin. When CD is used, this pin is TRAY OPEN/CLOSE detect pin of CD mechanical tray. |
| 15 | GPIO  | GPIO0_10  | GPIO0[10] | I/O | GPIO for exclusive use   |
| 16 | POWER | DVSS      |           | -   | GND  |
| 17 | POWER | DVDD_HV   |           | -   | 3.3V Power Supply  |
| 18 | POWER | DVDD_LV   |           | -   | 1.5V Power Supply  |
| 19 | POWER | DVSS      |           | -   | GND  |
| 20 | POWER | DVSS      |           | -   | GND  |
| 21 | MSIO  | MSCS      | GPIO0[11] | I/O | SIO Master Chip Select Output  |
| 22 | MSIO  | MSDI      | GPIO0[12] | I/O | SIO Master Data Input  |
| 23 | MSIO  | MSCLK     | GPIO0[13] | I/O | SIO Master Clock Output  |
| 24 | MSIO  | MSDO      | GPIO0[14] | I/O | SIO Master Data Output   |
| 25 | SSIO  | SSCS      | GPIO0[15] | I/O | SIO Slave Chip Select Input  |
| 26 | SSIO  | SSDI      | GPIO0[16] | I/O | SIO Slave Data Input   |
| 27 | SSIO  | SSCLK     | GPIO0[17] | I/O | SIO Slave Clock Input  |
| 28 | SSIO  | SSDO      | GPIO0[18] | I/O | SIO Slave Data Output  |
| 29 | GPIO  | GPIO0_19  | GPIO0[19] | I/O | GPIO for exclusive use   |
| 30 | GPIO  | GPIO0_20  | GPIO0[20] | I/O | GPIO for exclusive use   |
| 31 | GPIO  | GPIO0_21  | GPIO0[21] | I/O | GPIO pin. When CD is used, this pin is INNER_SW detect pin.                              |
| 32 | GPIO  | GPIO0_22  | GPIO0[22] | I/O | GPIO for exclusive use   |
| 33 | POWER | VDD_ADC   |           | -   | 3.3V ADC Power Supply  |
| 34 | ADC   | ADIN0     | GPIO2[0]  | I   | AD input CH0 or GPIO   |
| 35 | ADC   | ADIN1     | GPIO2[1]  | I   | AD input CH1 or GPIO   |
| 36 | ADC   | ADIN2     | GPIO2[2]  | I   | AD input CH2 or GPIO   |
| 37 | ADC   | ADIN3     | GPIO2[3]  | I   | AD input CH3 or GPIO   |
| 38 | ADC   | ADIN4     | GPIO2[4]  | I   | AD input CH4 or GPIO   |
| 39 | ADC   | ADIN5     | GPIO2[5]  | I   | AD input CH5 or GPIO   |
| 40 | ADC   | ADIN6     | GPIO2[6]  | I   | AD input CH6 or GPIO   |
| 41 | ADC   | ADIN7     | GPIO2[7]  | I   | AD input CH7 or GPIO   |
| 42 | POWER | VSS_ADC   |           | -   | ADC GND  |
| 43 | CDDSP | ANA_MONI0 | GPIO2[8]  | I/O | Input & Analog Monitor Output or GPIO  |
| 44 | CDDSP | ANA_MONI1 | GPIO2[9]  | I/O | Input & Analog Monitor Output or GPIO  |
| 45 | CDDSP | RFI       |           | I   | RF Output Capacitance Coupling Re-Input  |
| 46 | CDDSP | EQO       |           | O   | Output RF Equalizer  |
| 47 | CDDSP | AD_MONI0  | GPIO2[10] | I/O | Input & Monitor Signal Output or GPIO  |
| 48 | CDDSP | AD_MONI1  | GPIO2[11] | I/O | Input & Monitor Signal Output or GPIO  |
| 49 | POWER | AVDD      |           | -   | 3.3V CD RF Power Supply  |
| 50 | CDDSP | AC        |           | I   | A + C Voltage Input  |
| 51 | CDDSP | BD        |           | I   | B + D Voltage Input  |
| 52 | CDDSP | VBIAS     |           | O   | VBIAS Output   |
| 53 | POWER | AVSS      |           | -   | CD RF GND  |
| 54 | CDDSP | E         |           | I   | E Voltage Input  |
| 55 | CDDSP | F         |           | I   | F Voltage Input  |
| 56 | CDDSP | PD        |           | I   | APC Photo Detector Input   |
| 57 | CDDSP | LD        |           | O   | APC Laser Drive Output   |



Pin Description – continued

| No  | Block   | Pin Name  | GPIO      | I/O | Function   |
|-----|---------|-----------|-----------|-----|--|
| 58  | CDDSP   | ASY       |           | I   | Asymmetric Correction  |
| 59  | CDDSP   | PCO       |           | O   | PLL PCO Output   |
| 60  | CDDSP   | FCO       |           | O   | PLL FCO-DAC Output   |
| 61  | CDDSP   | FDOOUT    | GPIO2[12] | I/O | Focus Drive Output<br>Use this pin as analog pin.  |
| 62  | CDDSP   | TDOUT     | GPIO2[13] | I/O | Tracking Drive Output<br>Use this pin as analog pin.   |
| 63  | CDDSP   | SDOUT     | GPIO2[14] | I/O | Sled Drive Output<br>Use this pin as analog pin.   |
| 64  | CDDSP   | CLVOUT    | GPIO2[15] | I/O | CLV Drive Output<br>Use this pin as analog pin.  |
| 65  | CDDSP   | CLK88     | GPIO2[16] | I/O | Clock Output for Driver IC or GPIO   |
| 66  | JTAG    | JTAG_TDO  |           | O   | JTAG TDO   |
| 67  | JTAG    | JTAG_TCK  |           | I   | JTAG TCK   |
| 68  | JTAG    | JTAG_TMS  |           | I   | JTAG TMS   |
| 69  | JTAG    | JTAG_TDI  |           | I   | JTAG TDI   |
| 70  | JTAG    | JTAG_TRST |           | I/O | JTAG TRST  |
| 71  | POWER   | DVSS      |           | -   | GND  |
| 72  | GPIO    | GPIO0_23  | GPIO0[23] | I/O | GPIO for exclusive use   |
| 73  | GPIO    | GPIO0_24  | GPIO0[24] | I/O | GPIO for exclusive use   |
| 74  | GPIO    | GPIO0_25  | GPIO0[25] | I/O | GPIO for exclusive use   |
| 75  | I2C     | SCL0      | GPIO0[26] | I/O | I2C Clock I/O (0), Open drain output pin   |
| 76  | I2C     | SDA0      | GPIO0[27] | I/O | I2C Data I/O (0), Open drain output pin  |
| 77  | I2S OUT | MCLKO     | GPIO0[28] | I/O | Digital Audio Master Clock Output  |
| 78  | POWER   | DVDD_HV   |           | -   | 3.3V Power Supply  |
| 79  | POWER   | DVDD_HV   |           | -   | 3.3V Power Supply  |
| 80  | POWER   | DVSS      |           | -   | GND  |
| 81  | I2S OUT | DATA00    | GPIO0[29] | I/O | Digital Audio Data Output (0)  |
| 82  | I2S OUT | BCKO      | GPIO0[30] | I/O | Digital Audio Bit Clock Output   |
| 83  | I2S OUT | LRCKO     | GPIO0[31] | I/O | Digital Audio Channel Clock Output   |
| 84  | I2S OUT | DATA01    | GPIO1[0]  | I/O | Digital Audio Data Output (1)  |
| 85  | POWER   | DVSS      |           | -   | GND  |
| 86  | FLASH   | FL_DAT2   | GPIO1[1]  | I/O | Serial Flash ROM I/F Data I/O (2)  |
| 87  | FLASH   | FL_DAT1   | GPIO1[2]  | I/O | Serial Flash ROM I/F Data I/O (1)  |
| 88  | FLASH   | FL_CS     | GPIO1[3]  | I/O | Serial Flash ROM I/F Command Output  |
| 89  | FLASH   | FL_DAT3   | GPIO1[4]  | I/O | Serial Flash ROM I/F Data I/O (3)  |
| 90  | FLASH   | FL_CLK    | GPIO1[5]  | I/O | Serial Flash ROM I/F Clock Output  |
| 91  | FLASH   | FL_DAT0   | GPIO1[6]  | I/O | Serial Flash ROM I/F Data I/O (0)  |
| 92  | POWER   | DVDD_LV   |           | -   | 1.5V Power Supply  |
| 93  | GPIO    | GPIO1_7   | GPIO1[7]  | I/O | GPIO for exclusive use   |
| 94  | GPIO    | GPIO1_8   | GPIO1[8]  | I/O | GPIO for exclusive use   |
| 95  | GPIO    | GPIO1_9   | GPIO1[9]  | I/O | GPIO for exclusive use   |
| 96  | POWER   | DVDD_HV   |           | -   | 3.3V Power Supply  |
| 97  | USB     | USB_DM    |           | I/O | USB D-   |
| 98  | USB     | USB_DP    |           | I/O | USB D+   |
| 99  | POWER   | DVSS      |           | -   | GND  |
| 100 | USB     | REXTI     |           | I   | USB Reference Voltage Output. Connect a pull down resistance to DVSS pin. The pull down resistance must be 12.3 kΩ±1%.<br>About on PCB, do not wire as long as possible and not wire side by side long distance with noise line, especially note the next pin UART0_RXD(pin101). |

## Pin Description - continued

| No  | Block  | Pin Name  | GPIO      | I/O | Function                                     |
|-----|--------|-----------|-----------|-----|--|
| 101 | UART   | UART0_RXD | GPIO1[10] | I/O | UART0 Receive Data                           |
| 102 | UART   | UART0_TXD | GPIO1[11] | I/O | UART0 Transmit Data                          |
| 103 | UART   | UART0_RTS | GPIO1[12] | I/O | UART0 Transfer Request                       |
| 104 | UART   | UART0_CTS | GPIO1[13] | I/O | UART0 Clear Request                          |
| 105 | GPIO   | GPIO1_14  | GPIO1[14] | I/O | GPIO for exclusive use                       |
| 106 | GPIO   | GPIO1_15  | GPIO1[15] | I/O | GPIO for exclusive use                       |
| 107 | GPIO   | GPIO1_16  | GPIO1[16] | I/O | GPIO for exclusive use                       |
| 108 | GPIO   | GPIO1_17  | GPIO1[17] | I/O | GPIO for exclusive use                       |
| 109 | GPIO   | GPIO1_18  | GPIO1[18] | I/O | GPIO for exclusive use                       |
| 110 | I2S IN | LRCKI0    | GPIO1[19] | I/O | Digital Audio Channel Clock Input (0)        |
| 111 | I2S IN | BCKI0     | GPIO1[20] | I/O | Digital Audio Bit Clock Input (0)            |
| 112 | I2S IN | DATAI0    | GPIO1[21] | I/O | Digital Audio Data Input (0)                 |
| 113 | I2S IN | LRCKI1    | GPIO1[22] | I/O | Digital Audio Channel Clock Input (1)        |
| 114 | I2S IN | BCKI1     | GPIO1[23] | I/O | Digital Audio Bit Clock Input (1)            |
| 115 | I2S IN | DATAI1    | GPIO1[24] | I/O | Digital Audio Data Input (1)                 |
| 116 | UART   | UART1_RTS | GPIO1[25] | I/O | UART1 Transfer Request                       |
| 117 | UART   | UART1_CTS | GPIO1[26] | I/O | UART1 Clear Request                          |
| 118 | I2C    | SCL1      | GPIO1[27] | I/O | I2C Clock I/O (1), Open drain output pin     |
| 119 | I2C    | SDA1      | GPIO1[28] | I/O | I2C Data I/O (1), Open drain output pin      |
| 120 | RCR    | RCR       | GPIO1[29] | I/O | Remote Controller Signal Input               |
| 121 | UART   | UART1_RXD | GPIO1[30] | I/O | UART1 Receive Data                           |
| 122 | UART   | UART1_TXD | GPIO1[31] | I/O | UART1 Transmit Data                          |
| 123 | POWER  | DVSS      |           | -   | GND  |
| 124 | CLOCK  | XIN_32K   |           | I   | X'tal(32.768KHz) connection input pin.       |
| 125 | CLOCK  | XOUT_32K  |           | O   | X'tal(32.768KHz) connection output pin.      |
| 126 | TEST   | TMODE     |           | I   | Test Mode pin: This pin is connected to GND. |
| 127 | CLOCK  | XIN_PLL   |           | I   | X'tal(16.9344MHz) Connection Input           |
| 128 | CLOCK  | XOUT_PLL  |           | O   | X'tal(16.9344MHz) Connection Output          |

Application Circuit Diagram

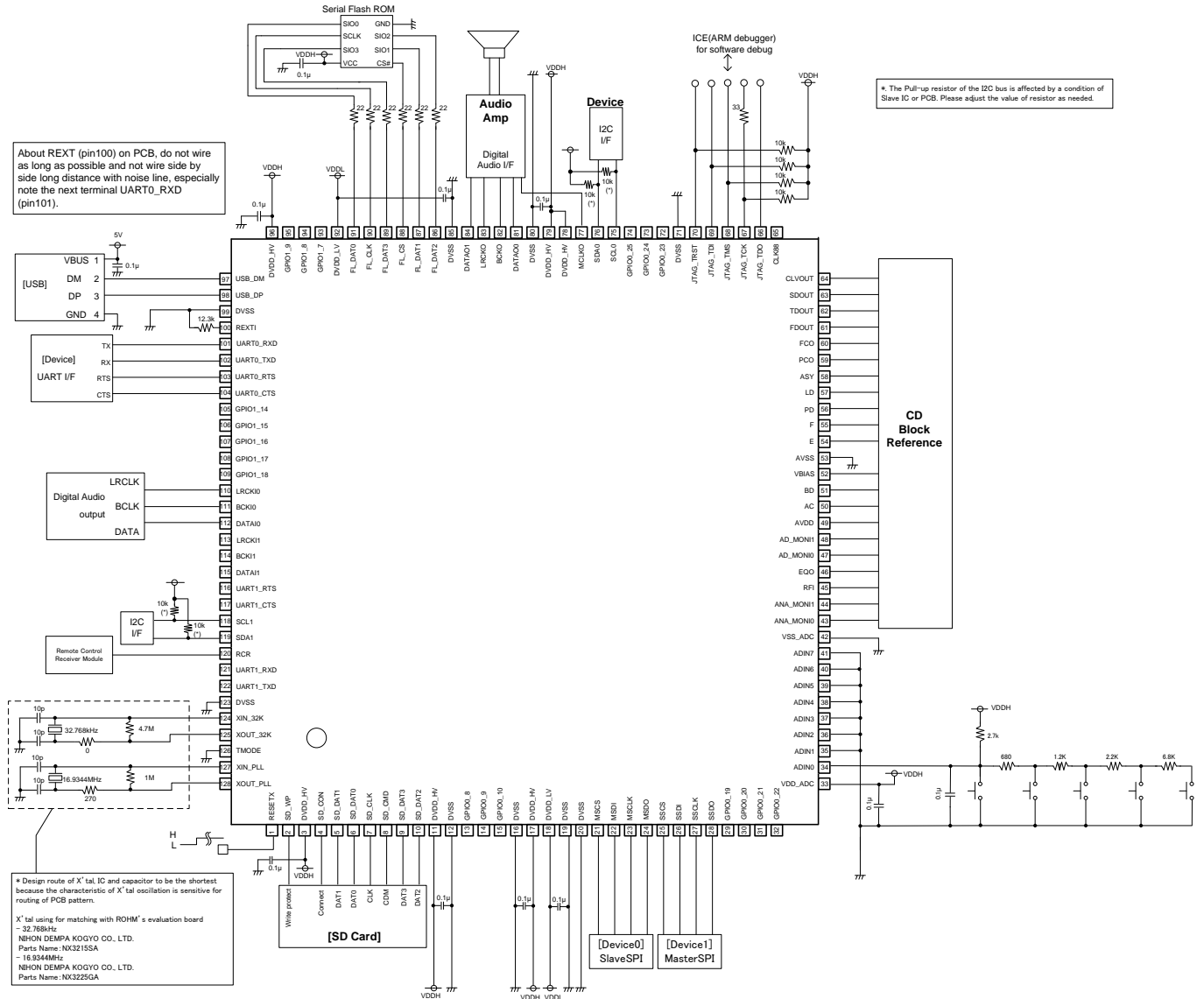


Figure 3. Application Circuit Diagram

**Absolute Maximum Ratings (Ta=25°C)**

| Parameter                    | Symbol  | Rating           | Unit | Remarks                |
|------------------------------|---------|------------------|------|------------------------|
| Input Voltage (Analog, I/O)  | VDDHMAX | -0.3 to +4.5     | V    | DVDD_HV, VDD_ADC, AVDD |
| Input Voltage (Core)         | VDDLMAX | -0.3 to +2.1     | V    | DVDD_LV                |
| Input Voltage                | VIN     | -0.3 to VDDH+0.3 | V    |                        |
| Storage Temperature Range    | TSTG    | -55 to +125      | °C   |                        |
| Operating Temperature Range  | TOPR    | -40 to +85       | °C   |                        |
| Maximum Junction Temperature | Tjmax   | +125             | °C   |                        |

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Recommended Operating Conditions (Ta=25°C)**

| Parameter                   | Symbol | Rating       | Unit | Remarks                |
|-----------------------------|--------|--------------|------|------------------------|
| Input Voltage (Analog, I/O) | VDDH   | 3.0 to 3.6   | V    | DVDD_HV, VDD_ADC, AVDD |
| Input Voltage (Core)        | VDDL   | 1.45 to 1.65 | V    | DVDD_LV                |

**Thermal Resistance** (Note 1)

| Parameter   | Symbol        | Thermal Resistance (Typ) |               | Unit |
|---|---------------|--------------------------|---------------|------|
|   |               | 1s (Note 3)              | 2s2p (Note 4) |      |
| HTQFP128UA  |               |                          |               |      |
| Junction to Ambient                                 | $\theta_{JA}$ | 54.9                     | 27.6          | °C/W |
| Junction to Top Characterization Parameter (Note 2) | $\Psi_{JT}$   | 10                       | 9             | °C/W |

(Note 1) Based on JE51-2A(Still-Air)

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JE51-3.

(Note 4) Using a PCB board based on JE51-5, 7.

| Layer Number of Measurement Board | Material | Board Size                |
|-----------------------------------|----------|---------------------------|
| Single                            | FR-4     | 114.3mm x 76.2mm x 1.57mm |

| Top                   |           |
|-----------------------|-----------|
| Copper Pattern        | Thickness |
| Footprints and Traces | 70µm      |

| Layer Number of Measurement Board | Material | Board Size               | Thermal Via (Note 5) |          |
|-----------------------------------|----------|--------------------------|----------------------|----------|
|                                   |          |                          | Pitch                | Diameter |
| 4 Layers                          | FR-4     | 114.3mm x 76.2mm x 1.6mm | 1.20mm               | Φ0.30mm  |

| Top                   |           | 2 Internal Layers |           | Bottom          |           |
|-----------------------|-----------|-------------------|-----------|-----------------|-----------|
| Copper Pattern        | Thickness | Copper Pattern    | Thickness | Copper Pattern  | Thickness |
| Footprints and Traces | 70µm      | 74.2mm (Square)   | 35µm      | 74.2mm (Square) | 70µm      |

(Note 5) This thermal via connects with the copper pattern of all layers.

**Caution:** As reference information of thermal design, thermal resistance of 1s and 2s2p are described. If the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. Increase the board size and copper area to prevent exceeding the maximum junction temperature rating. This IC is recommended more than 2s PCB.

**Electrical Characteristics**

(Unless otherwise noted, Ta=25°C, DVDD\_HV = VDD\_ADC = AVDD = 3.3V, DVDD\_LV = 1.5V, DVSS=VSS\_ADC=AVSS =0V, XIN\_PLL= 16.9344MHz, XIN\_32K =32.768kHz, REXTI pin externally fitted resistance = 12.3 kΩ±1%)

| Parameter                                    | Symbol  | Rating   |     |          | Unit | Conditions Suitable Pin  |
|--|---------|----------|-----|----------|------|--|
|  |         | MIN      | TYP | MAX      |      |  |
| <Overall>                                    |         |          |     |          |      |  |
| Operating Current Consumption (VDDH)         | IDDFS1  | -        | 65  | 130      | mA   | Using USB Full-Speed   |
| Operating Current Consumption (VDDL)         | IDD2    | -        | 150 | 210      | mA   |  |
| In a standby mode Consumption current (VDDH) | ISTBH   | -        | 1.1 | -        | mA   | At standby mode  |
| In a standby mode Consumption current (VDDL) | ISTBL   | -        | 50  | -        | µA   | At standby mode  |
| <Logic Interface>                            |         |          |     |          |      |  |
| H input current                              | IIH     | -        | -   | 1.0      | µA   | (Note 1)   |
| L input current                              | IIL     | -1.0     | -   | -        | µA   | (Note 1)   |
| Input "H" Voltage                            | VIH     | VDDH*0.7 | -   | VDDH     | V    | (Note 1)   |
| Input "L" Voltage                            | VIL     | DVSS     | -   | VDDH*0.3 | V    | (Note 1)   |
| Output "H" Voltage 1                         | VOH1    | VDDH-0.4 | -   | VDDH     | V    | IOH=-1.6mA, (Note 2)   |
| Output "L" Voltage 1                         | VOL1    | 0        | -   | 0.4      | V    | IOL=1.6mA, (Note 2)  |
| Output "H" Voltage 2                         | VOH2    | VDDH-0.4 | -   | VDDH     | V    | IOH=-3.6mA, (Note 3)   |
| Output "L" Voltage 2                         | VOL2    | 0        | -   | 0.4      | V    | IOL=3.6mA, (Note 3) (Note 4)   |
| Output "H" Voltage 3                         | VOH3    | VDDH-1.0 | -   | VDDH     | V    | IOH=-0.6mA, (Note 5)   |
| Output "L" Voltage 3                         | VOL3    | 0        | -   | 1.0      | V    | IOL=0.6mA, (Note 5)  |
| <USB Interface>                              |         |          |     |          |      |  |
| Idle Pull-Up Resistance                      | RPU_ID  | 0.9      | -   | 1.575    | kΩ   | (Note 7)   |
| RX Pull-Up Resistance                        | RPU_RX  | 1.425    | -   | 3.09     | kΩ   | (Note 7)   |
| Pull-Down Resistance                         | RPD     | 14.25    | -   | 24.8     | kΩ   | (Note 6)   |
| FS High Output Impedance                     | ZFDRH   | -        | 45  | -        | Ω    | (Note 6)   |
| FS Low Output Impedance                      | ZFDRL   | -        | 45  | -        | Ω    | (Note 6)   |
| FS High Voltage                              | VFOH    | 2.8      | -   | 3.6      | V    | Measured when pin is pulled down to VSS using 15 kΩ resistor (Note 6)    |
| FS Low Voltage                               | VFOL    | 0        | -   | 0.3      | V    | Measured when pin is pulled up to DVDD_HV using 1.5 kΩ resistor (Note 6) |
| FS RX Differential Input Sensitivity         | VFLSNS  | -        | -   | 200      | mV   | (Note 6)   |
| FS RX Differential Input Range               | VFLCM   | 0.8      | -   | 2.5      | V    | (Note 6)   |
| H input voltage                              | VIHUSB  | 2        | -   | VDDH     | V    | (Note 6)   |
| L input voltage                              | VILUSB  | DVSS     | -   | 0.8      | V    | (Note 6)   |
| <ADC>  |         |          |     |          |      |  |
| A/D Conversion Frequency                     | FADCONV | -        | -   | 705.6    | kHz  | FADCONV≤16.9344MHz/24  |
| Analog Input Voltage Range                   | VAIN    | 0.1*VDDH | -   | 0.9*VDDH | V    |  |
| Differential Non-Linearity                   | DNL     | -        | -   | ±5       | LSB  |  |
| Integral Non-Linearity                       | INL     | -        | -   | ±5       | LSB  |  |

- (Note 1) Input pin 1,2,4-10,13-15,21-32,34-41,43-44,47-48,65,67-70,72-77,81-84,86-91,93-95,101-122 pin
- (Note 2) Output pin1 13-15,29-32,34-41,43,44,47,48,61-66,77,81-84,93-95,101-117,120-122 pin
- (Note 3) Output pin2 2,4-10,21-28,72-74,86-91 pin
- (Note 4) Output pin3 75,76,118,119 pin
- (Note 5) Output pin4 125,128 pin
- (Note 6) USB pin 97,98 pin
- (Note 7) USB pin 98 pin

## Electrical Characteristics – continued

(Unless otherwise noted, Ta=25°C, DVDD\_HV = VDD\_ADC = AVDD = 3.0V, DVDD\_LV = 1.55V, DVSS= VSS\_ADC= AVSS= 0V, XIN\_PLL= 16.9344MHz, XIN\_32K =32.768kHz, RL=10kΩ, VBIAS=Reference)

| Parameter                     | Symbol | Rating |      |      | Unit | Conditions Suitable Pin                |
|-------------------------------|--------|--------|------|------|------|--|
|                               |        | MIN    | TYP  | MAX  |      |  |
| <PLL (VCO) Block>             |        |        |      |      |      |  |
| Maximum Oscillation Frequency | fVCOH  | 4.6    | 6.5  | -    | MHz  | GPIO1_7,1/4 of VCO Output              |
| Minimum Oscillation Frequency | fVCOL  | -      | 1.1  | 1.7  | MHz  | GPIO1_7,1/4 of VCO Output              |
| <FC DAC>                      |        |        |      |      |      |  |
| Offset Voltage                | VFCOF  | -50    | -    | +50  | mV   | FCO                                    |
| Maximum Output Voltage        | VFCH   | 0.2    | 0.5  | -    | V    | FCO                                    |
| Minimum Output Voltage        | VFCL   | -      | -0.5 | -0.2 | V    | FCO                                    |
| <PCO.>                        |        |        |      |      |      |  |
| Output "L" Voltage            | VPCH   | -      | -1.0 | -0.6 | V    | PCO                                    |
| Output "H" Voltage            | VPCL   | 0.6    | 1.0  | -    | V    | PCO                                    |
| < EFM Comparator >            |        |        |      |      |      |  |
| Threshold Voltage             | VEFM   | -200   | -    | 200  | mV   | RFI,ANA_MONIO,GPIO1_8                  |
| <Servo ADC>                   |        |        |      |      |      |  |
| Offset Voltage                | VADOF  | -140   | -    | +140 | mV   | ANA_MONIO,ANA_MONI1                    |
| Maximum Conversion Voltage    | VADH   | 1.0    | 1.2  | 1.4  | V    | ANA_MONIO,ANA_MONI1                    |
| Minimum Conversion Voltage    | VADL   | -1.4   | -1.2 | -1.0 | V    | ANA_MONIO,ANA_MONI1                    |
| <Servo DAC>                   |        |        |      |      |      |  |
| Offset Voltage                | VDAOF  | -80    | -    | +80  | mV   | FDOUT,TDOUT,SDOUT,CLVOUT               |
| Maximum Output Voltage        | VDAH   | 0.8    | 1.2  | -    | V    | FDOUT,TDOUT,SDOUT,CLVOUT               |
| Minimum Output Voltage        | VDAL   | -      | -1.2 | -0.8 | V    | FDOUT,TDOUT,SDOUT,CLVOUT               |
| <Bias Amplifier>              |        |        |      |      |      |  |
| Maximum Output Current        | IBO    | -      | ±1.5 | -    | mA   | VBIAS, BIAS Fluctuation: 200mV or less |
| <RF Amplifier>                |        |        |      |      |      |  |
| Offset Voltage                | VRFOF  | -      | 0    | -    | mV   | AC,BD,EQO                              |
| Maximum Output Voltage        | VRFH   | 1.0    | 1.2  | -    | V    | AC,BD,EQO                              |
| Minimum Output Voltage        | VRFL   | -      | -1.3 | -1.1 | V    | AC,BD,EQO                              |
| <FE Amplifier>                |        |        |      |      |      |  |
| Offset Voltage                | VFEOF  | -      | 0    | -    | mV   | AC,BD,ANA_MONIO,ANA_MONI1              |
| Maximum Output Voltage        | VFEH   | 1.0    | 1.4  | -    | V    | AC,BD,ANA_MONIO,ANA_MONI1              |
| Minimum Output Voltage        | VFEL   | -      | -1.4 | -1.0 | V    | AC,BD,ANA_MONIO,ANA_MONI1              |
| <TE Amplifier>                |        |        |      |      |      |  |
| Offset Voltage                | VTEOF  | -      | 70   | -    | mV   | E,F,ANA_MONIO,ANA_MONI1                |
| Maximum Output Voltage        | VTEH   | 1.0    | 1.4  | -    | V    | E,F,ANA_MONIO,ANA_MONI1                |
| Minimum Output Voltage        | VTEL   | -      | -1.4 | -1.0 | V    | E,F,ANA_MONIO,ANA_MONI1                |
| <Asymmetry Amplifier>         |        |        |      |      |      |  |
| Offset Voltage                | VASYOF | -      | 0    | -    | mV   | ASY=VBIAS,RFI,ANA_MONIO                |
| Maximum Output Voltage        | VASYH  | 1.1    | 1.4  | -    | V    | ASY,RFI,ANA_MONIO                      |
| Minimum Output Voltage        | VASYL  | -      | -1.4 | -1.1 | V    | ASY,RFI,ANA_MONIO                      |
| <APC Block>                   |        |        |      |      |      |  |
| Output Voltage 1              | VAPC1  | 2.4    | 2.8  | -    | V    | PD="H", LD,ANA_MONIO                   |
| Output Voltage 2              | VAPC2  | -      | 0.1  | 0.5  | V    | PD="L", LD,ANA_MONIO                   |
| Maximum Reference Voltage     | VAPCH  | -      | 220  | -    | mV   | PD,LD,ANA_MONIO                        |
| Minimum Reference             | VAPCL  | -      | 145  | -    | mV   | PD,LD,ANA_MONIO                        |

Application Information

Power on/ Reset Timing/ Power off

Release the Reset Signal by L input with over 100µs after clock input from I/O pins of 16.9344MHz becomes stable.  
(See Figure 4)

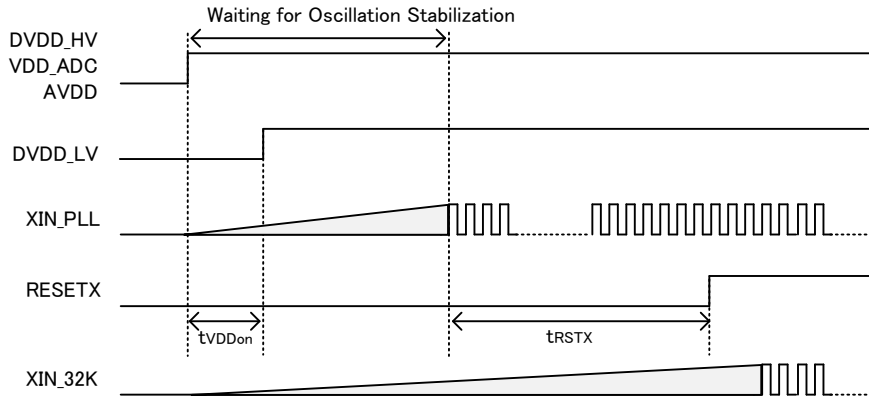


Figure 4. Power on/ Reset Timing

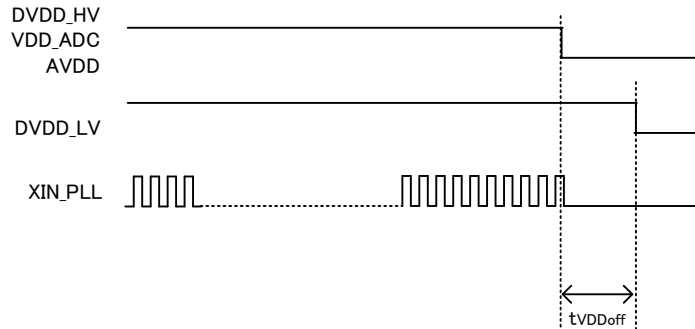


Figure 5. Power off

| Parameter                                  | Symbol  | Rating |     |     | Unit | Remarks |
|--|---------|--------|-----|-----|------|---------|
|  |         | MIN    | TYP | MAX |      |         |
| Time lag of Power Supply at Starting       | tVDDon  | 0      | -   | -   | ms   |         |
| Reset L Interval                           | tRSTX   | 100    | -   | -   | µs   |         |
| Time lag of Power Supply at Shutting down. | tVDDoff | 0      | -   | -   | ms   |         |

Note) There is a risk that the electric current flows in case the order of power supply starting and shutting down is other than the above order.

Oscillation Stable Time

Suggested value for XIN\_PLL(16.9344MHz) oscillation stable time is 4ms.

Suggested value for XIN\_32K(32.768kHz) oscillation stable time is 500ms.

The above-mentioned oscillation stable time cannot be guaranteed since the oscillation stable time depends on crystal oscillator, external constant, or board layout. Check the oscillation stable time of your own system.

I/O Equivalence Circuits

| No. | Name      | I/O | Power   | Internal Circuits | No. | Name      | I/O | Power   | Internal Circuits |
|-----|-----------|-----|---------|-------------------|-----|-----------|-----|---------|-------------------|
| 1   | RESETX    | I   | DVDD_HV |                   | 2   | SD_WP     | I   | DVDD_HV |                   |
| 34  | ADIN0     | I   | VDD_ADC |                   | 4   | SD_CON    | I   |         |                   |
| 35  | ADIN1     | I   |         |                   |     |           |     |         |                   |
| 36  | ADIN2     | I   |         |                   |     |           |     |         |                   |
| 37  | ADIN3     | I   |         |                   |     |           |     |         |                   |
| 38  | ADIN4     | I   |         |                   |     |           |     |         |                   |
| 39  | ADIN5     | I   |         |                   |     |           |     |         |                   |
| 40  | ADIN6     | I   |         |                   |     |           |     |         |                   |
| 41  | ADIN7     | I   |         |                   |     |           |     |         |                   |
| 43  | ANA_MONI0 | O   | AVDD    |                   | 5   | SD_DAT1   | I/O |         |                   |
| 44  | ANA_MONI1 | O   |         |                   |     |           |     |         |                   |
| 47  | AD_MONI0  | O   |         |                   |     |           |     |         |                   |
| 48  | AD_MONI1  | O   |         |                   |     |           |     |         |                   |
| 61  | FDOUT     | O   |         |                   |     |           |     |         |                   |
| 62  | TDOUT     | O   |         |                   |     |           |     |         |                   |
| 63  | SDOUT     | O   |         |                   |     |           |     |         |                   |
| 64  | CLVOUT    | O   |         |                   |     |           |     |         |                   |
| 45  | RFI       | I   | AVDD    |                   | 65  | CLK88     | O   |         |                   |
| 46  | EQO       | O   | AVDD    |                   | 72  | GPIO0_23  | I/O |         |                   |
| 50  | AC        | I   | AVDD    |                   | 73  | GPIO0_24  | I/O |         |                   |
| 51  | BD        | I   |         |                   |     |           |     |         |                   |
| 54  | E         | I   | AVDD    |                   | 74  | GPIO0_25  | I/O |         |                   |
| 55  | F         | I   |         |                   |     |           |     |         |                   |
|     |           |     |         |                   | 77  | MCLKO     | O   |         |                   |
|     |           |     |         |                   | 81  | DATA00    | O   |         |                   |
|     |           |     |         |                   | 82  | BCKO      | O   |         |                   |
|     |           |     |         |                   | 83  | LRCKO     | O   |         |                   |
|     |           |     |         |                   | 84  | DATA01    | O   |         |                   |
|     |           |     |         |                   | 93  | GPIO1_7   | I/O |         |                   |
|     |           |     |         |                   | 94  | GPIO1_8   | I/O |         |                   |
|     |           |     |         |                   | 95  | GPIO1_9   | I/O |         |                   |
|     |           |     |         |                   | 101 | UART0_RXD | I   |         |                   |
|     |           |     |         |                   | 102 | UART0_TXD | O   |         |                   |
|     |           |     |         |                   | 103 | UART0_RTS | O   |         |                   |
|     |           |     |         |                   | 104 | UART0_CTS | I   |         |                   |
|     |           |     |         |                   | 105 | GPIO1_14  | I/O |         |                   |
|     |           |     |         |                   | 106 | GPIO1_15  | I/O |         |                   |
|     |           |     |         |                   | 107 | GPIO1_16  | I/O |         |                   |
|     |           |     |         |                   | 108 | GPIO1_17  | I/O |         |                   |
|     |           |     |         |                   | 109 | GPIO1_18  | I/O |         |                   |
|     |           |     |         |                   | 110 | LRCKI0    | I   |         |                   |
|     |           |     |         |                   | 111 | BCKI0     | I   |         |                   |
|     |           |     |         |                   | 112 | DATAI0    | I   |         |                   |
|     |           |     |         |                   | 113 | LRCKI1    | I   |         |                   |
|     |           |     |         |                   | 114 | BCKI1     | I   |         |                   |
|     |           |     |         |                   | 115 | DATAI1    | I   |         |                   |
|     |           |     |         |                   | 116 | UART1_RTS | I/O |         |                   |
|     |           |     |         |                   | 117 | UART1_CTS | I/O |         |                   |
|     |           |     |         |                   | 120 | RCR       | I   |         |                   |
|     |           |     |         |                   | 121 | UART1_RXD | I   |         |                   |
|     |           |     |         |                   | 122 | UART1_TXD | O   |         |                   |

Figure 6. I/O equivalence circuits 1



I/O Equivalence Circuits – continued

| No. | Name      | I/O | Power   | Internal Circuits | No. | Name     | I/O | Power   | Internal Circuits |
|-----|-----------|-----|---------|-------------------|-----|----------|-----|---------|-------------------|
| 56  | PD        | I   | AVDD    |                   | 75  | SCL0     | I/O | DVDD_HV |                   |
| 57  | LD        | O   |         |                   | 76  | SDA0     | I/O |         |                   |
| 58  | ASY       | I   | AVDD    |                   | 118 | SCL1     | I/O |         |                   |
|     |           |     |         |                   | 119 | SDA1     | I/O |         |                   |
|     |           |     |         |                   | 86  | FL_DAT2  | I/O |         |                   |
|     |           |     |         |                   | 87  | FL_DAT1  | I/O |         |                   |
|     |           |     |         |                   | 88  | FL_CS    | O   |         |                   |
| 52  | VBIAS     | O   | AVDD    |                   | 89  | FL_DAT3  | I/O |         |                   |
|     |           |     |         |                   | 90  | FL_CLK   | O   |         |                   |
| 59  | PCO       | O   | AVDD    |                   | 91  | FL_DAT0  | I/O |         |                   |
|     |           |     |         |                   | 60  | FCO      | O   |         |                   |
| 97  | USB_DM    | I/O | DVDD_HV |                   | 100 | REXTI    | I   | DVDD_HV |                   |
|     |           |     |         |                   | 98  | USB_DP   | I/O |         |                   |
| 124 | XIN_32K   | I   | DVDD_HV |                   | 127 | XIN_PLL  | I   | DVDD_HV |                   |
|     |           |     |         |                   |     |          |     |         |                   |
| 66  | JTAG_TDO  | O   | DVDD_HV |                   | 128 | XOUT_PLL | O   | DVDD_HV |                   |
| 67  | JTAG_TCK  | I   | DVDD_HV |                   |     |          |     |         |                   |
| 68  | JTAG_TMS  | I   |         |                   |     |          |     |         |                   |
| 69  | JTAG_TDI  | I   |         |                   |     |          |     |         |                   |
| 70  | JTAG_TRST | I   |         |                   |     |          |     |         |                   |
| 126 | TMODE     | I   |         |                   |     |          |     |         |                   |

Figure 7. I/O equivalence circuits 2

**Operational Notes1**

1. About Compatibility in USB Memory Device and SD Memory Card  
According to the file structure and communication speed of USB memory, SD memory card, this LSI might not play back correctly.
2. About Compatibility in Bluetooth device  
According to the type of Bluetooth device, , this LSI might not play back correctly.
3. About 2X Speed Recording  
Recording to a memory with slow access speed may require data connection operation.  
2X speed recording to all the memories cannot be guaranteed.
4. Power OFF or Memory Disconnection Under Memory Writing  
The sudden power off or memory disconnection during recording or file write operation to a memory may break the data in a memory.
5. Browsing Operation  
With a memory with slow access speed, browsing operation during music playing may generate skipping.
6. CD-ROM Playing  
CD-ROM playing operation is premised on data being inputted so that an internal data buffer may not become empty.  
When an input does not meet the deadline and internal data buffers become empty, skipping occurs.
7. Playing Time of MP3 File  
The playing time when MP3 file playing may shift when fast forward playing, rewind playing, and VBR playing.
8. Write-In Operation Exceeding Memory Size  
Writing to a file when memory size is exceeded is not supported.
9. Write-In Operation of the File Size Exceeding FAT Specification  
Writing to a file when file size is exceeded is not supported.
10. About I2C Format I/F  
Although this LSI has adopted the I2C format, the level shifter circuit is not built in.  
For this reason, level shifter is needed for connection with the device besides the range of operating power supply voltage of this LSI.
11. CD Media Playing  
According to the condition of CD media, flawed, dirty, curved, eccentric and etc., this LSI might not play back normally.
12. Application Block Diagram  
Each software function of Audio Encoder, Audio Decoder, BT stack A2DP, SBC Decoder and File System(FTA12/16/32, ISO9660) described in Figure 1. Application Block are realized by downloading applicable program from external Serial Flash ROM.

## Operational Notes2

1. **Reverse Connection of Power Supply**  
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.
2. **Power Supply Lines**  
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
3. **Ground Voltage**  
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
4. **Ground Wiring Pattern**  
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.
5. **Thermal Consideration**  
Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.
6. **Recommended Operating Conditions**  
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
7. **Inrush Current**  
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.
8. **Operation Under Strong Electromagnetic Field**  
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

**Operational Notes2 – continued**

9. **Testing on Application Boards**  
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
10. **Inter-pin Short and Mounting Errors**  
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.
11. **Unused Input Pins**  
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.
12. **Regarding the Input Pin of the IC**  
In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.
13. **Ceramic Capacitor**  
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

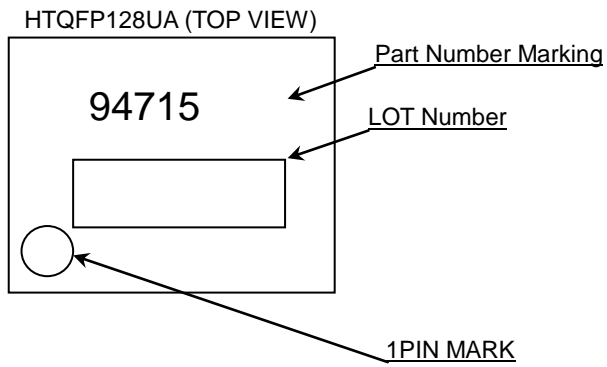
Ordering Information

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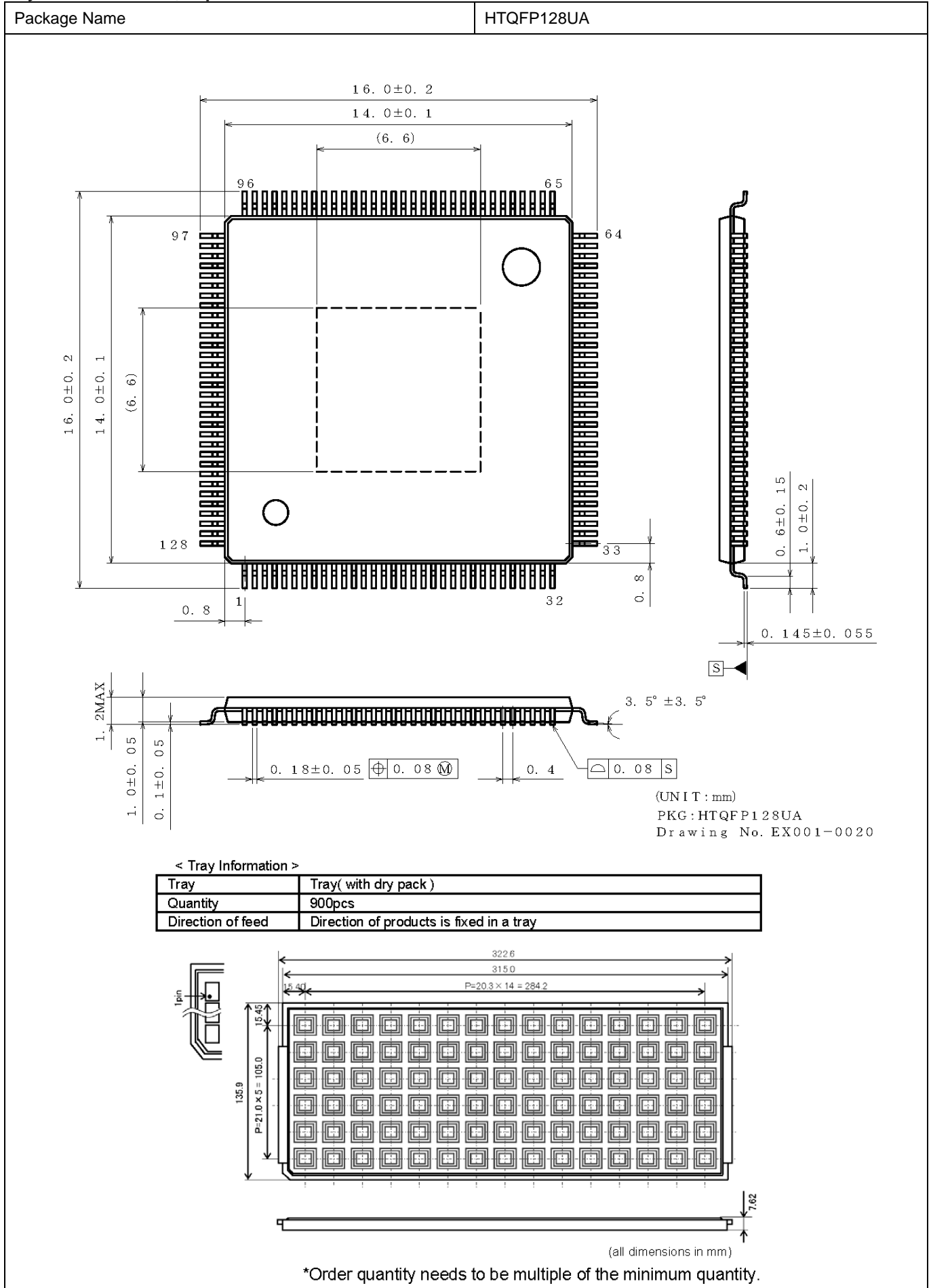
Part Number

Package  
HTQFP128UA, supply with tray

Marking Diagram



Physical Dimension, Tape and Reel Information



**Revision History**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 22.Dec.2016 | 001      | New Release  |
| 25.Jan.2017 | 002      | P10: Modified Block name of 118/119pin to I2C.<br>P18: Added Note about Application Block diagram. |



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|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV  |           | CLASS III  |           |

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  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
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- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

### Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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