

BOE

1.0 cm(Type 0.39) Active Matrix Color OLED Panel Module

1. Overview/Application

BO039M1920M is a 0.39 inch (1 cm) diagonal, FHD resolution(1920 x1080), active matrix color OLED (Organic Light Emitting Display)panel module based on single crystal silicon backplane . The pixel circuits and driving IC are integrated on the silicon backplane to get the compact size and very low power consumption.

(Potential applications: Virtual Reality application (AR/VR) , Head mounted displays, Near-Eye Displays etc.)

2. Features

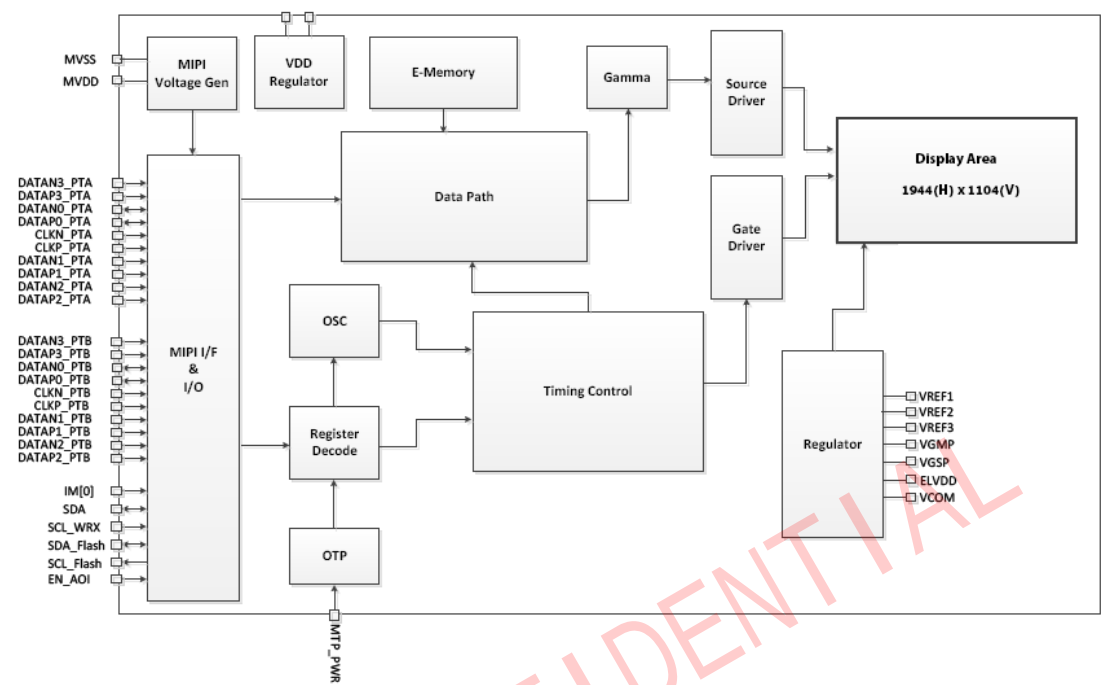
- Small-size, high resolution 0.39 FHD Display PPI=5644
 - AP Operated Resolution (8*M, M=40~240) x RGB x (8*N, N=30~135)
 - Full color mode, 16.7M colors
 - Fast response
 - Thin and light in weight
 - Color enhancement, Sharpness enhancement
 - High contrast mode
 - High fluency mode
 - Power-saving (PS) mode
 - Scan direction selection, up or down
 - Interface, Support MIPI only or MIPI(data)+I²C(CMD)
-

3. Module Structure

- Active matrix color OLED display with on-chip driver based on single crystal silicon transistors

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4. System Block Diagram



5. Pin Description

5.1 Interface Logic Pin

Signal	Type	Description									
RESX	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.									
IM[0]	I	Use to select the Interface type. <table><tr><td>IM[0]</td><td>Command Execute</td><td>Image Write</td></tr><tr><td>0</td><td>MIPI</td><td>MIPI</td></tr><tr><td>1</td><td>I2C</td><td>MIPI</td></tr></table> Note: MIPI 1port or 2port is selected by register setting	IM[0]	Command Execute	Image Write	0	MIPI	MIPI	1	I2C	MIPI
IM[0]	Command Execute	Image Write									
0	MIPI	MIPI									
1	I2C	MIPI									
OCP_OUT	O	Over current protect flag.									
OTP_SEL	I	MTP type selection. OTP_SEL=0: use internal OTP OTP_SEL=1: use external OTP									
MTP_PWR	I	MTP program power, 7.75V. If not use, please connect to GND or OPEN.									
EN_AOI	I	AOI mode enable. EN_AOI=0: AOI mode disable EN_AOI=1:AOI mode enable									

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5.2 Interface Pin

Signal	Type	Description
CLKP_PTA/B CLKN_PTA/B	I	These pins are DSI-CLK+/- differential clock signals if MIPI Port A/B interface is used. CLKP/N_PTA/B are differential small amplitude signals. If not used, please keep it open.
DATA0P_PTA/B DATA0N_PTA/B	I/O	These pins are DSI-D0+/-differential clock signals if MIPI Port A/B interface is used. DATA0P/N_PTA/B are differential small amplitude signals. If not used, please keep it open.
DATA1P_PTA/B DATA1N_PTA/B	I/O	These pins are DSI-D1+/-differential clock signals if MIPI Port A/B interface is used. DATA1P/N_PTA/B are differential small amplitude signals. If not used, please keep it open.
DATA2P_PTA/B DATA2N_PTA/B	I/O	These pins are DSI-D2+/-differential clock signals if MIPI Port A/B interface is used. DATA2P/N_PTA/B are differential small amplitude signals. If not used, please keep it open.
DATA3P_PTA/B DATA3N_PTA/B	I/O	These pins are DSI-D3+/-differential clock signals if MIPI Port A/B interface is used. DATA3P/N_PTA/B are differential small amplitude signals. If not used, please keep it open.
SDA	I	Bi-direction data PIN in I2C I/F. If this pin is not used, please connect to VDDI.
SCL_WRX	I/O	Synchronous clock signal in I2C I/F. If this pin is not used, please connect to VDDI.
SDA_FLASH	I/O	Bi-direction data PIN in I2C I/F for external EEROM. If this pin is not used, please keep it open.
SCL_FLASH	O	Synchronous clock signal in I2C I/F for external EEROM. If this pin is not used, please keep it open.

5.3 Power Supply Pin

Signal	Type	Description
VDDI	P	Power supply for interface system except for the interface
AVDD AVDD_DC	P	Power supply for analog system. AVDD/AVDD_DC should be the same input voltage. Please divide the signals on panel layout and connect the signals together on FPC. Need stabilize capacitance
ELVDD	P	Power supply for OLED cell.
AVEE	P	Power supply for OLED cell.
VSS	P	System GND for internal digital system.
AVSS	P	System GND for analog system.
AVSS_DC	P	System GND for power generation system. Please divide the signals on panel layout and connect the signals to AVSS on FPC.
MVSS	P	System GND for MIPI interface.

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5.4 Regulator Pin

Signal	Type	Description
DVDD	O	Regulator output for logic system power. Connect a capacitor for stabilization.
MVDDA	O	Regulator output for MIPI digital system power. Connect a capacitor for stabilization.
MVDDL	O	Regulator output for MIPI analog system power. Connect a capacitor for stabilization.
VGMP	O	Regulator output for gamma high voltage generation. Connect a capacitor for stabilization.
VGSP	O	Regulator output for gamma low voltage generation. Connect a capacitor for stabilization.
VCOM	O	Regulator output for common electrode voltage. Connect a capacitor for stabilization.
VREF1	O	Regulator output for internal reference voltage. Connect a capacitor for stabilization.
VREF2	O	Regulator output for internal reference voltage. Connect a capacitor for stabilization.
VREF3	O	Regulator output for internal reference voltage. Connect a capacitor for stabilization.

5.5 Test Pin

Signal	Type	Description
PADA PADB PADC PADD	-	Bonding test pin.

6. Absolute Maximum Ratings

The absolute maximum rating is listed on the below table. When the VTOS6201 is used beyond the absolute maximum ratings, it may be permanently damaged. It is strongly recommended use the drive IC within the following specified limits for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the driver IC will malfunction and cause poor reliability.

Item	Symbol	Value	Unit
Power Supply Voltage (1)	VDDI	4	V
Power Supply Voltage (2)	AVDD-AVSS	7	V
	AVEE-AVSS	7	V
Power Supply Voltage in AOI mode 1	VDDI	1.65	V
	AVDD-AVSS	7	V
	AVEE-AVSS	7	V
Power Supply Voltage in AOI mode 2	AOI_VDDI	1.65	V
	AOI_AVDD	7	V
	AOI_ELVDD	7	V
	AOI_AVEE	7	V
MIPI Differential Input	CLKP_PTA/B, CLKN_PTA/B DATA0_PTA/B, DATAN0_PTA/B DATA1_PTA/B, DATAN1_PTA/B DATA2_PTA/B, DATAN2_PTA/B DATA3_PTA/B, DATAN3_PTA/B	1.32	V
Input Voltage of Interface	Vin	-0.3~VDDI+0.3	V
Output Voltage of Interface	Vo	-0.3~VDDI+0.3	V
Operating temperature	Topr	-40~85	°C
Storage temperature	Tstg	-55~125	°C

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7. Recommended Operating Conditions

Item	Parameter	Min	Typ	Max	Unit
Power Supply Voltage	VDDI	1.65	1.8	1.95	V
	AVDD-AVSS	5		6	V
	AVEE-AVSS	-5		-6	V
Power Supply Voltage in AOI mode 1	VDDI		1.6		V
	AVDD-AVSS	1.8		5	V
	AVEE-AVSS	-2		-5	V
Power Supply Voltage in AOI mode 2	AOI_VDDI		1.6		V
	AOI_AVDD	1.8		5	V
	AOI_ELVDD	1.8		5	V
	AOI_AVEE	-2		-5	V
	AOI_VSS		0		V
Input Voltage of Interface	V _{in}	-0.3		VDDI+0.3	V
Output Voltage of Interface	V _o	-0.3		VDDI+0.3	V
Operating temperature	T _{opr}	-40		85	°C
Storage temperature	T _{stg}	-55		125	°C

8. Electrical Characteristics

8.1 DC Characteristics

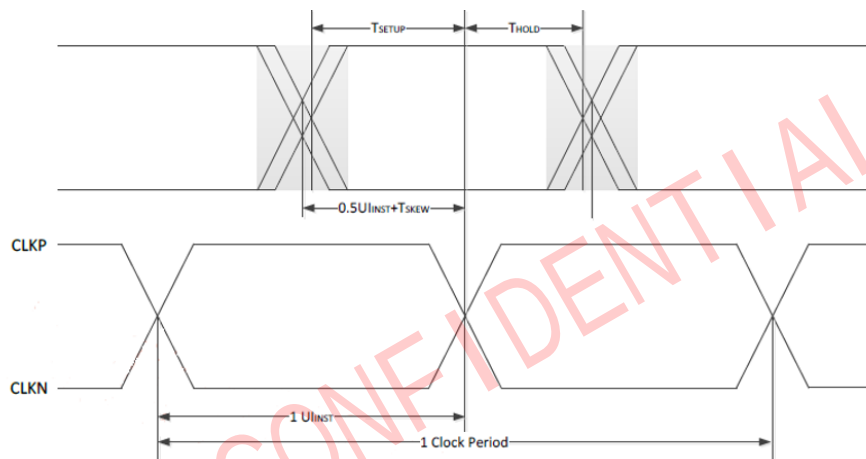
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power & Operation Voltage						
AVDD Input Level	AVDD	-	5.0		6.0	V
Digital I/O Power Supply (non-MIPI I/O)	VDDI	-		1.8		V
Digital I/O Input Level @Logic High	V _{IH}	VDDI=1.65V ~ 1.95V	0.7*VDDI	-	VDDI	V
Digital I/O Input Level @Logic Low	V _{IL}	VDDI=1.65V ~ 1.95V	0		0.3*VDDI	V
Digital I/O Output Level @Logic High	V _{OH}	I _{out} = -1mA	0.8*VDDI	-	VDDI	V
Digital I/O Output Level @Logic Low	V _{OL}	I _{out} = +1mA	0	-	0.2*VDDI	V
Digital I/O Input leakage @Logic High	I _{IHD}	V _{in} = VDDI			1	uA
Digital I/O Input leakage @Logic Low	I _{ILD}	V _{in} = 0	-1			uA
MIPI I/O Power Supply	MVDD	-	-	1.2	-	V
MIPI Input leakage @Logic High	I _{IHMD}	V _{in} = MVDD			1	uA
MIPI Input leakage @Logic Low	I _{ILMD}	V _{in} = 0	-1			uA
Reference Voltage	VREF1	-	-	1.9	-	V
Panel Reference Voltage	VREF2	-	-0.3	-	-2	V
	VREF3	-	-0.3	-	-2	V
	VCOM	-	-1	-	-5.5	V

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8.2 AC Characteristics

8.2.1 High Speed Mode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
UI instantaneous	UIINST	1	-	3	ns
T Data to Clock Skew	TSKEW	-0.15	-	0.15	UIHS
RX Data to Clock Setup Time Tolerance	TSETUP	0.15	-	-	UIHS
RX Data to Clock Hold Time Tolerance	THOLD	0.15	-	-	UIHS

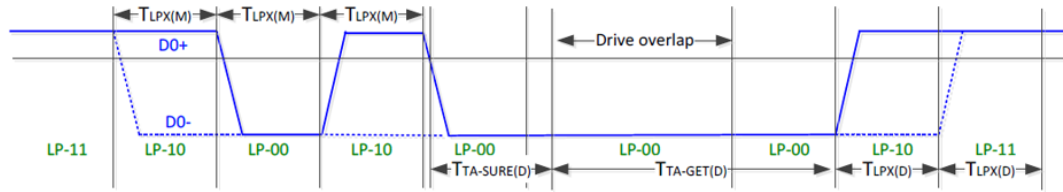


8.2.2 Low Power Mode Characteristics

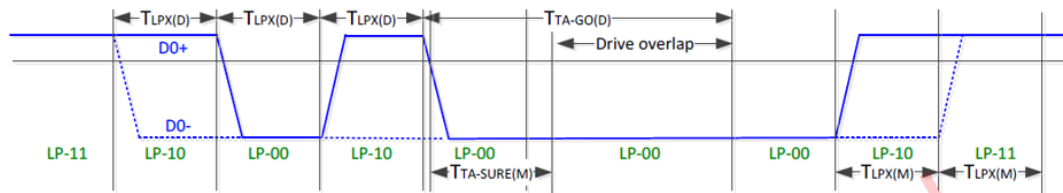
Parameter	Description	Min.	Typ.	Max.	Unit
$T_{LPX(M)}$	Transmitted length of any Low-Power state period (MCU to display module)	50	-	-	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period (display module to MCU)	50	-	-	ns
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state(LP-00) during a Link Turnaround	T_{LPX}	-	$2 * T_{LPX}$	
T_{TA-GET}	Time that the new transmitter drives the Bridge state(LP-00) after accepting control during a Link Turnaround	$5 * T_{LPX}$			
T_{TA-GO}	Time that the transmitter drives the Bridge state(LP-00) before releasing control during a Link Turnaround	$4 * T_{LPX}$			

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- Bus Turnaround from MPU to display module

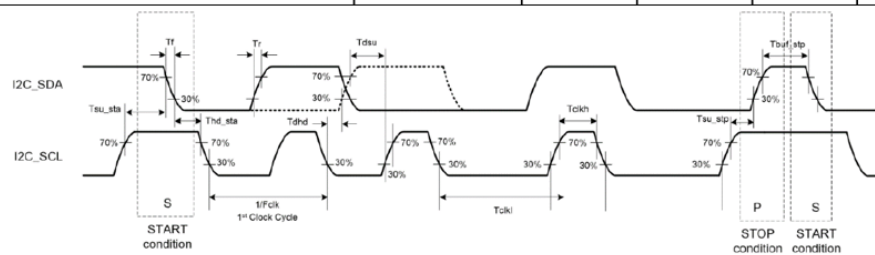


- Bus Turnaround from display module to MPU



8.2.3 I2C Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
I2C Clock Frequency	Fclk	-	-	400	kHz
I2C Clock Low	Tclk	1300	-	-	ns
I2C Clock High	Tclkh	600	-	-	ns
I2C Data Rising Time	Tdr	-	-	300	ns
I2C Data Falling Time	Tdr	-	-	300	ns
I2C Data Setup Time	Tdsu	100	-	-	ns
I2C Data Hold Time	Tdhd	-	-	TBD	ns
I2C Setup Time (Start Condition)	Tsu_sta	600	-	-	ns
I2C Hold Time (Start Condition)	Thd_sta	600	-	-	ns
I2C Setup Time (Stop Condition)	Tsu_stp	600	-	-	ns
I2C Bus Free Time (Stop Condition)	Tbutf_stp	1300	-	-	ns

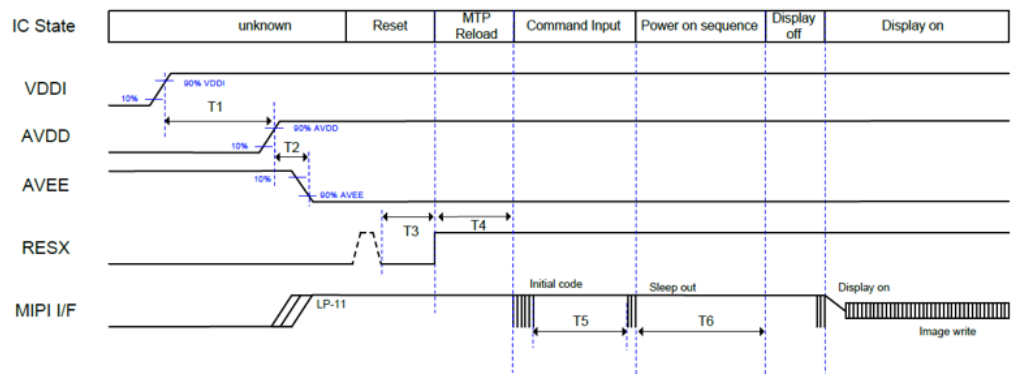


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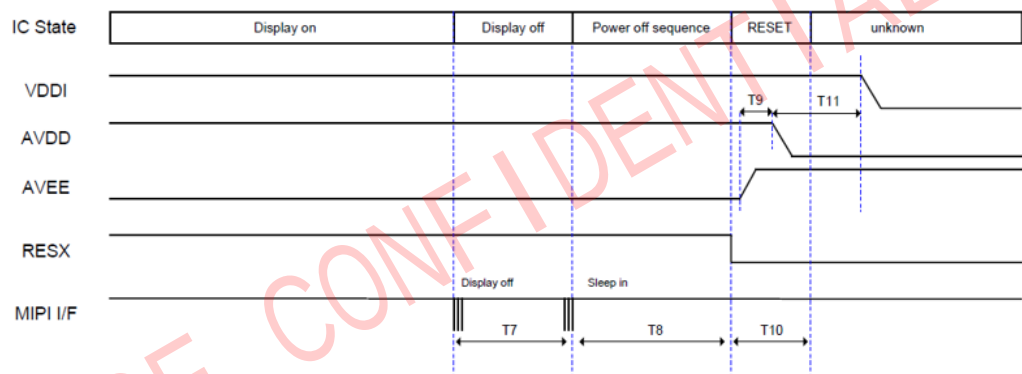
9. Power Supply Sequence

9.1 Power On/Off Sequence

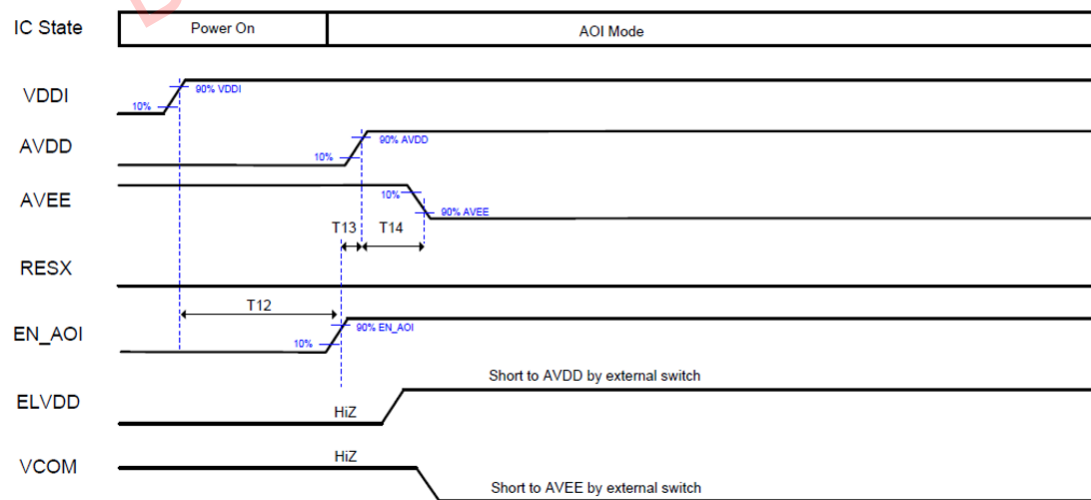
power on sequence



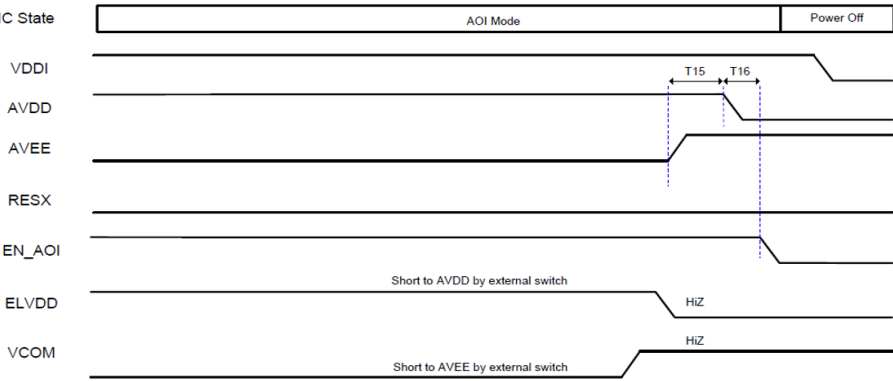
power off sequence



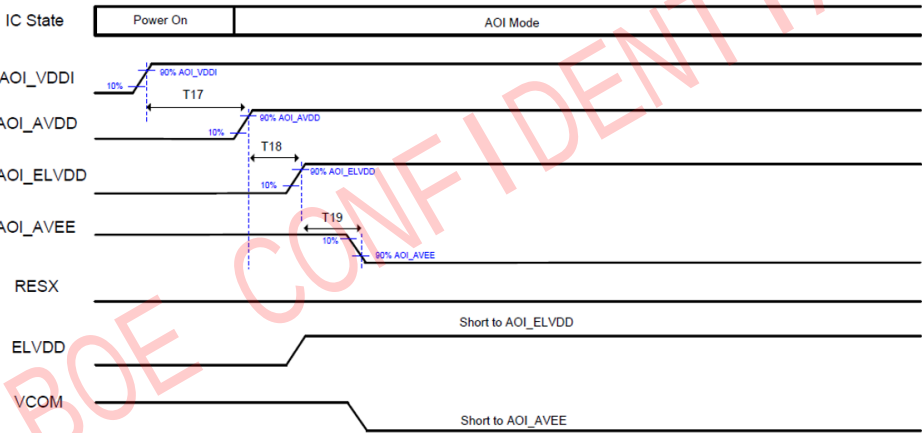
AOI model power on sequence



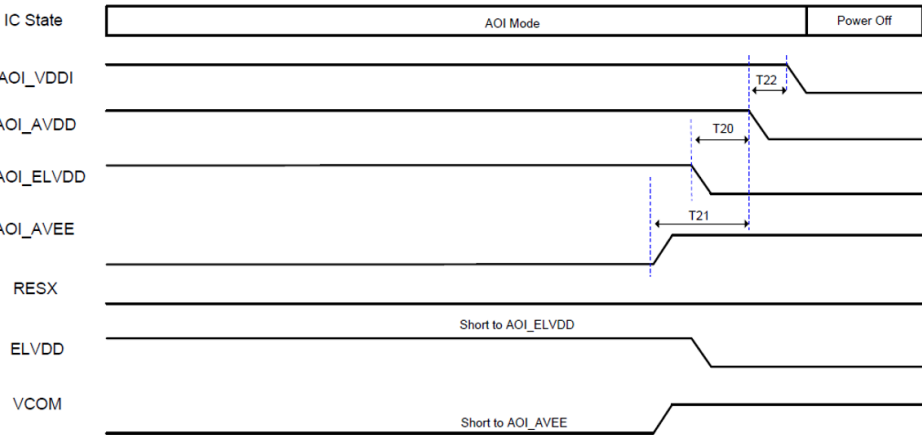
AOI mode1 power off sequence



AOI mode2 power on sequence



AOI mode2 power off sequence



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9.2 Power Supply Sequence

Symbol	Min.	Typ.	Max.	Unit	Description
T1	1	-	-	ms	Power on time between AVDD and VDDI
T2	1	-	-	ms	Power on time between AVDD and AVEE
T3	1	-	-	ms	Effective hardware reset period
T4	20	-	-	ms	MTP reload time
T5	0	-	-	ms	The time is between initial code finished and sleep-out command
T6	2	-	8	VS	Power on sequence, the period can be modified
T7	1	-	-	VS	Blanking region
T8	-	1	-	VS	Power off sequence, the period can be modified
T9	1	-	-	ms	Power off time between AVEE and AVDD
T10	1	-	-	ms	Effective hardware reset period
T11	1	-	-	ms	Power off time between AVEE and VDDI
T12	5	-	-	ms	Power on time between VDDI and EN_AOI in AOI mode1
T13	1	-	-	ms	Power on time between EN_AOI and AVDD in AOI mode1
T14	1	-	-	ms	Power on time between AVDD and AVEE in AOI mode1
T15	1	-	-	ms	Power off time between AVEE and AVDD in AOI mode1
T16	1	-	-	ms	Power off time between AVDD and EN_AOI in AOI mode1
T17	5	-	-	ms	Power on time between AOI_VDDI and AOI_AVDD in AOI mode2
T18	1	-	-	ms	Power on time between AOI_AVDD and AOI_ELVDD in AOI mode2
T19	1	-	-	ms	Power on time between AOI_ELVDD and AOI_AVEE in AOI mode2
T20	1	-	-	ms	Power off time between AOI_ELVDD and AOI_AVDD in AOI mode2
T21	1	-	-	ms	Power off time between AOI_AVEE and AOI_ELVDD in AOI mode2
T22	1	-	-	ms	Power off time between AOI_AVDD and AOI_VDDI in AOI mode2

10. Description of Function

10.1 Display Mode

10.1.1 Power Mode

ITEM	Code value
Sleep In	0x10
Sleep Out	0x11
Display On	0x29
Display Off	0x28

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10.1.2 Idle Mode

ITEM	Code value
Idle On	0x39(Default value)
Idle Off	0x38

10.1.3 BIST Mode

Register setting:

◆ BIST On/Off Control (C4h CMD2 Page1)

Instruction	R/W	Address name		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
BISTONOFF	R/W	C4h	C400h	-	1	0	1	0	0	1	0	1
			C401h	-	0	1	0	1	0	1	0	1
			C402h	-	-	-	-	-	-	-	-	BION1
			C403h	-	BION2	-	-	-	-	-	-	-
Description	This command is used to control BIST function (Free Run mode). BIST function enable step: 1. Enter Sleep-In(10h) mode and stop MIPI video data. 2. Setting PATENICYC[1:0] and BISTPATEN[11:0] to control the display cycle time and pattern. 3. Setting BION1="1" and BION2="1", the driver IC will start to run the BIST function. BIST function disable step: 1. Setting BION1="0" and BION2="0",the driver IC will return to normal function. 2. Sending MIPI video data and enter Sleep-Out(11h) mode for normal display.											
	Restriction	-										
Default												
	Status			Default Value								
	Power On Sequence			C400h				AAh				
				C401h				55h				
				C402h				00h				
C403h				00h								

◆ BIST CTRL (C5h CMD2 Page1)

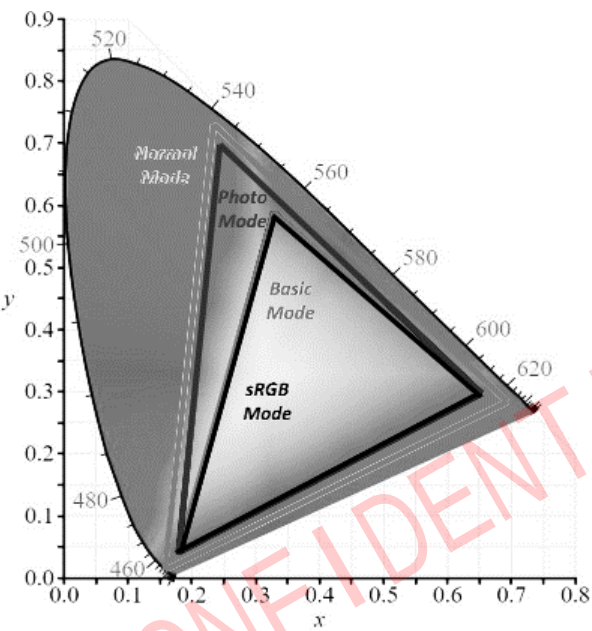
Instruction	R/W	Address name		Parameter																																		
		MIPI	I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0																										
BISTSET	R/W	C5h	C500h	-	0	0	PATENICYC[1:0]		BISTPATEN[11:8]																													
			C501h	-	BISTPATEN[7:0]																																	
			C502h	-	GRAY_LEVEL[7:0]																																	
Description	This command is used to set the display pattern in BIST function. PATENICYC[1:0] : Cycle time between each display pattern.																																					
	<table><tr><th>PATENICYC[1:0]</th><th>Pattern cycle time</th></tr><tr><td>0h</td><td>256 Frame</td></tr><tr><td>1h</td><td>512 Frame</td></tr><tr><td>2h</td><td>1024 Frame</td></tr><tr><td>3h</td><td>2048 Frame</td></tr></table>												PATENICYC[1:0]	Pattern cycle time	0h	256 Frame	1h	512 Frame	2h	1024 Frame	3h	2048 Frame																
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	1h	512 Frame																																				
	2h	1024 Frame																																				
	3h	2048 Frame																																				
	BISTPATEN[11:0] : Select the display pattern in BIST function.																																					
	<table><tr><th>BISTPATEN[9:0]</th><th>Description</th></tr><tr><td>BISTPATEN[0]</td><td>Red pattern.</td></tr><tr><td>BISTPATEN[1]</td><td>Green pattern.</td></tr><tr><td>BISTPATEN[2]</td><td>Blue pattern.</td></tr><tr><td>BISTPATEN[3]</td><td>Black pattern.</td></tr><tr><td>BISTPATEN[4]</td><td>Gray Level pattern. (Set by BIST_GRAY_LEVEL[7:0])</td></tr><tr><td>BISTPATEN[5]</td><td>Vertical Gradation pattern.</td></tr><tr><td>BISTPATEN[6]</td><td>Horizontal Gradation pattern.</td></tr><tr><td>BISTPATEN[7]</td><td>Color Bar pattern.</td></tr><tr><td>BISTPATEN[8]</td><td>Crosstalk with boundary pattern.</td></tr><tr><td>BISTPATEN[9]</td><td>Source CP Pattern</td></tr><tr><td>BISTPATEN[10]</td><td>Gamma CP Pattern</td></tr><tr><td>BISTPATEN[11]</td><td>Reserved</td></tr></table>												BISTPATEN[9:0]	Description	BISTPATEN[0]	Red pattern.	BISTPATEN[1]	Green pattern.	BISTPATEN[2]	Blue pattern.	BISTPATEN[3]	Black pattern.	BISTPATEN[4]	Gray Level pattern. (Set by BIST_GRAY_LEVEL[7:0])	BISTPATEN[5]	Vertical Gradation pattern.	BISTPATEN[6]	Horizontal Gradation pattern.	BISTPATEN[7]	Color Bar pattern.	BISTPATEN[8]	Crosstalk with boundary pattern.	BISTPATEN[9]	Source CP Pattern	BISTPATEN[10]	Gamma CP Pattern	BISTPATEN[11]	Reserved
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	BISTPATEN[4]	Gray Level pattern. (Set by BIST_GRAY_LEVEL[7:0])																																				
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BISTPATEN[11]	Reserved																																					
Note1: the patterns which the bit number of BISTPATEN[9:0] is set to “1” will display and change automatically. Note2: When BISTPATEN[11:0]=12'h000, display pattern will be black pattern.																																						
GRAY_LEVEL[7:0] : Set the gray level when BISTPATEN[4]=”1” in BIST function.																																						
<table><tr><th>GRAY_LEVEL[7:0]</th><th>Description</th></tr><tr><td>0h</td><td>Gray Level : 00h</td></tr><tr><td>1h</td><td>Gray Level : 01h</td></tr><tr><td>2h</td><td>Gray Level : 02h</td></tr><tr><td>:</td><td>:</td></tr><tr><td>FDh</td><td>Gray Level : FDh</td></tr><tr><td>FEh</td><td>Gray Level : FEh</td></tr><tr><td>FFh</td><td>Gray Level : FFh</td></tr></table>												GRAY_LEVEL[7:0]	Description	0h	Gray Level : 00h	1h	Gray Level : 01h	2h	Gray Level : 02h	:	:	FDh	Gray Level : FDh	FEh	Gray Level : FEh	FFh	Gray Level : FFh											
GRAY_LEVEL[7:0]	Description																																					
0h	Gray Level : 00h																																					
1h	Gray Level : 01h																																					
2h	Gray Level : 02h																																					
:	:																																					
FDh	Gray Level : FDh																																					
FEh	Gray Level : FEh																																					
FFh	Gray Level : FFh																																					
Restriction	-																																					
Default	<table><tr><th>Status</th><th colspan="2">Default Value</th></tr><tr><td rowspan="3">Power On Sequence</td><td>C500h</td><td>01h</td></tr><tr><td>C501h</td><td>FFh</td></tr><tr><td>C502h</td><td>FFh</td></tr></table>												Status	Default Value		Power On Sequence	C500h	01h	C501h	FFh	C502h	FFh																
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	Power On Sequence	C500h	01h																																			
		C501h	FFh																																			
C502h		FFh																																				

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10.2 Image Enhancement

10.2.1 Gamut Mapping—Selectable Color Mode with Different Gamut

◆ 0.39" Micro OLED support Normal Mode/Photo Mode/ Basic Mode(sRGB Mode).



◆ Register Setting
Gamut mapping (57 CMD1).

5700H	GAMUT											
Instruction	R/W	Address name		Parameter								
		MIPI	I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
GAMUT	R/W	57h	5700h	-	-	-	-	-	-	-	GAMUT_SEL [1:0]	
Description	This command sets the control of gamut mapping.											
	Bit	Symbol		Description				Comment				
	2bit	GAMUT_SEL[1:0]		Gamut mapping control				0h= Gamut mapping 0 —Normal Mode 1h= Gamut mapping 1—Photo Mode 2h= Gamut mapping 2—Basic Mode				
Restriction	-											
Default	Status			Default Value								
	Power On Sequence			5700h					00h			

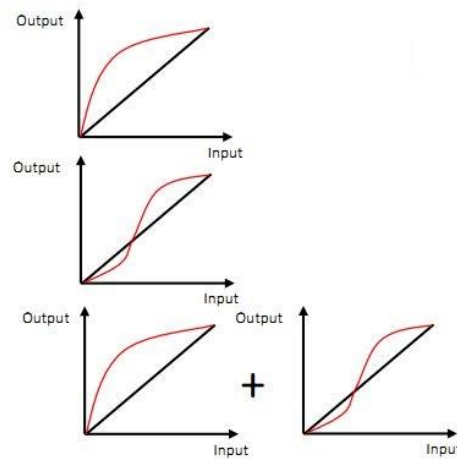
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10.2.2 Contrast/Edge Enhancement

Contrast Enhancement:

- ◆ Adaptive curve for indoor and outdoor environment

In order to increase the readable, we need trade-off between brightness and contrast ratio.



Adaptive curve of contrast

- ◆ 2D Edge enhancement

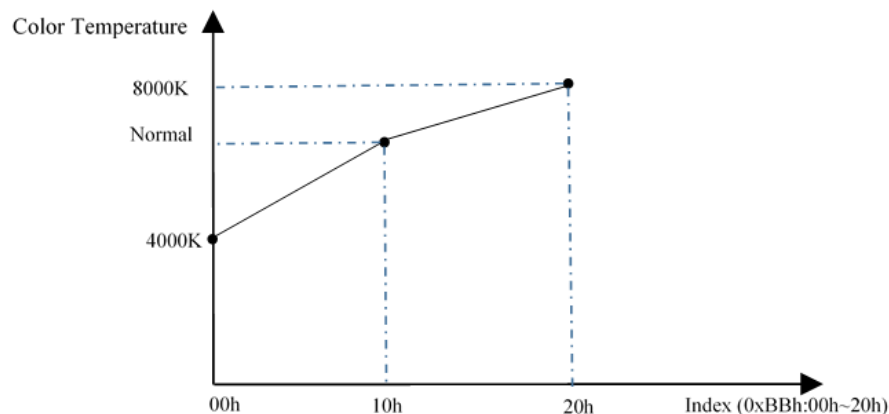
The 0.39"Micro OLED support a better display effect by the "2D Edge enhancement", such as increasing the image sharpness, Jagger, Overshooting and Noise Depression.

10.2.3 High Brightness or High Contrast Mode

High Brightness for AR Application, High Contrast for VR Application. This function adjusts the display mode according to the register "53h".

10.3 Color Temperature Function (Auto White Balance Control)

This function adjusts the R/G/B gamma parameter according to the register BBh setting to adjust the White balance and change the color temperature at the same time.



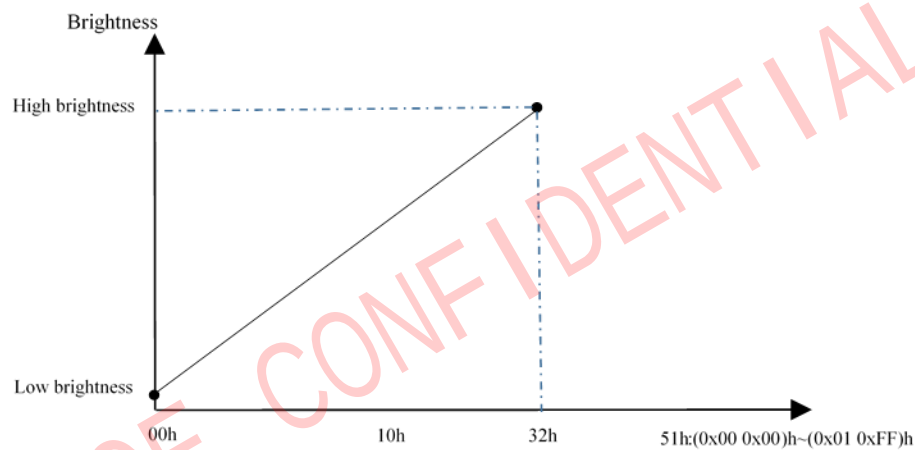
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◆ Register setting

ITEM	Address name	Code value	Default value
Color Temperature	0xBBh CMD Page1	00h~20h	10h

10.4 Brightness Control(BC) Functions

This function adjusts the gamma parameter according to the register 51h and 53h setting to adjust the luminance.



◆ Register setting

White Display Brightness(51h CMD1).

5100H	WRDISBV											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
WRDISBV	W	51h	5100h	-	DBV[7:0]							
			5101h	-	-	-	-	-	-	-	-	DBV [8]
Description	This command is used to adjust brightness.											
Restriction	-											
Default		Status		Default Value								
		Power On Sequence		5100h				00h				
				5101h				00h				

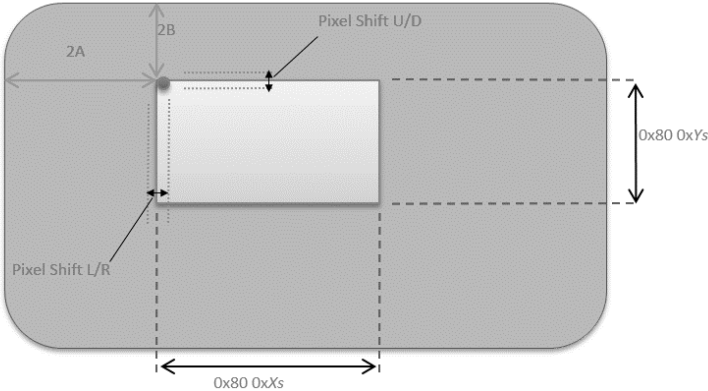
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White CTRL Display (53h CMD1)

5300H	WRCTRLD											
Instruction	R/W	Address		Parameter								
		MIPI	I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
WRCTRLD	W	53h	5300h	-	-	-	BCTRL L	-	DD_ BC	-	-	HBHC _SEL
Description	This command is used to set brightness control and display diming control.											
	Bit	Symbol		Description				Comment				
	D5	BCTRL		Brightness control				1= Brightness control enable 0= Brightness control disable				
	D3	DD_BC		Display dimming control				1= Display dimming control enable 0= Display dimming control disable				
	D0	HBHC_SEL		Display mode control				0=High Brightness Low Contrast 1=Low Brightness High Contrast				
Restriction												
Default	Status			Default Value								
	Power On Sequence			5300h					00h			

10.5 Display Active-Area(AA) Control

ITEM	Description	Code 值
Resolution	X-direction: Support 8N, N=40~240 Y-direction: support 8M, M=30~135	CMD1: 0x80(NC[7:0] NL[7:0])
Active-Area(AA) control	Display start pointer	Xs: CMD1: 0x2A Ys: CMD1: 0x2B
	Pixel shift: $\pm 12\text{pixel}/\text{step}=4\text{pixel}$	CMD2 Page0: 0xB4



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10.6 Auto Temperature Compensation Function

Brightness and white point of OLED depends on display panel temperature as show in below. This module integrates Brightness and white point compensation function against panel temperature variation. This function allows to sustain relatively constant luminance and white point even if panel temperature changing as shown in below.

◆ Register Settings

2300H	ALLPON											
Instruction	R/W	Address name		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
ALLPON	R/W	25h	2500h	-	-	-	-	-	-	-	-	TC_ENABLE
Description	This command is used to turn on temperature sensor.											
Restriction	-											
Default	Status			Default Value								
	Power On Sequence			2500h				00h				

11. Optical Characteristics

11.1 Optical Characteristics

Item		0.39 Micro OLED SPEC	
White Brightness	Center	1500 cd/m²	
White Uniformity 9 point	White (255)	>90%	
	White (128)	>90%	
	White (64)	>90%	
View Angle (White)	Lum. Decay (50%)	-55°~55°	
	Color Shift ($\Delta u'v' < 0.025$)	-45°~45°	
Contrast	CR	>10000:1	
Color Coordinate	Red	CIE-x	0.64±0.03
		CIE-y	0.33±0.03
	Green	CIE-x	0.26±0.03
		CIE-y	0.67±0.03
	Blue	CIE-x	0.15±0.03
		CIE-y	0.07±0.03
	White	CIE-x	0.31±0.03
		CIE-y	0.31±0.03
Color Gamut (NTSC)		>80%	
Color Temperature		>6000K	

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11.2 Measurement System • Measurement Method

The luminance and chromaticity are measured in Measurement System A shown below.

Measurement temperature: $T_{pnl} = 30^{\circ}\text{C}$

Measurement point: One point on the screen center

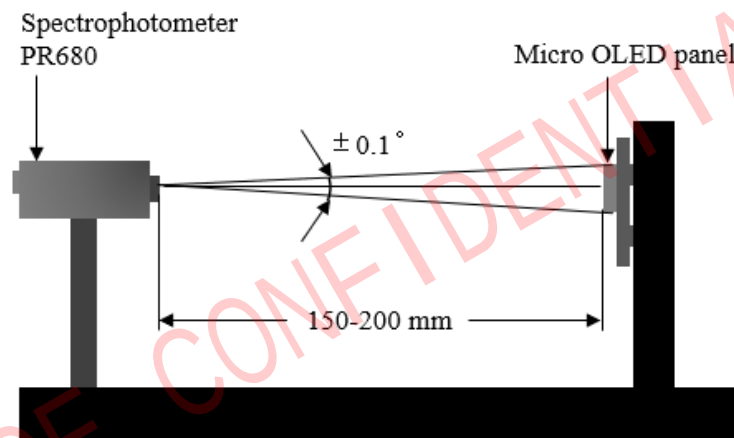
All white display: All RGB signal data is set to High.

All black display: All RGB signal data is set to Low.

Luminance and chromaticity: Measure the luminance and chromaticity in all white display in Measurement System A.

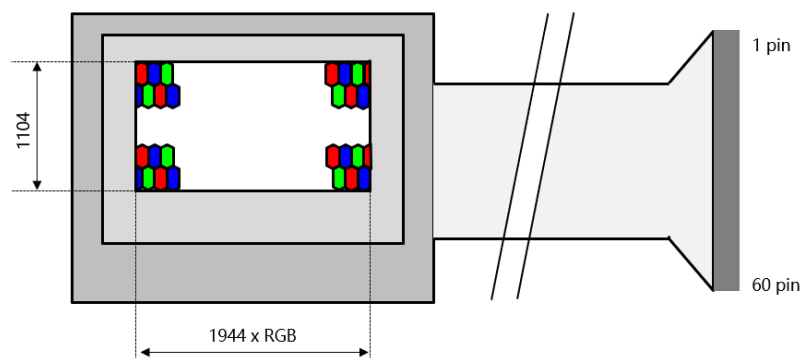
Contrast: Measure the luminance in all white display (@ : 500cd/m^2) and all black display in Measurement System A, and substitute them into the formula below.

Contrast = Luminance in all white display / Luminance in all black display



Measurement System

12. Pixel Alignment



※Including orbit margin

13. Package Outline

Figure 1: Dimensions of the device. The figure consists of four sub-diagrams showing different views of a rectangular device with a connector.

- Top-left diagram:** Front view showing dimensions: 8.7495, 3.9108±0.05, 9.5±0.1, 45.02±0.1, and 6.4±0.05. The "Active Area" is indicated.
- Top-right diagram:** Side view showing dimensions: 0.5±0.05, 1.35 Max, 0.15±0.05, 0.2±0.05, 1.83, 1.32, 1.5±0.15, and Thickness of connector.
- Bottom-right diagram:** Top view showing the connector area with two rows of pins. The label "Connector" is present.
- Bottom-left diagram:** Enlarged view of the connector showing dimensions: 1.3, 0.9, 0.23, 0.17, 0.4, 0.8, 6.4, 11.83, 18, and pin labels PIN_31, PIN_60, PIN_1, and PIN_30.

Connector(enlarged)

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14. Notes on Handling

14.1 Static charge prevention

Be sure to take the following protective measures. Organic EL panels are easily damaged by static charges.

- (1) Use non-chargeable gloves or handle with bare hands.
- (2) Use a wrist strap connecting ground when handling.
- (3) Do not touch any electrodes on the panel.
- (4) Wear non-chargeable clothes and conductive shoes.
- (5) Install grounded conductive mats on the working floor and working table.
- (6) Keep the panel away from any charged materials.

14.2 Protection from dust and dirt

- (7) Operate in a clean environment.
- (8) Do not touch the panel surface. The surface is easily scratched.

When cleaning on panel surface, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.

- (9) Use ionized air to blow dust off the panel surface.

14.3 Others

- (10) Not hold FPC (Flexible Printed Circuit) , not twist the FPC, not bend FPC because connection area between the FPC and panel is easily broken by mechanical stress.
- (11) The minimum fold radius of the FPC is 1.0 mm, So, do not fold the FPC less than 1.0mm radius.
- (12) Do not drop the module.
- (13) Do not twist or bend the module .
- (14) Keep the module away from heat sources.
- (15) Not be close the module to water or other solvents.
- (16) Do not store or use the module at high temperatures or high humidity circumstance, as the circumstance may affect module specifications.
- (17) When disposing of this, regard it as industrial waste and please comply with related regulations.
- (18) Do not store or use the panel in reactive chemical substance (including alcohol) environments, as these may affect the specifications.