



# LCD MODULE SPECIFICATION

**MODEL NO.**

**BO12864E2 series**

**VER01**

FOR MESSRS:

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ON DATE OF:

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APPROVED BY:

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## 1. Numbering System

<b>B</b>	<b>Q</b>	<b>12864</b>	<b>E2</b>	<b>-</b>	<b>-</b>	<b>-</b>	<b>-</b>	<b>-</b>	<b>xxx</b>
<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>	<b>7</b>	<b>8</b>	<b>9</b>

<b>0</b>	Brand	Bolymin
<b>1</b>	Module Type	C= character type G= graphic type P= TAB/TCP type O= COG type F= COF type
<b>2</b>	Format	2002=20 characters, 4 lines 12232= 122 x 32 dots
<b>3</b>	Version No.	A type
<b>4</b>	LCD Color	G=STN/gray Y=STN/yellow-green C=color STN B=STN/blue F=FSTN T=TN
<b>5</b>	LCD Type	R=positive/reflective P=positive/transflective M=positive/transmissive N=negative/transmissive
<b>6</b>	Backlight type/color	L=LED array/ yellow-green H=LED edge/white R=LED array/red G=LED edge/yellow-green D=LED edge/blue E=EL/white B=EL/blue C=CCFL/white
<b>7</b>	CGRAM Font	J=English/Japanese Font E=English/European Font C=English/Cyrillic Font H=English/Hebrew Font
<b>8</b>	View Angle/ Operating Temperature	B=Bottom/Normal Temperature H=Bottom/Wide Temperature U=Bottom/Ultra wide Temperature T=Top/Normal Temperature W=Top/Wide Temperature C=9H/Normal Temperature
<b>9</b>	Special Code	3=3 volt logic supply n=negative voltage LCD c=cable/connector xxx=to be assigned on data sheet t=temperature compensation for LCD p=touch panel



## 2. Precaution in use of LCD Module

1. To avoid applying excessive shocks to the module or making any alterations or modifications to it.
2. Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
3. Don't disassemble the LCM.
4. Don't operate it above the absolute maximum rating.
5. Don't drop, bend or twist LCM.
6. Soldering: only to the I/O terminals.
7. Storage: please storage in anti-static electricity container and clean environment.
8. Don't touch the elastmer connector, especially insert a backlight panel (EL or CCFL)

## 3. General Features

This BO12864E2 is a dot matrix graphic LCD module fabricated by low power COMS technology, interfaced with 8 –bit MPU.

### **Features**

- Display format: 128dots\* 64dots
- FSTN transflective mode
- Easy interface with 8-bit MPU
- Low power consumption
- Transflective (low)light method
- Viewing angle:6 o'clock
- Multiplex level: 1/64duty, 1/9bias
- LCD driver IC :ST7565V
- Connector: COG+FPC
- Power supply:2.7~3.3V
- Backlight: LED edge /( option YG, white, Amber, Blue)



#### 4. Mechanical Specifications

Item	Dimension	Unit
Module Size(W*H*T)	80.0X54.0X9.7(LED b/l)	mm
Viewing Area (W*H)	70.7*38.8	mm
Dot Pitch (W*H)	0.52*0.52	mm
Dot Size (W*H)	0.48*0.48	mm
Active Area (W*H)	66.52*33.24	mm
Number of Dots	128*64	mm

#### 5. Temperature Characteristics

Parameter	Symbol	Rating	Unit
Operating	Top	-20-70	°C
Storage temperature	Tst	-30-80	°C

#### 6. Electro-Optical characteristics

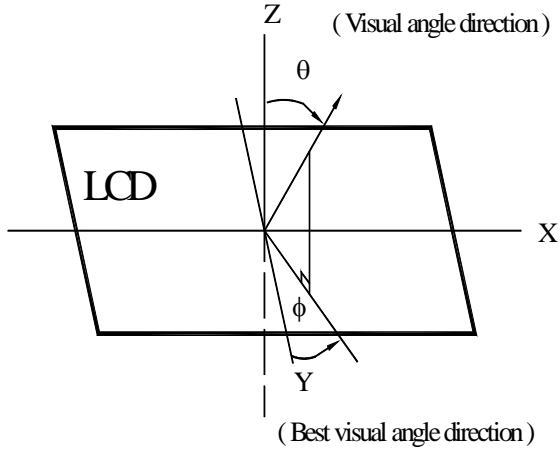
FSTN Type

Item	Sym	Condition	Min.	Typ.	Max.	Unit
Contrast	CR	$\theta=0^\circ$ $\Phi=0^\circ$	5 : 1	—	—	deg.
Viewing Angle	$\theta$	K=5 $\Phi=0^\circ$	$\theta_2 - \theta_1=40$	—	—	deg.
		K=5 $\theta=10^\circ$	$\Phi=\pm 40$	—	—	deg.
Response time	T <sub>on</sub>	25°C	—	200	350	ms
	T <sub>off</sub>	25°C	—	200	350	ms

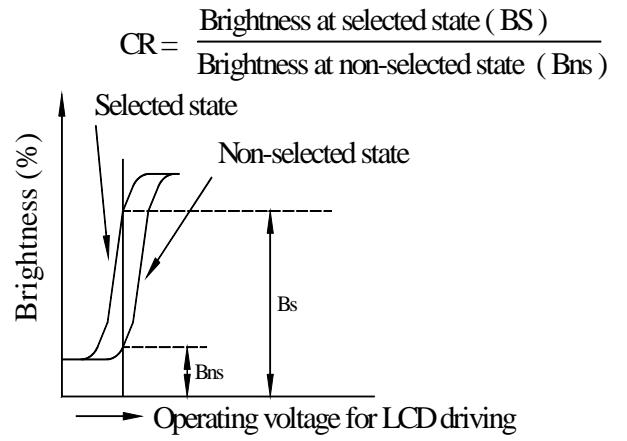


6.1 Definitions

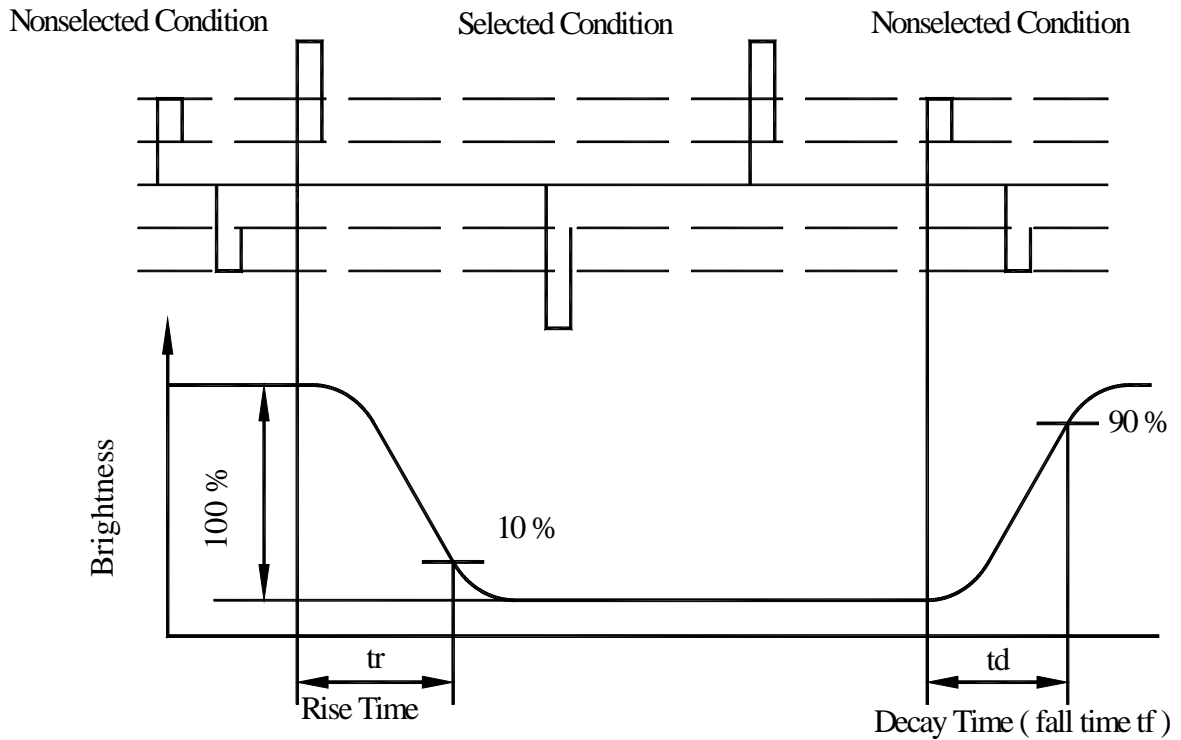
■ View Angles



■ Contrast Ratio



■ Response time





## 7. Interface Pin Function

Pin No.	Symbol	Level	Description
1	/CS1	I	This is the chip select signal
2	/RES	I	When /RES is set to "L," the settings are initialized. The reset operation is performed by the /RES signal level.
3	A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
4	/WR (R/W)	I	<ul style="list-style-type: none"> <li>When connected to an 8080 MPU, this is active LOW.</li> </ul> (R/W) This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. <ul style="list-style-type: none"> <li>When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/W = "H": Read. When R/W = "L": Write</li> </ul>
5	/RD(E)	I	<ul style="list-style-type: none"> <li>When connected to an 8080 MPU, this is active LOW.</li> </ul> (E) This pin is connected to the /RD signal of the 8080 MPU, and the ST7565S series data bus is in an output status when this signal is "L". <ul style="list-style-type: none"> <li>When connected to a 6800 Series MPU, this is active HIGH. This is the 6800 Series MPU enable clock input terminal.</li> </ul>
6~13	D0~D5 D6(SCL) D7(SI)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = "L") : D7 : serial data input (SI) ; D6 : the serial clock input (SCL). D0 to D5 are set to high impedance. When the chip select is not active, D0 to D7 are set to high impedance.
14	Vdd	3.3V	Power supply for logic
15	VSS	0V	Power supply for logic GND
16	VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS
17	CAP5-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal
18	CAP3-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal
19	CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal
20	CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal
21	CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal
22	CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal
23	CAP4-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal
24	VRS	Power supply	This is the internal-output VREG power supply for the LCD power supply voltage regulator





25~29	V1~V5	Power supply	<p>This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divider or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below.  <math>VDD (= V0) \geq V1 \geq V2 \geq V3 \geq V4 \geq V5</math>                  When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command .</p>					
				1/65 DUTY	1/49 DUTY	1/33 DUTY	1/55 DUTY	1/53 DUTY
			V1	$1/9 * V5, 1/7 * V5$	$1/8 * V5, 1/6 * V5$	$1/6 * V5, 1/5 * V5$	$1/8 * V5, 1/6 * V5$	$1/8 * V5, 1/6 * V5$
			V2	$2/9 * V5, 2/7 * V5$	$2/8 * V5, 2/6 * V5$	$2/6 * V5, 2/5 * V5$	$2/8 * V5, 2/6 * V5$	$2/8 * V5, 2/6 * V5$
			V3	$7/9 * V5, 5/7 * V5$	$6/8 * V5, 4/6 * V5$	$4/6 * V5, 3/5 * V5$	$6/8 * V5, 4/6 * V5$	$6/8 * V5, 4/6 * V5$
			V4	$8/9 * V5, 6/7 * V5$	$7/8 * V5, 5/6 * V5$	$5/6 * V5, 4/5 * V5$	$7/8 * V5, 5/6 * V5$	$7/8 * V5, 5/6 * V5$
30	VR	I	<p>Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divider.                  IRS = "L" : the V5 voltage regulator internal resistors are not used .                  IRS = "H" : the V5 voltage regulator internal resistors are used</p>					
31	C86	I	<p>This is the MPU interface switch terminal.                  C86 = "H": 6800 Series MPU interface.                  C86 = "L": 8080 MPU interface.</p>					
32	P/S	I	<p>This is the parallel data input/serial data input switch terminal.                  P/S = "H": Parallel data input.                  P/S = "L": Serial data input.                  The following applies depending on the P/S status:</p>					
			P/S	Data/Command	Data	Read/Write	Serial Clock	
			"H"	A0	D0 to D7	/RD, /WR	X	
			"L"	A0	SI (D7)	Write only	SCL (D6)	
<p>When P/S = "L", D0 to D5 fixed "H".                  /RD (E) and /WR (R/W) are fixed to either "H" or "L".                  With serial data input, It is impossible read data from RAM.</p>								
33	/HPM	I	<p>This is the power control terminal for the power supply circuit for liquid crystal drive.                  /HPM = "H": Normal mode                  /HPM = "L": High power mode</p>					
34	IRS	I	<p>This terminal selects the resistors for the V5 voltage level adjustment.                  IRS = "H": Use the internal resistors                  IRS = "L": Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.</p>					



## 8. Backlight information

### 8.1. edge LED/yellow-green

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Current	I <sub>LED</sub>	—	80		mA	V=4.2V
Supply Voltage	V	—	4.2	4.4	V	
Reverse Voltage	V <sub>R</sub>	—	—	8	V	
Luminous Intensity	I <sub>V</sub>	2.5	—	—	cd/m <sup>2</sup>	I <sub>LED</sub> =80mA
Wave Length	λ <sub>p</sub>		574		nm	I <sub>LED</sub> =80mA
Life Time		—	100000	—	Hr.	V ≤ 4.2V
Color	Yellow Green					

### 8.2. edge LED/White

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Current	I <sub>LED</sub>	—	80		mA	V=3.0V
Supply Voltage	V	—	3.0	3.2	V	
Reverse Voltage	V <sub>R</sub>	—	—	6	V	
Luminous Intensity	I <sub>V</sub>	30	—	—	cd/m <sup>2</sup>	I <sub>LED</sub> =80mA
Wave Length	λ <sub>p</sub>				nm	I <sub>LED</sub> =80mA
Life Time		—	20000	—	Hr.	V ≤ 3.2V
Color	White					



## 8.2. edge LED/Blue

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Current	I <sub>LED</sub>	—	80		mA	V=3.0V
Supply Voltage	V	—	3.0	3.2	V	
Reverse Voltage	V <sub>R</sub>	—	—	6	V	
Luminous Intensity	I <sub>V</sub>	15	—	—	cd/m <sup>2</sup>	I <sub>LED</sub> =80mA
Wave Length	λ <sub>p</sub>				nm	I <sub>LED</sub> =80mA
Life Time		—	50000	—	Hr.	V ≤ 3.2V
Color	Blue					



9. Quality Assurance

◆ Screen Cosmetic Criteria

No.	Defect	Judgement Criterion	Partition																				
1	Spots	<p>A) Clear</p> <table border="1"> <thead> <tr> <th>Size:d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.1</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.1 &lt; d \leq 0.2</math></td> <td>6</td> </tr> <tr> <td><math>0.2 &lt; d \leq 0.3</math></td> <td>2</td> </tr> <tr> <td><math>0.3 &lt; d</math></td> <td>0</td> </tr> </tbody> </table> <p>Note: Including pin holes and defective dots which must be within one pixel size.</p> <p>B) Unclear</p> <table border="1"> <thead> <tr> <th>Size:d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.2</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.2 &lt; d \leq 0.5</math></td> <td>6</td> </tr> <tr> <td><math>0.5 &lt; d \leq 0.7</math></td> <td>2</td> </tr> <tr> <td><math>0.7 &lt; d</math></td> <td>0</td> </tr> </tbody> </table>	Size:d mm	Acceptable Qty in active area	$d \leq 0.1$	Disregard	$0.1 < d \leq 0.2$	6	$0.2 < d \leq 0.3$	2	$0.3 < d$	0	Size:d mm	Acceptable Qty in active area	$d \leq 0.2$	Disregard	$0.2 < d \leq 0.5$	6	$0.5 < d \leq 0.7$	2	$0.7 < d$	0	Minor
Size:d mm	Acceptable Qty in active area																						
$d \leq 0.1$	Disregard																						
$0.1 < d \leq 0.2$	6																						
$0.2 < d \leq 0.3$	2																						
$0.3 < d$	0																						
Size:d mm	Acceptable Qty in active area																						
$d \leq 0.2$	Disregard																						
$0.2 < d \leq 0.5$	6																						
$0.5 < d \leq 0.7$	2																						
$0.7 < d$	0																						
2	Bubbles in Polarizer	<table border="1"> <thead> <tr> <th>Size:d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.3</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.3 &lt; d \leq 1.0</math></td> <td>3</td> </tr> <tr> <td><math>1.0 &lt; d \leq 1.5</math></td> <td>1</td> </tr> <tr> <td><math>1.5 &lt; d</math></td> <td>0</td> </tr> </tbody> </table>	Size:d mm	Acceptable Qty in active area	$d \leq 0.3$	Disregard	$0.3 < d \leq 1.0$	3	$1.0 < d \leq 1.5$	1	$1.5 < d$	0	Minor										
Size:d mm	Acceptable Qty in active area																						
$d \leq 0.3$	Disregard																						
$0.3 < d \leq 1.0$	3																						
$1.0 < d \leq 1.5$	1																						
$1.5 < d$	0																						
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor																				
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor																				
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor																				



## 10. Reliability

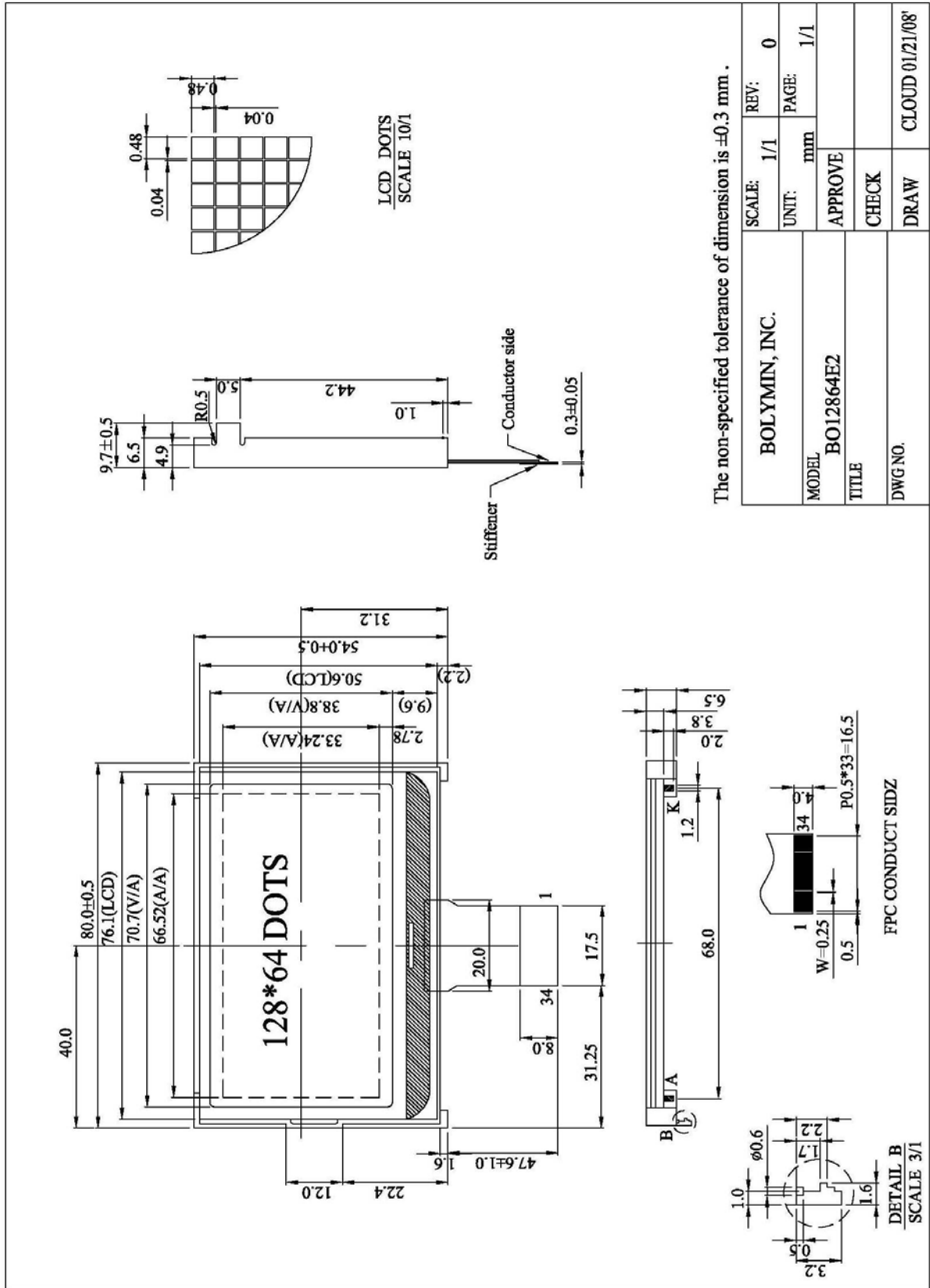
### ■ Content of Reliability Test

Environmental Test				
No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High Temperature storage	Endurance test applying the high storage temperature for a long time.	70°C 200hrs	—
2	Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30°C 200hrs	—
3	High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	60°C 200hrs	—
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	—
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60°C, 90%RH 96hrs	—
6	High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40°C, 90%RH 96hrs	—
7	Temperature Cycle	Endurance test applying the low and high temperature cycle. $\begin{array}{c} \leftarrow -10^{\circ}\text{C} \quad 25^{\circ}\text{C} \quad 60^{\circ}\text{C} \rightarrow \\ \hline 30\text{min} \quad 5\text{min} \quad 30\text{min} \\ \hline 1 \text{ cycle} \end{array}$	-10°C/60°C 10 cycles	—
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	—
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msdc 3 times of each direction	—
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	—
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V, RS=1.5kΩ CS=100pF 1 time	—

\*\*\*Supply voltage for logic system=5V. Supply vo

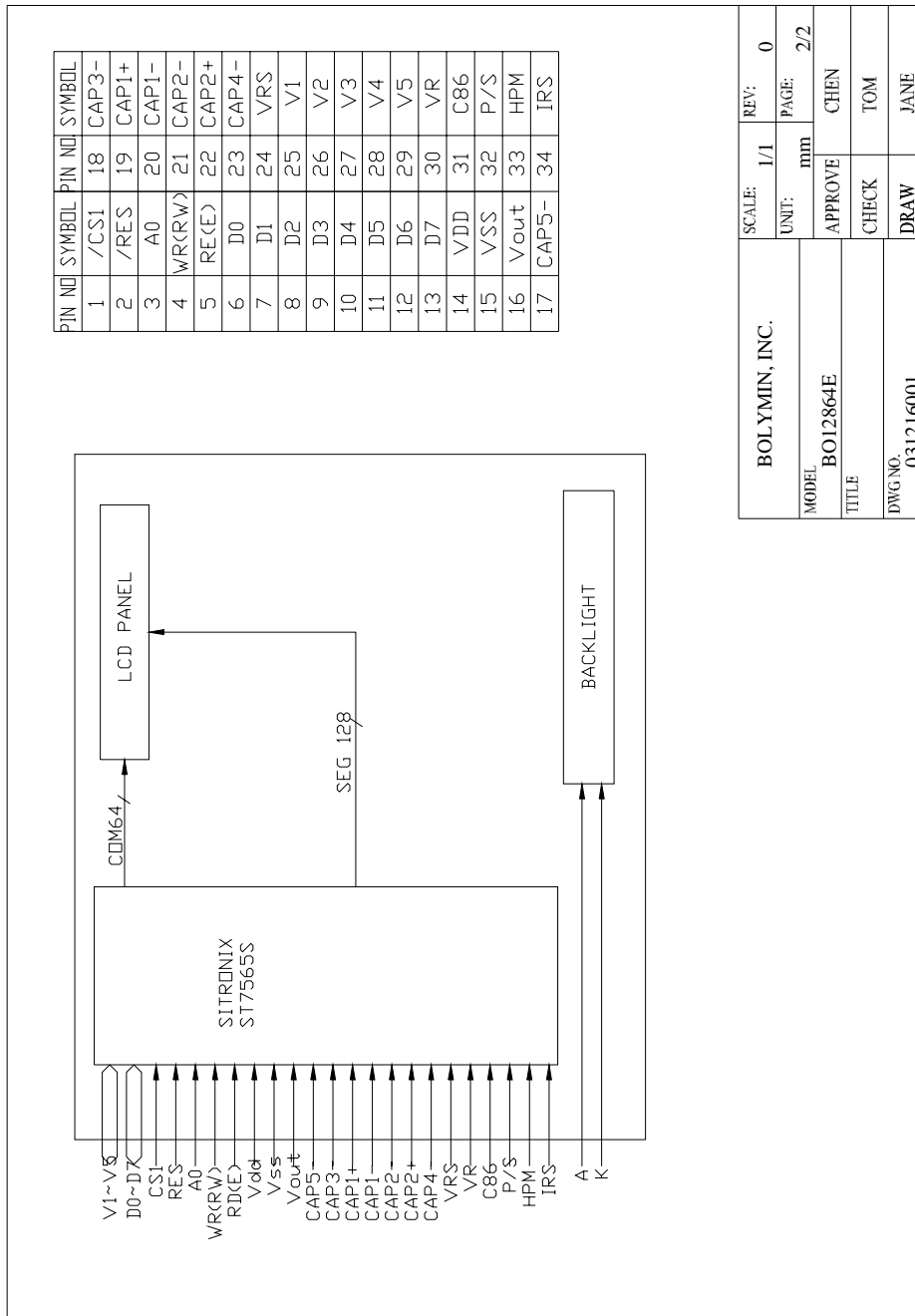


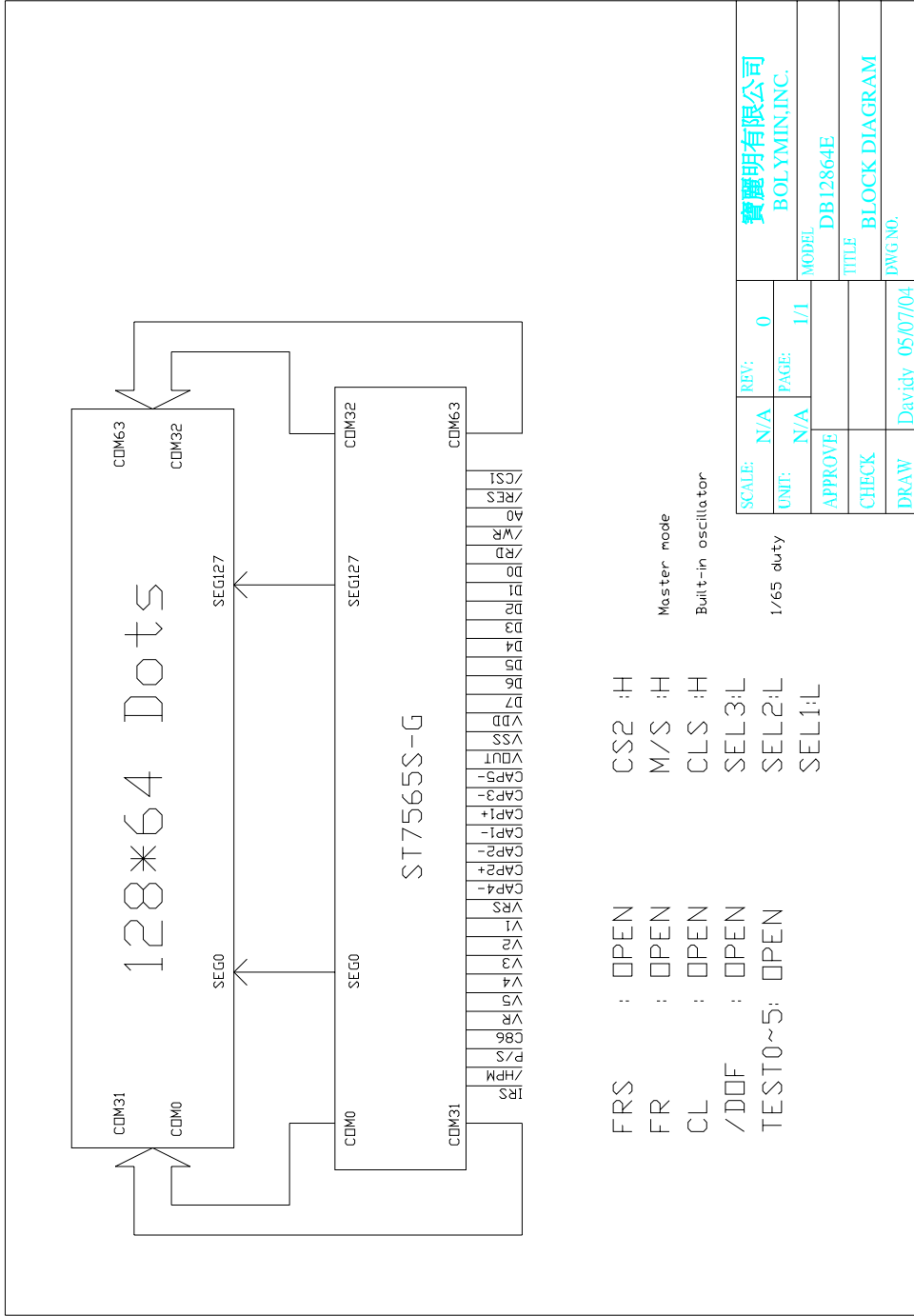
11.1 Outline Dimension





## 11.1.2 Block diagram





11.2 ST7565 controller spec.