Ver 1.1

In-System Programmable Configuration PROMs

Datasheet

Part Number：BQ18V04

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Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2017.6		Initial release.	
1.1	2018.3		Update format	

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1. Features

- In-system programmable 3.3V 4-megabit FLASH-based PROMs
  - Applicable for configuration of The BMTI of Aerospace and Xilinx Inc FPGAs
  - Data retention time: 20 years
  - Endurance of 2,000 program/erase cycles over full military temperature range
- Reliability
  - Temperature range：-55℃ ~ +125℃
  - Antistatic ability(human boby model)：2000V
  - Class B of GJB597A and GJB548A-96
  - IEEE Std 1149.1 boundary-scan (JTAG) support
  - JTAG command initiation of standard FPGA configuration
- Multiple configuration modes
  - Serial Slow/Fast configuration (up to 33 MHz)
  - 5V tolerant I/O pins accept 3.3V signals
  - Design support using the Xilinx Alliance™ and Foundation™ series software packages
  - Available in CLCC44 and CQFP44 packages
- Compatibility of BQ18V04
  - Complete substitute for Xilinx XC18V04 of PC44 package
  - Complete substitute for Xilinx XQ18V04 of VQ44 package
  - Available for substitution of pin-to-pin, no modification for the whole design including PCB

2. Description

BQ18V04 is a PROM product compatible with Xilinx XQ18V04. Initial devices in this 3.3V family are a 4-megabit in-system programmable FLASH-based PROM that provides an repeatedly erased, non-volatile method for storing large FPGA configuration bitstreams in militray equipment on the ground or in space.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short valid time after $\overline{CE}$ and OE/$\overline{Reset}$, data is available on the PROM DATA (D0) pin that is connected to the FPGA DIN pin. At every rising CCLK, PROM sends 1-bit data in turn. When the FPGA is in Slave Serial mode, the PROM and the FPGA are clocked by an external clock. Parallel configuration mode is similar to serial configuration mode, and Data output terminal is D0-D7.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs

in this chain are interconnected. BQ18V04 can be cascaded with Xilinx configuration PROM including XQ18V04 and XQ17V16, etc.

3. Structure

The structure of BQ18V04 includes three main logic block. See Figure 1.

- ✧ JTAG interface
- ✧ Serial and parallel interface
- ✧ FLASH memory

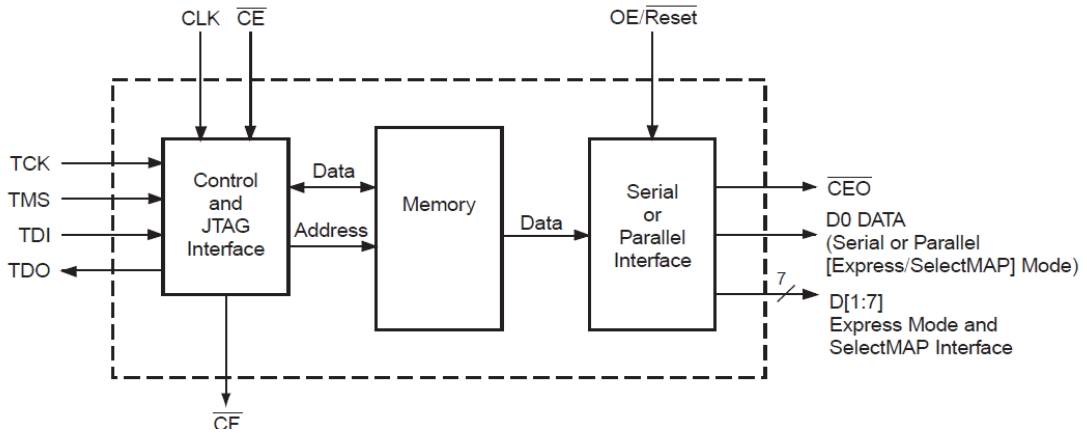


Figure 1: BQ18V04 Series Block Diagram

4. Pinout and Pin Description

Table 1: Pin Names and Descriptions

Pin Name	Function	Pin Decription
D0~D7	DATA OUT	D0-D7 are the output pins to provide parallel data for configuring a FPGA. In serial mode, D1-D7 can be not connected and is in a high-impedance state by default.
CLK	DATA IN	Each rising edge on the CLK input increments the internal address counter if both $\overline{CE}$ is Low and OE/$\overline{Reset}$ is High.
OE/$\overline{RESET}$	DATA IN DATA OUT OUTPUT ENABLE	When Low, this input holds the address counter reset and the DATA output is in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM is reset. Polarity is NOT programmable.
$\overline{CE}$	DATA IN	When $\overline{CE}$ is High, this pin puts the device into standby mode and resets the address counter. The DATA output pin is in a high-impedance state, and the device is in low power standby mode.
$\overline{CF}$	DATA OUT	Allows JTAG CONFIG instruction to initiate FPGA

	OUTPUT ENABLE	configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.
$\overline{CEO}$	DATA OUT	Chip Enable Output ($\overline{CEO}$) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. When OE/$\overline{RESET}$ goes Low, $\overline{CEO}$ stays High until the PROM is brought out of reset by bringing OE/$\overline{RESET}$ High.
	OUTPUT ENABLE	
GND		Ground connection
TMS	MODE SELECT	The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50K ohm resistive pull-up on it to provide a logic "1" to the device if the pin is not driven.
TCK	CLOCK	This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.
TDI	DATA IN	This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50K ohm resistive pull-up on it to provide a logic "1" to the system if the pin is not driven.
TDO	DATA OUT	This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50K ohm resistive pull-up on it to provide a logic "1" to the system if the pin is not driven.
Vccint	INTERNAL VOLTAGE	Positive 3.3V supply voltage for internal logic and input buffers.
Vcco	I/O VOLTAGE	Positive 3.3V supply voltage connected to the output voltage drivers.

5. Product Description

5.1 Connecting BQ18V04

The outputs of BQ18V04 drive the inputs of inputs. Connectiong the FPGAdevice and the PROM in master serial mode, see Figure 2. In master serial mode, CCLK drives the CLK of PROM. Other signals are as following.

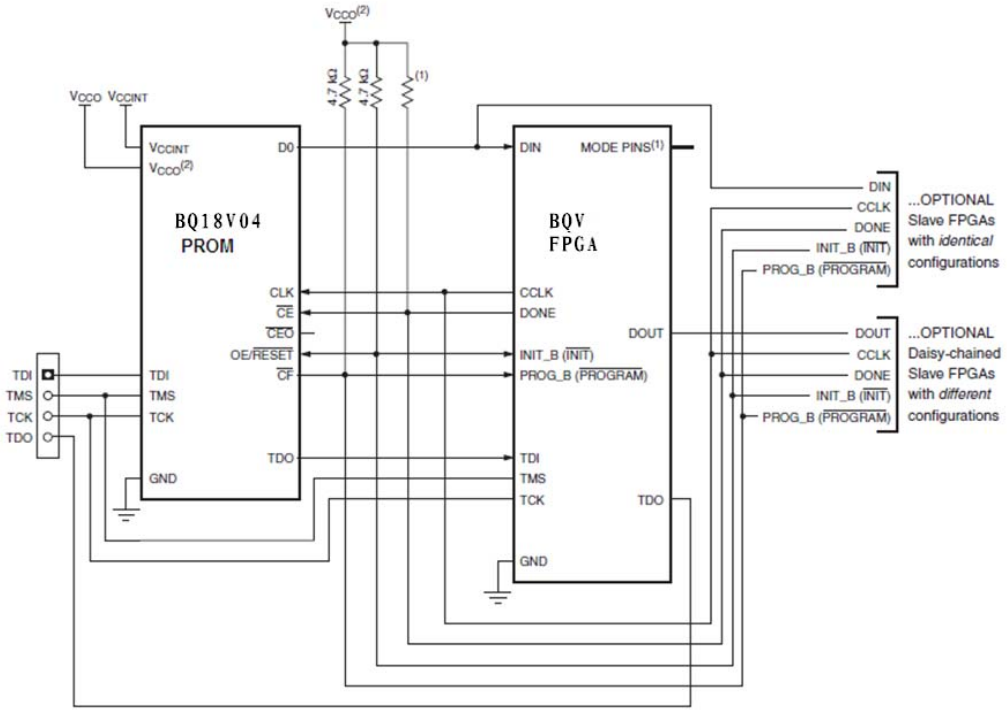


Figure 2: Master Serial Mode

- The DATA output(s) of the PROM(s) drives the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s) in Master Serial mode.
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain.
- The OE/$\overline{Reset}$ pins of all PROMs are connected to the $\overline{INIT}$ of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any configuration.
- The BQ18V04 $\overline{CE}$ input can be driven from the DONE pin. The CE input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded.$\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary power.
- In serial mode, the BQ18V04 D1-D7 can keep non-connected and are in a high-impendance state.
- Parallel mode is similar to slave serial mode. The DATA is clocked out of the PROM one byte per CCLK instead of one bit per CCLK cycle.

5.2 Operation Timing

After the BQ18V04 $\overline{CE}$ and OE/$\overline{Reset}$ are valid for a short time, the data of PROM are transferred to the Din terminal of FPGA through the D0 terminal. Figure 3 shows the operation timing.

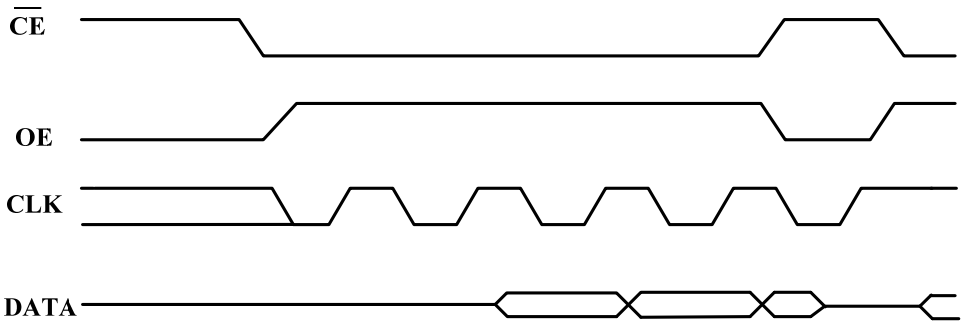


Figure 3: PROM operation timing

5.3 Initiating FPGA Configuration

The BQ18V04 devices incorporate a pin named $\overline{CF}$ that is controllable through the JTAG CONFIG instruction. Executing the CONFIG instruction through JTAG pulses the $\overline{CF}$ low, which resets the FPGA and initiates configuration. The $\overline{CF}$ pin must be connected to the $\overline{PROGRAM}$ pin on the FPGA(s). The Xilinx iMPACT software can issue the CONFIG command.

5.4 Configuration Modes

The BQ18V04 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the BQ18V04 device. This control register is accessible through JTAG, and is set using the "Parallel mode" setting on the Xilinx iMPACT software. Serial output is the default programming mode.

5.5 Cascading Configuration

For multiple FPGAs configured as a serial daisy-chain, or a single FPGA requiring larger configuration memories in a serial or SelectMAP configuration mode, cascaded PROMs provide additional memory. Figure 4 shows a daisy configuration mode.

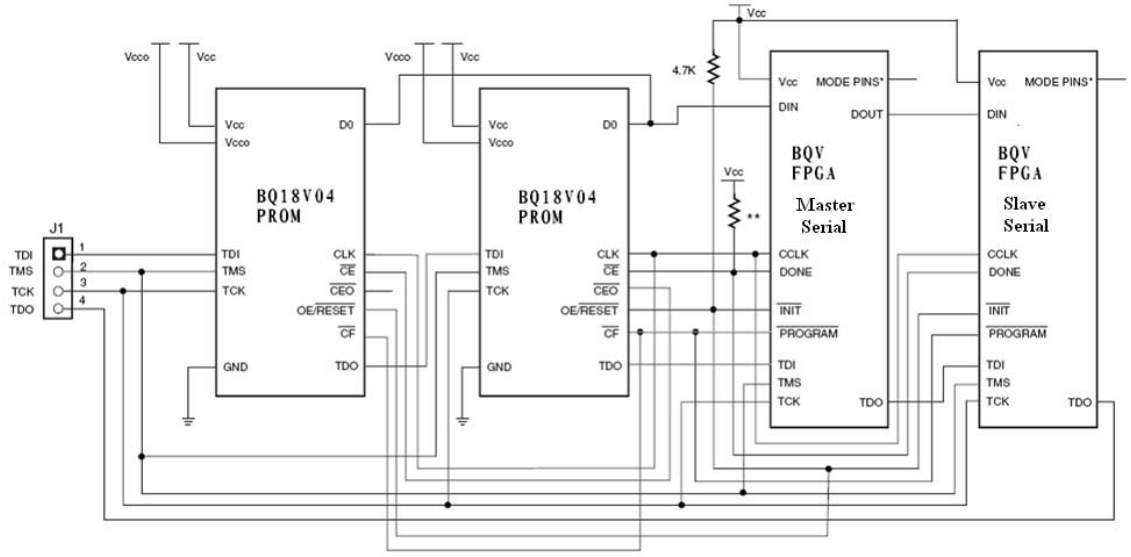


Figure 4: a daisy configuration mode

Multiple BQ18V04 devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the downstream device. The clock inputs and the data outputs of all BQ18V04 devices in the chain are interconnected. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its $\overline{CEO}$ output Low and drives its DATA line to a high-impedance state. The second PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

5.6 Reset Activation

On power up, OE/$\overline{Reset}$ is held low until the BQ18V04 is active (1.6 ms) and able to supply data after receiving a CCLK pulse from the FPGA. OE/$\overline{Reset}$ is connected to an external resistor to pull OE/$\overline{Reset}$ HIGH releasing the FPGA $\overline{INIT}$ and allowing configuration to begin. OE/$\overline{Reset}$ is held low until the BQ18V04 voltage reaches the operating voltage range. If the power drops below 2.0V, the PROM will reset. OE/$\overline{Reset}$ polarity is NOT programmable.

Note:

After BQ18V04 power on is compeleted, if OE/$\overline{Reset}$ is externally pull down, then the OE/$\overline{Reset}$ low pulse time will not be less than 1.6mS.

5.7 Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high-impedance state regardless of the state of the OE/$\overline{Reset}$ input. JTAG pins TMS, TDI and TDO can be in a high-impedance state or High. See table 2.

Table 2: Truth Table for Control inputs and outputs

Control Inputs		Internal Address	Outputs		
OE/$\overline{\text{RESET}}$	$\overline{\text{CE}}$		DATA	$\overline{\text{CEO}}$	I_{CC}
High	Low	If address ≤ TC(1): increment If address > TC(1): don't change	Active High-Z	High Low	Active Reduced
Low	Low	Held reset	High-Z	High	Active
High	High	Held reset	High-Z	High	Standby
Low	High	Held reset	High-Z	High	Standby

Notes:
1. TC = Terminal Count = highest address value. TC + 1 = address 0.

5.8 In-System Programming

In-System Programmable PROMs can be programmed individually, or two or more can be daisy-chained together and programmed in-system via the standard 4-pin JTAG protocol. In-system programming can use the following software kits.

1) Xilinx development system (iMPACT software and a download cable)
2) A third-party JTAG development system
3) A JTAG-compatible board tester
4) A simple microprocessor interface that emulates the JTAG instruction sequence

BQ18V04 can be programmed by the Xilinx HW-130, MultiPRO and third-party programmers. The ISP programming algorithm requires issuance of a reset that will cause OE/$\overline{\text{Reset}}$ to go low. Figure 5 shows the BQV18V04 TAP (Test Access Port) timing.

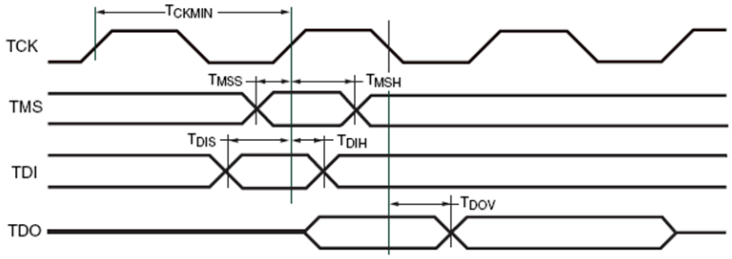


Figure 5: Test Access Port timing

5.9 JTAG Protocol Compatibility

The BQ18V04 family is fully compliant with the IEEE Std. 1149.1 Boundary-Scan, also known as JTAG. A Test Access Port (TAP) and registers are provided to support all required boundary scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the BQ18V04 device.

The boundary-scan register is a 8-bit register. It supports many instructions, including BYPAS, SAMPLE/PRELOAD, EXTEST, CLAMP, HIGHZ, IDCODE, USERCODE and CONFIG. Table 4 lists the instruction code and function of these

instructions.

Table 4: Boundary Scan Instructions

Boundary-Scan Command	Binary Code(7:0)	Description
Required Instructions		
BYPASS	11111111	Enables BYPASS
SAMPLE/PRELOAD	00000001	Enables boundary-scan SAMPLE/PRELOAD operation
EXTEST	00000000	Enables boundary-scan EXTEST operation
Optional Instructions		
CLAMP	11111010	Enables boundary-scan CLAMP operation
HIGHZ	11111100	All outputs in high-impedance state simultaneously
IDCODE	11111110	Enables shifting out 32-bit IDCODE
USERCODE	11111101	Enables shifting out 32-bit USERCODE
BQ18V04 Specific Instructions		
CONFIG	11101110	Initiates FPGA configuration by pulsing $\overline{CF}$ pin low

The IDCODE of BQ18V04 is 05026093h. The USERCODE register is user-programmable, which shows the programmed content of the device. If the device is blank or was not loaded during programming, the USERCODE register will contain FFFFFFFFh.

6. Electrical Parameters

Electrical parameters of BQ18V04

Parameter	Symbol	Conditions（Unless special conditions, 3.0V≤Vccint≤3.6V，3.0V≤Vcco≤3.6V，-55℃ ≤T_A≤ 125℃）	Limit		Units
			Min	Max	
High-level output voltage	V_{OH}	I_{OH}=-4mA，V_{CCINT}=3.0V，V_{CCO}=3.0V	2.4	—	V
Low-level output voltage	V_{OL}	I_{OL}=4mA，V_{CCINT}=3.0V，V_{CCO}=3.0V	—	0.4	V

Input high voltage leakage current	I_{IH}	V_{CCINT}=3.6V，V_{CCO}=3.6，V_{IN}=3.6V	—	10	μA
Input low voltage leakage current	$\|I_{IL}\|$	V_{CCINT}=3.6V，V_{CCO}=3.6，V_{IN}=0V	—	10	μA
JTAG input pins leakage current	IIL_{JTAG}	V_{CCINT}=3.6V，V_{CCO}=3.6V，V_{IN}=3.6V	-100	—	μA
Output High-Z leakage current	I_{OZH}	V_{CCINT}=3.6V，V_{CCO}=3.6V，V_{IN}=3.6V	-10	10	μA
High-level input voltage	V_{IH}	V_{CCINT}=3.3V，V_{CCO}=3.3V	2.0	—	V
Low-level input voltage	V_{IL}	V_{CCINT}=3.3V,V_{CCO}=3.3V	—	0.8	V
Supply current, standby mode	I_{CCSTA}	V_{CCINT}=3.6V，V_{CCO}=3.6V	—	20	mA
Supply current, active mode	I_{CCDYN}	V_{CCINT}=3.6V，V_{CCO}=3.6V，f=25MHz	—	50	mA
Input and output capacitance	C_{in}/ $_{out}$	f=1.0MHz，T_A=25 ℃	—	15	pF
Function test	—	V_{CCINT}=3.3V，V_{CCO}=3.3V，f=40MHz	—	—	—
TDO valid delay	T_{DOV}	V_{CCINT}=3.0V，V_{CCO}=3.0V（See Figure 1A, 1B）	—	25	ns
CLK to data D0-D7 delay	T_{CAC}		—	25	ns

6.1 Operating Conditions

Absolute Maximum Ratings:

Internal supply voltage(V_{CCINT}) …… -0.5V～+4.0V

IO supply voltage(V_{CCO}) …… -0.5V～+4.0V

DC input voltage(V_{IN}) internal threshold …… -0.5V～+5.5V

Voltage applied to High-Z output(V_{TS}) …… -0.5V～+5.5V

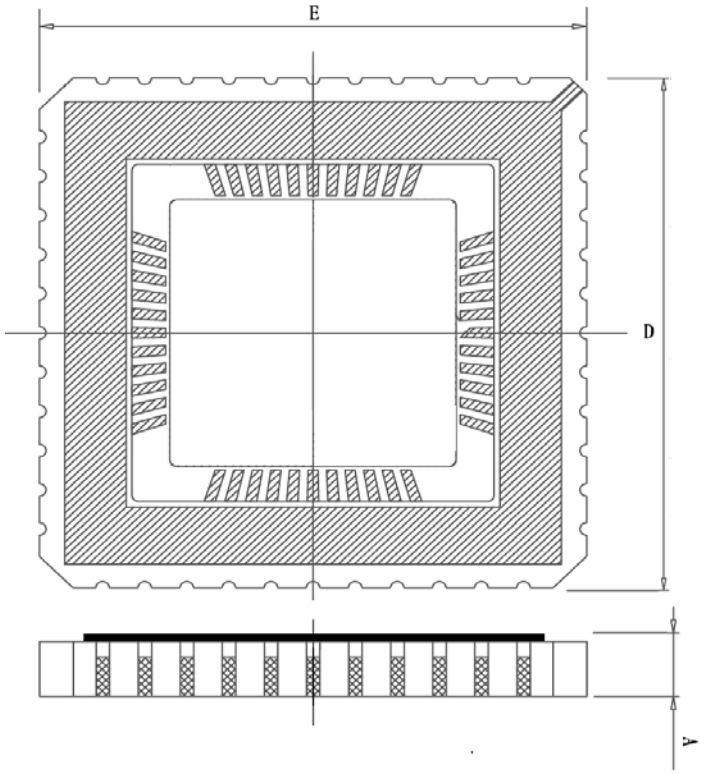
Lead soldering temperature of CLCC44（T_h）10s ..... 220℃
Lead soldering temperature of CQFP44（T_h）10s ..... 260℃
Thermal resistance, junction to case（θ_{JC}） .....1℃/W
Junction temperature（T_J） ..... 150℃
Storage temperature(T_{STG}) ..... -65℃～+150℃
Data retention time（T_{DR}） ..... 20 years
Max erase/program cycles（T_{PE}） 2000

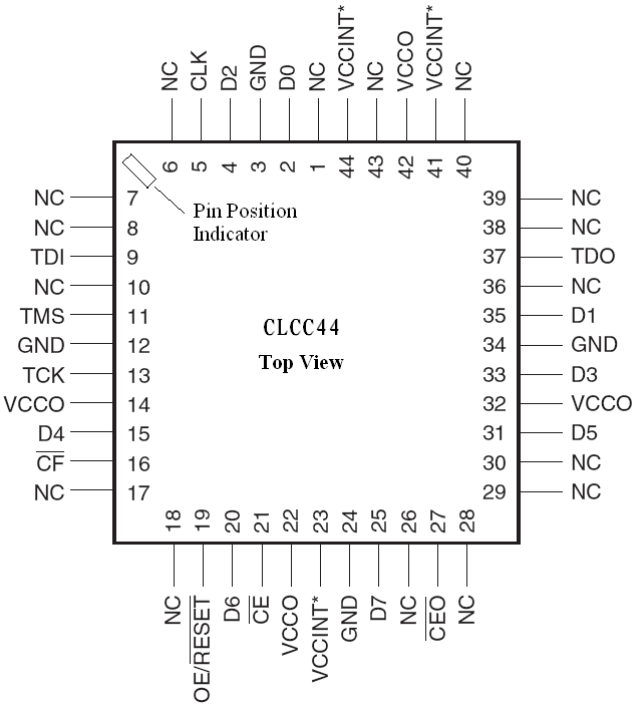
6.2 Recommended Operating Conditions

Recommended operating conditions:
Internal voltage supply（V_{CCINT}） ..... 3.0V～3.6V
Supply voltage for I/O for 3.3V operation（V_{CCO}）.....3.0V～3.6V
High-level input voltage（V_{IH}） ..... 2.0V～3.6V
Low-level input voltage（V_{IL}） .....0V～0.8V
Operating temperature（TC） ..... -55℃～+125℃

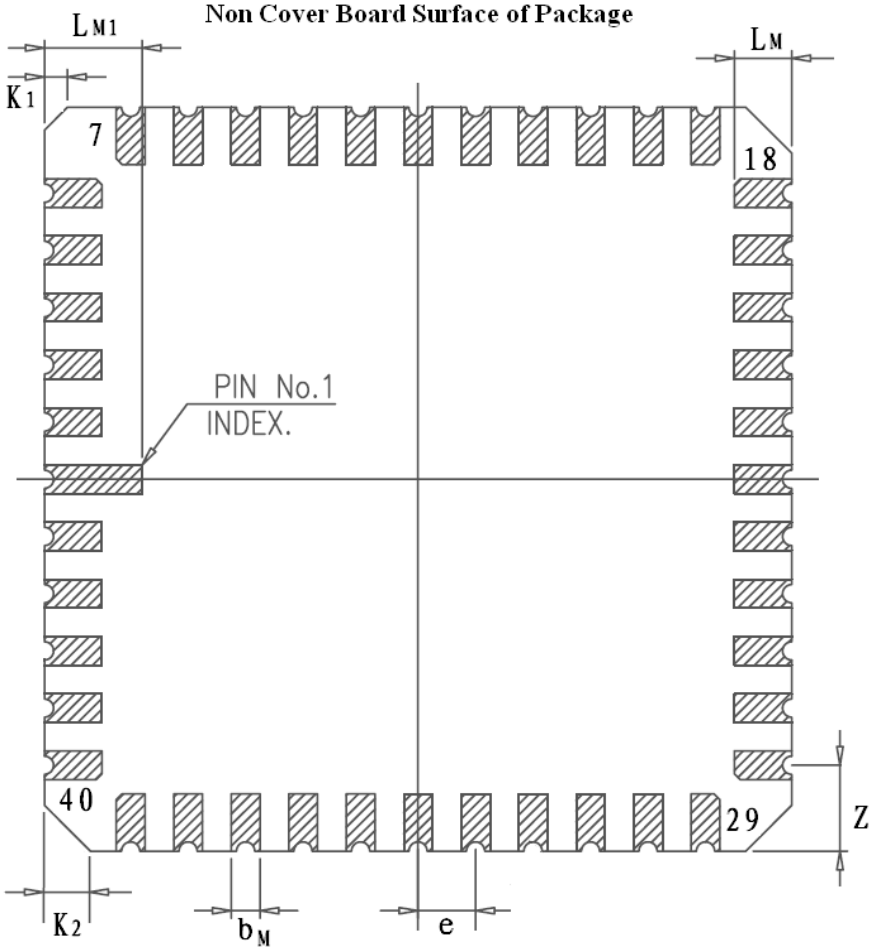
7. Package Description

BQ18V04 packaged with CCLC44 is named BQ18V04CL. BQ18V04 packaged with CQFP44 is named BQ18V04CQ. The dimension and pin arrangement of BQ18V04 CCLC44 package:





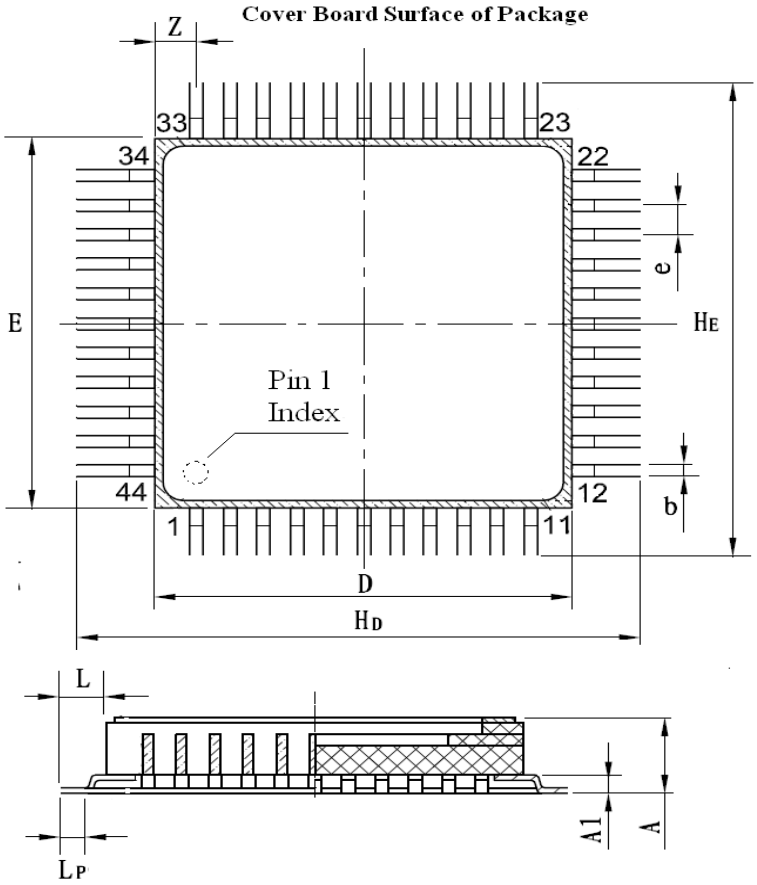
Non Cover Board Surface of Package

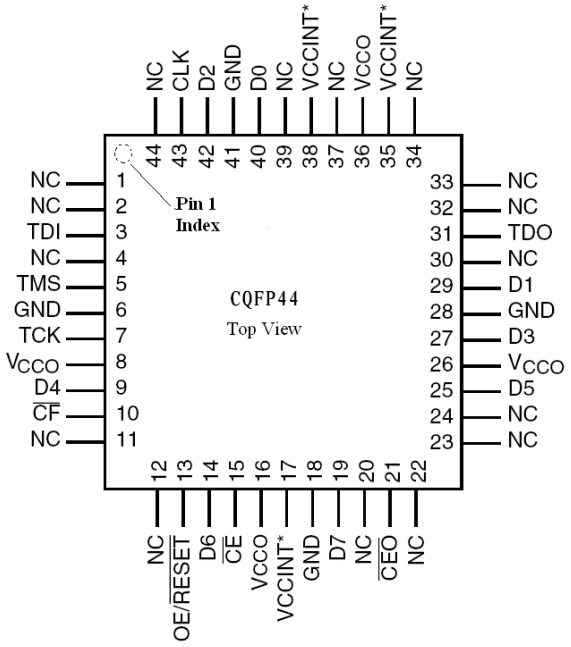


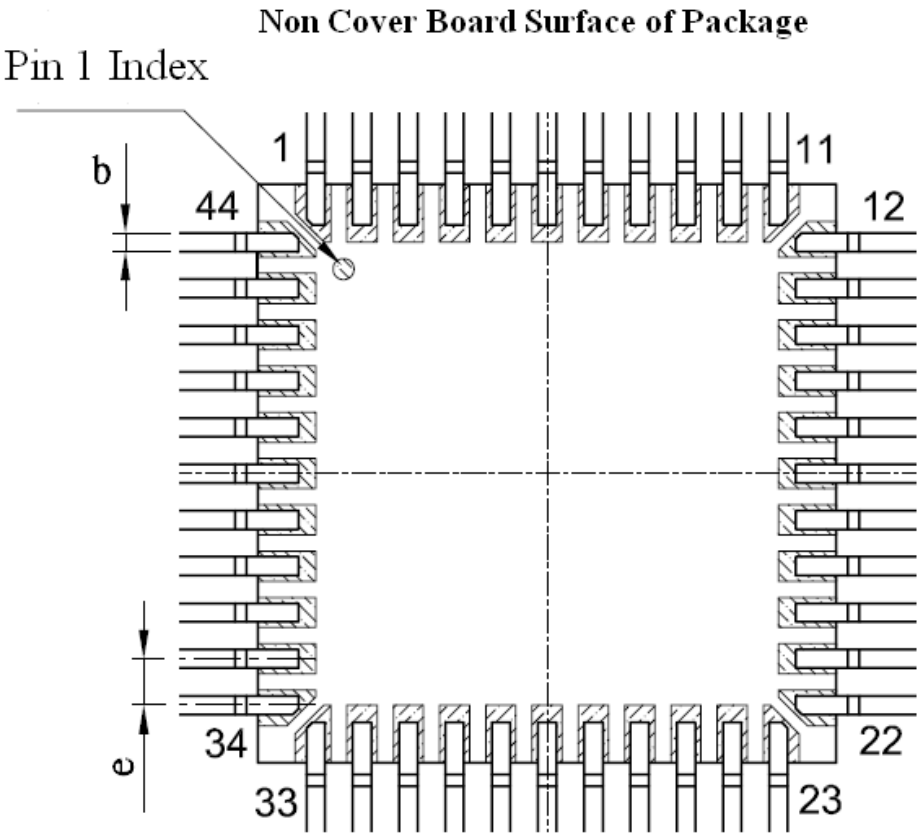
Units: mm

SYMBOL	INCHES		
	MIN	NOM	MAX
A	1.63	——	3.05
b_M	0.56	——	0.71
e	——	1.27	——
K_1	——	——	0.63
K_2	0.77	——	——
L_M	1.14	——	1.40
L_{M1}	1.95	——	2.36
D	16.25	——	16.76
E	16.25	——	16.76
Z	——	1.91	——

The dimension and pin arrangement of BQ18V04 CQFP44 package:


Cover Board Surface of Package
Z
33
23
34
22
e
E
HE
Pin 1
Index
44
12
b
1
11
D
HD
L
A1
A
LP


NC 1
NC 2
TDI 3
NC 4
TMS 5
GND 6
TCK 7
VCCO 8
D4 9
CF 10
NC 11
12 NC
13 OE/RESET
14 D6
15 CE
16 VCCO
17 VCCINT*
18 GND
19 D7
20 NC
21 CEO
22 NC
23 NC
24 NC
25 D5
26 VCCO
27 D3
28 GND
29 D1
30 NC
31 TDO
32 NC
33 NC
34 NC
35 VCCINT*
36 VCCO
37 NC
38 VCCINT*
39 NC
40 D0
41 GND
42 D2
43 CLK
44 NC
Pin 1
Index
CQFP44
Top View



Units: mm

SYMBOL	MIN	NOM	MAX
A	1.90	—	2.90
A1	0.35	—	—
b	—	0.32	—
c	0.11	—	0.2
e	—	0.80	—
D/E	9.70	—	10.30
HD/HE	12.00	—	13.50
L	1.30	—	1.80
Lp	0.80	—	1.20
Z	—	—	1.27

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