Ver 1.0

# BQ5V Series FPGA

# Datasheet

**Part Number:BQ5VSX35T/50T/95T/240T/LX155T**

# INDEX

*1. Feature ..... 3*

*2. General Description ..... 4*

*3. Architecture ..... 5*

3.1 Architecture Overview ..... 5

3.2 Architecture Features ..... 8

*4. Configuration Interfaces ..... 13*

4.1 Serial Configuration Interface ..... 13

4.2 SelectMAP Configuration Interface ..... 19

4.3 SPI Configuration Interface ..... 33

4.4 Byte Peripheral Interface Parallel Flash Mode ..... 36

*5. Electrical Characteristics ..... 41*

5.1 DC Characteristics ..... 41

5.2 Power-On Power Supply Requirements ..... 44

5.3 SelectIO™ DC Input and Output Levels ..... 45

5.4 HT DC Specifications (HT_25) ..... 46

5.5 LVDS DC Specifications (LVDS_25) ..... 47

5.6 Extended LVDS DC Specifications (LVDSEXT_25) ..... 47

5.7 LVPECL DC Specifications (LVPECL_25) ..... 47

*6. Pin Definitions ..... 48*

*Appendix I Pinout Information and Package ..... 51*

# 1. Feature

- **Two platforms LXT and SXT**
  - Virtex-5 LXT: High-performance logic with advanced serial connectivity
  - Virtex-5 SXT: High-performance signal processing
- **Cross-platform compatibility**
  - LXT and SXT devices are footprint compatible in the same package using adjustable voltage regulators
- **Temperature**
  - Guaranteed over the full military temperature range(–55℃ to +125℃)
- **Development System**
  - Supported by Xilinx ISE Development Systems
- **Most advanced, high-performance, optimal-utilization, FPGA fabric**
  - Real 6-input look-up table (LUT) technology
  - Dual 5-LUT option
  - Improved reduced-hop routing
  - 64-bit distributed RAM option
  - SRL32/Dual SRL16 option
- **Powerful clock management tile (CMT) clocking**
  - Digital Clock Manager (DCM) blocks for zero delay buffering, frequency synthesis, and clock phase shifting
  - PLL blocks for input jitter filtering, zero delay buffering, frequency synthesis, and phase-matched clock division
- **36-Kbit block RAM/FIFOs**
  - True dual-port RAM blocks
  - Enhanced optional programmable FIFO logic
  - Programmable
    True dual-port widths up to 36
    Simple dual-port widths up to 72
  - Built-in optional error-correction circuitry
  - Optionally program each block as two independent 18-Kbit blocks
- **High-performance parallel SelectIO technology**
  - 1.2 to 3.3V I/O Operation
  - Source-synchronous interfacing using ChipSync™ technology
  - Digitally-controlled impedance (DCI) active termination
  - Flexible fine-grained I/O banking
  - High-speed memory interface support
- **Advanced DSP48E slices**
  - 25 x 18, two's complement, multiplication
  - Optional adder, subtracter, and accumulator
  - Optional pipelining
  - Optional bitwise logical functionality
  - Dedicated cascade connections
- **Flexible configuration options**
  - SPI and Parallel FLASH interface
  - Multi-bitstream support with dedicated fallback reconfiguration logic
  - Auto bus width detection capability
- **System Monitoring capability on all devices**
  - On-chip/Off-chip thermal monitoring
  - On-chip/Off-chip power supply monitoring
  - JTAG access to all monitored quantities
- **Integrated Endpoint blocks for PCI Express Designs**
  - Compliant with the PCI Express Base Specification 1.1
  - x1, x4, or x8 lane support per block
  - Works in conjunction with RocketIO™ transceivers
- **Tri-mode 10/100/1000 Mb/s Ethernet MACs**
  - RocketIO transceivers can be used as PHY or connect to external PHY using many soft MII (Media

Independent Interface) options

- **RocketIO**
  - GTP transceivers 100 Mb/s to 3.75 Gb/s
- **65-nm copper CMOS process technology**
- **1.0V core voltage**
- **High signal-integrity flip-chip packaging available in standard**

## 2. General Description

The BQ5V Series provides the newest most powerful features in the Space Level FPGA market. In addition to the most advanced, high-performance logic fabric, BQ5V FPGAs contain many hard-IP system level blocks, including powerful 36-Kbit block RAM/FIFOs, second generation 25 x 18 DSP slices, SelectIO technology with built-in digitally- controlled impedance, ChipSync source-synchronous interface blocks, system monitor functionality, enhanced clock management tiles with integrated DCM (Digital Clock Managers) and phase-locked-loop (PLL) clock generators, and advanced configuration options. Additional platform dependant features include power-optimized high-speed serial transceiver blocks for enhanced serial connectivity, PCI Express compliant integrated Endpoint blocks, and tri-mode Ethernet MACs (Media Access Controllers). These features allow advanced logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 65-nm state-of-the-art copper process technology, BQ5V FPGAs are a programmable alternative to custom ASIC technology. Most advanced system designs require the programmable strength of FPGAs. BQ5V FPGAs offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP, hard/soft microprocessor, and connectivity capabilities.

Table 1:BQ5V series FPGA Members

| Device | System Gates | CLB | | | DSP48E Slices | Block RAM Blocks (Kb) | CMTs | EndpointBlocks for PCI Express | Ethernet MACs | Max GTPs | Max I/O Pads | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Array Row x Col. | Slices | Maximum Distributed RAM Kbits | | | | | | | | |
| BQ5V SX35T | 3.5M | 80 x 34 | 5440 | 520 | 192 | 3024 | 2 | 1 | 4 | 8 | 360 | BGA665 |
| BQ5V SX50T | 5M | 120 x 34 | 8160 | 780 | 288 | 4752 | 6 | 1 | 4 | 12 | 360 | BGA665 |
| BQ5V SX95T | 9.5M | 160 x 46 | 14,720 | 1,520 | 640 | 8,784 | 6 | 1 | 4 | 16 | 640 | CCGA1136 |
| BQ5V SX240T | 24M | 240 x 78 | 37440 | 4200 | 1056 | 18576 | 6 | 1 | 4 | 24 | 960 | BGA1738 |
| BQ5V LX155T | 15.5M | 160 x 76 | 24320 | 1640 | 128 | 7632 | 6 | 1 | 4 | 16 | 680 | CCGA1738 |

# 3. Architecture

## 3.1 Architecture Overview

**BQ5V FPGA Logic**

- On average, one to two speed grade improvement over Virtex-4 devices
- Cascadable 32-bit variable shift registers or 64-bit distributed memory capability
- Superior routing architecture with enhanced diagonal routing supports block-to-block connectivity with minimal hops
- Up to 240,000 logic cells including:
  - Up to 149,760 internal fabric flip-flops with clock enable
  - Up to 149,760 real 6-input look-up tables (LUTs)
  - Two outputs for dual 5-LUT mode gives enhanced utilization
  - Logic expanding multiplexers and I/O registers

**550 MHz Clock Technology**

- Up to six Clock Management Tiles (CMTs)
  - Each CMT contains two DCMs and one PLL—up to eighteen total clock generators
  - Flexible DCM-to-PLL or PLL-to-DCM cascade
  - Precision clock deskew and phase shift
  - Flexible frequency synthesis
  - Multiple operating modes to ease performance trade-off decisions
  - Improved maximum input/output frequency
  - Fine-grained phase shifting resolution
  - Input jitter filtering
  - Low-power operation
  - Wide phase shift range
- Differential clock tree structure for optimized low-jitter clocking and precise duty cycle
- 32 global clock networks
- Regional, I/O, and local clocks in addition to global clocks

**SelectIO Technology**

- Up to 960 user I/Os
- Wide selection of I/O standards from 1.2V to 3.3V
- Extremely high-performance
  - Up to 800Mb/s HSTL and SSTL (on all single-ended I/Os)
  - Up to 1.25 Gb/s LVDS (on all differential I/O pairs)
- True differential termination on-chip
- Same edge capture at input and output I/Os
- Extensive memory interface support

**550 MHz Integrated Block Memory**

- Up to 16.4 Mbits of integrated block memory
- 36-Kbit blocks with optional dual 18-Kbit mode
- True dual-port RAM cells
- Independent port width selection (x1 to x72)
  - Up to x36 total per port for true dual port operation
  - Up to x72 total per port for simple dual port operation (one Read port and one Write port)
  - Memory bits plus parity/sideband memory support for x9, x18, x36, and x72 widths
  - Configurations from 32K x 1 to 512 x 72 (8K x 4 to 512 x 72 for FIFO operation)
- Multirate FIFO support logic

  - Full and Empty flag with fully programmable Almost Full and Almost Empty flags
- Synchronous FIFO support without Flag uncertainty
- Optional pipeline stages for higher performance
- Byte-write capability
- Dedicated cascade routing to form 64K x 1 memory without using FPGA routing
- Integrated optional ECC for high-reliability memory requirements
- Special reduced-power design for 18 Kbit (and below) operation

**550 MHz DSP48E Slices**

- 25 x 18 two's complement multiplication
- Optional pipeline stages for enhanced performance
- Optional 48-bit accumulator for multiply accumulate (MACC) operation with optional accumulator cascade to 96-bits
- Integrated adder for complex-multiply or multiply-add operation
- Optional bitwise logical operation modes
- Independent C registers per slice
- Fully cascadable in a DSP column without external routing resources

**ChipSyncSource-Synchronous Interfacing Logic**

- Works in conjunction with SelectIO technology to simplify source-synchronous interfaces
- Per-bit deskew capability built into all I/O blocks (variable delay line on all inputs and outputs)
- Dedicated I/O and regional clocking resources (pins and trees)
- Built-in data serializer/deserializer logic with corresponding clock divider support in all I/O
- Networking/telecommunication interfaces up to 1.25 Gb/s per I/O

**Digitally Controlled Impedance (DCI) Active I/O Termination**

- Optional series or parallel termination
- Temperature and voltage compensation
- Makes board layout much easier
  - Reduces resistors
  - Places termination in the ideal location, at the signal source or destination

**Configuration**

- Support for platform Flash, standard SPI Flash, or standard parallel NOR Flash configuration
- Bitstream support with dedicated fallback reconfiguration logic
- 256-bit AES bitstream decryption provides intellectual property security and prevents design copying
- Improved bitstream error detection/correction capability
- Auto bus width detection capability
- Partial Reconfiguration via ICAP port

**Advanced Flip-Chip Packaging**

- Pre-engineered packaging technology for proven superior signal integrity
  - Minimized inductive loops from signal to return
  - Optimal signal-to-PWR/GND ratios
- Reduces SSO induced noise by up to 7x
- standard packages

**Integrated Endpoint Block for PCI Express Compliance**

- Works in conjunction with RocketIO GTP transceivers to deliver full PCI Express Endpoint functionality with minimal FPGA logic utilization.
- Compliant with the PCI Express Base Specification 1.1

- PCI Express Endpoint block or Legacy PCI Express Endpoint block
- x8, x4, or x1 lane width
- Power management support
- Block RAMs used for buffering
- Fully buffered transmit and receive
- Management interface to access PCI Express configuration space and internal configuration
- Supports the full range of maximum payload sizes
- Up to 6 x 32 bit or 3 x 64 bit BARs (or a combination of 32 bit and 64 bit)

**Tri-Mode Ethernet Media Access Controller**

- Designed to the IEEE 802.3-2002 specification
- Operates at 10, 100, and 1,000 Mb/s
- Supports tri-mode auto-negotiation
- Receive address filter (5 address entries)
- Fully monolithic 1000Base-X solution with RocketIO GTP transceivers
- Supports multiple external PHY connections (RGMII, GMII, etc.) interfaces through soft logic and SelectIO resources
- Supports connection to external PHY device through SGMII using soft logic and RocketIO GTP transceivers
- Receive and transmit statistics available through separate interface
- Separate host and client interfaces
- Support for jumbo frames
- Support for VLAN
- Flexible, user-configurable host interface
- Supports IEEE 802.3ah-2004 unidirectional mode

**RocketIO GTP Transceivers**

- Full-duplex serial transceiver capable of 100 Mb/s to 3.75 Gb/s baud rates
- 8B/10B, user-defined FPGA logic, or no encoding options
- Channel bonding support
- CRC generation and checking
- Programmable pre-emphasis or pre-equalization for the transmitter
- Programmable termination and voltage swing
- Programmable equalization for the receiver
- Receiver signal detect and loss of signal indicator
- User dynamic reconfiguration using secondary configuration bus
- Out of Band (OOB) support for Serial ATA (SATA)
- Electrical idle, beaconing, receiver detection, and PCI Express and SATA spread-spectrum clocking support
- Less than 100 mW typical power consumption
- Built-in PRBS Generators and Checkers

**System Monitor**

- On-Chip temperature measurement (±4 ℃)
- On-Chip power supply measurement (±1%)
- Easy to use, self-contained
  - No design required for basic operation
  - Autonomous monitoring of all on-chip sensors
  - User programmable alarm thresholds for on-chip sensors
- User accessible 10-bit 200kSPS ADC
  - Automatic calibration of offset and gain error
  - DNL = ±0.9 LSBs maximum
- Up to 17 external analog input channels supported
  - 0V to 1V input range
  - Monitor external sensors e.g., voltage, temperature
  - General purpose analog inputs
- Full access from fabric or JTAG TAP to System Monitor
- Fully operational prior to FPGA configuration and during device power

down (access via JTAG TAP only)

**65-nm Copper CMOS Process**

- 1.0V Core Voltage
- 12-layer metal provides maximum routing capability and accommodates hard-IP immersion
- Triple-oxide technology for proven reduced static power consumption

## 3.2 Architecture Features

This section briefly describes BQ5V Series features.

**Input/Output Blocks (SelectIO)**

IOBs are programmable and can be categorized as follows:

- Programmable single-ended or differential (LVDS) operation
- Input block with an optional single data rate (SDR) or double data rate (DDR) register
- Output block with an optional SDR or DDR register
- Bidirectional block
- Per-bit deskew circuitry
- Dedicated I/O and regional clocking resources
- Built-in data serializer/deserializer

The IOB registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended standards:

- LVTTL
- LVCMOS (3.3V, 2.5V, 1.8V, 1.5V, and 1.2V)
- PCI (33 and 66 MHz)
- PCI-X
- GTL and GTLP
- HSTL 1.5V and 1.8V (Class I, II, III, and IV)
- HSTL 1.2V (Class 1)
- SSTL 1.8V and 2.5V (Class I and II)

The Digitally Controlled Impedance (DCI) I/O feature can be configured to provide on-chip termination for each single-ended I/O standard and some differential I/O standards.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V only)
- BLVDS (Bus LVDS)
- ULVDS
- Hypertransport™
- Differential HSTL 1.5V and 1.8V (Class I and II)
- Differential SSTL 1.8V and 2.5V (Class I and II)
- RSDS (2.5V point-to-point)

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

Per-bit deskew circuitry allows for programmable signal delay internal to the FPGA. Per-bit deskew flexibly provides fine-grained increments of delay to carefully produce a range of signal delays. This is especially useful for synchronizing signal edges in source-synchronous interfaces.

General purpose I/O in select locations (eight per bank) are designed to be “regional clock capable” I/O

by adding special hardware connections for I/O in the same locality. These regional clock inputs are distributed within a limited region to minimize clock skew between IOBs. Regional I/O clocking supplements the global clocking resources.

Data serializer/deserializer capability is added to every I/O to support source-synchronous interfaces. A serial-to- parallel converter with associated clock divider is included in the input path, and a parallel-to-serial converter in the output path.

**Configurable Logic Blocks (CLBs)**

A BQ5V FPGA CLB resource is made up of two slices. Each slice is equivalent and contains:

- Four function generators
- Four storage elements
- Arithmetic logic gates
- Large multiplexers
- Fast carry look-ahead chain

The function generators are configurable as 6-input LUTs or dual-output 5-input LUTs. SLICEMs in some CLBs can be configured to operate as 32-bit shift registers (or 16-bit x 2 shift registers) or as 64-bit distributed RAM. In addition, the four storage elements can be configured as either edge-triggered D-type flip-flops or level sensitive latches. Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

**Block RAM**

The 36 Kbit true dual-port RAM block resources are programmable from 32K x 1 to 512 x 72, in various depth and width configurations. In addition, each 36-Kbit block can also be configured to operate as two, independent 18- Kbit dual-port RAM blocks.

Each port is totally synchronous and independent, offering three “read-during-write” modes. Block RAM is cascadable to implement large embedded storage blocks. Additionally, back-end pipeline registers, clock control circuitry, built-in FIFO support, ECC, and byte write enable features are also provided as options.

**Global Clocking**

The CMTs and global-clock multiplexer buffers provide a complete solution for designing high-speed clock networks.

Each CMT contains two DCMs and one PLL. The DCMs and PLLs can be used independently or extensively cascaded. Up to six CMT blocks are available, providing up to eighteen total clock generator elements.

Each DCM provides familiar clock generation capability. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90 °, 180 °, and 270 ° phase-shifted versions of the output clocks. Fine-grained phase shifting offers higher-resolution phase adjustment with fraction of the clock period increments. Flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency.

To augment the DCM capability, BQ5V FPGA CMTs also contain a PLL. This block provides reference clock jitter filtering and further frequency synthesis options.

BQ5V devices have 32 global-clock MUX buffers. The clock tree is designed to be differential. Differential clocking helps reduce jitter and duty cycle distortion.

**DSP48E Slices**

DSP48E slice resources contain a 25 x 18 two's complement multiplier and a 48-bit adder/subtacter/accumulator. Each DSP48E slice also contains extensive cascade capability to efficiently implement high-speed DSP algorithms.

**Routing Resources**

All components in BQ5V devices use the same interconnect scheme and the same access to the global routing matrix. In addition, the CLB-to-CLB routing is designed to offer a complete set of connectivity in as few hops as possible. Timing models are shared, greatly improving the predictability of the performance for high- speed designs.

**Boundary Scan**

Boundary-Scan instructions and associated data registers support a standard methodology for accessing and configuring BQ5V devices, complying with IEEE standards 1149.1 and 1532.

**Configuration**

BQ5V devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE-1532 and -1149)
- SPI mode (Serial Peripheral Interface standard Flash)
- BPI-up/BPI-down modes (Byte-wide Peripheral interface standard x8 or x16 NOR Flash)

In addition, BQ5V devices also support the following configuration options:

- 256-bit AES bitstream decryption for IP protection
- Multi-bitstream management (MBM) for cold/warm boot support
- Parallel configuration bus width auto-detection
- Parallel daisy chain
- Configuration CRC and ECC support for the most robust, flexible device integrity checking

**System Monitor**

FPGAs are an important building block in high availability/reliability infrastructure. Therefore, there is need to better monitor the on-chip physical environment of the FPGA and its immediate surroundings within the system. For the first time, the BQ5V family System Monitor facilitates

easier monitoring of the FPGA and its external environment. Every member of the BQ5V family contains a System Monitor block. The System Monitor is built around a 10-bit 200kSPS ADC (Analog-to-Digital Converter). This ADC is used to digitize a number of on-chip sensors to provide information about the physical environment within the FPGA. On-chip sensors include a temperature sensor and power supply sensors. Access to the external environment is provided via a number of external analog input channels. These analog inputs are general purpose and can be used to digitize a wide variety of voltage signal types. Support for unipolar, bipolar, and true differential input schemes is provided. There is full access to the on- chip sensors and external channels via the JTAG TAP, allowing the existing JTAG infrastructure on the PC board to be used for analog test and advanced diagnostics during development or after deployment in the field. The System Monitor is fully operational after power up and before configuration of the FPGA. System Monitor does not require an explicit instantiation in a design to gain access to its basic functionality. This allows the System Monitor to be used even at a late stage in the design cycle.

**Tri-Mode (10/100/1000 Mb/s) Ethernet MACs**

BQ5V devices contain up to eight embedded Ethernet MACs, two per Ethernet MAC block. The blocks have the following characteristics:

- Designed to the IEEE 802.3-2002 specification
- UNH-compliance tested
- RGMII/GMII Interface with SelectIO or SGMII interface when used with RocketIO transceivers
- Half or full duplex
- Supports Jumbo frames
- 1000 Base-X PCS/PMA: When used with RocketIO GTP transceiver, can provide complete 1000 Base-X implementation on-chip
- DCR-bus connection to microprocessors

**Integrated Endpoint Blocks for PCI Express**

BQ5V devices contain up to four integrated Endpoint blocks. These blocks implement Transaction Layer, Data Link Layer, and Physical Layer functions to provide complete PCI Express Endpoint functionality with minimal FPGA logic utilization. The blocks have the following characteristics:

- Compliant with the PCI Express Base Specification 1.1
- Works in conjunction with RocketIO transceivers to provide complete endpoint functionality
- 1, 4, or 8 lane support per block

**RocketIO GTP Transceivers**

4 - 24 channel RocketIO GTP transceivers capable of running 100 Mb/s to 3.75 Gb/s.

- Full clock and data recovery
- 8/16-bit or 10/20-bit datapath support
- Optional 8B/10B or FPGA-based encode/decode

Integrated FIFO/elastic buffer

- Channel bonding and clock correction support
- Embedded 32-bit CRC generation/checking
- Integrated comma-detect or A1/A2 detection
- Programmable pre-emphasis (AKA transmitter equalization)
- Programmable transmitter output swing
- Programmable receiver equalization
- Programmable receiver termination
- Embedded support for:

− Out of Band (OOB) signalling: Serial ATA

− Beaconing, electrical idle, and PCI Express receiver detection

- Built-in PRBS generator/checker

# 4. Configuration Interfaces

BQ5V devices have six configuration interfaces. Each configuration interface corresponds to one or more configuration modes and bus width, shown in Table 2.

Table 2: BQ5V Device Configuration Modes

| Configuration Mode | M[2:0] | Bus Width | CCLK Direction |
|---|---|---|---|
| Master Serial(2) | 000 | 1 | Output |
| Master SPI(2) | 001 | 1 | Output |
| Master BPI-Up(2) | 010 | 8, 16 | Output |
| Master BPI-Down(2) | 011 | 8, 16 | Output |
| Master SelectMAP(2) | 100 | 8, 16 | Output |
| JTAG | 101 | 1 | Input (TCK) |
| Slave SelectMAP | 110 | 8, 16, 32 | Input |
| Slave Serial | 111 | 1 | Input |

**Notes:**

1. Parallel configuration mode bus is auto-detected by the configuration logic.
2. In Master configuration mode, the CCLK pin is the clock source for the BQ5V internal configuration logic. The BQ5V CCLK output pin must be free from reflections to avoid double-clocking the internal configuration logic. Refer to the "Board Layout for Configuration Clock (CCLK)" section for more details.

## 4.1 Serial Configuration Interface

In serial configuration modes, the FPGA is configured by loading one configuration bit per CCLK cycle:

- In Master Serial mode, CCLK is an output.
- In Slave Serial mode, CCLK is an input.

Figure 1 shows the basic BQ5V serial configuration interface. There are four methods of configuring an FPGA in serial mode:

- Master serial configuration
- Slave serial configuration
- Serial daisy-chain configuration
- Ganged serial configuration

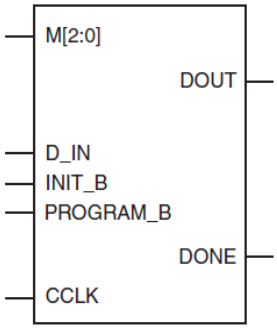


Figure 1:BQ5V FPGA Serial Configuration Interface

Table 3 describes the Serial Configuration Interface.

Table 3:BQ5V FPGA Serial Configuration Interface Pins

| Pin Name | Type | Dedicated or Dual-Purpose | Description |
|---|---|---|---|
| M[2:0] | Input | Dedicated | Mode Pins – determine configuration mode |
| CCLK | Input or Output | Dedicated | Configuration clock source for all configuration modes except JTAG |
| D_IN | Input | Dedicated | Serial configuration data input, synchronous to rising CCLK edge |
| DOUT_BUSY | Output | Dedicated | Serial data output for downstream daisy-chained devices |
| DONE | Bidirectional, Open-Drain, or Active | Dedicated | Active High signal indicating configuration is complete:<br>0 = FPGA not configured<br>1 = FPGA configured<br>Refer to the BitGen section of the *Development System Reference Guide* for software settings. |
| INIT_B | Input or Output, Open-Drain | Dedicated | Before the Mode pins are sampled, INIT_B is an input that can be held Low to delay configuration.<br>After the Mode pins are sampled, INIT_B is an open-drain active Low output indicating whether a CRC error occurred during configuration:<br>0 = CRC error<br>1 = No CRC error |
| PROGRAM_B | Input | Dedicated | Active-Low asynchronous full-chip reset |

**Clocking Serial Configuration Data**

Figure 2 shows how configuration data is clocked into BQ5V devices in Slave Serial and Master Serial modes.

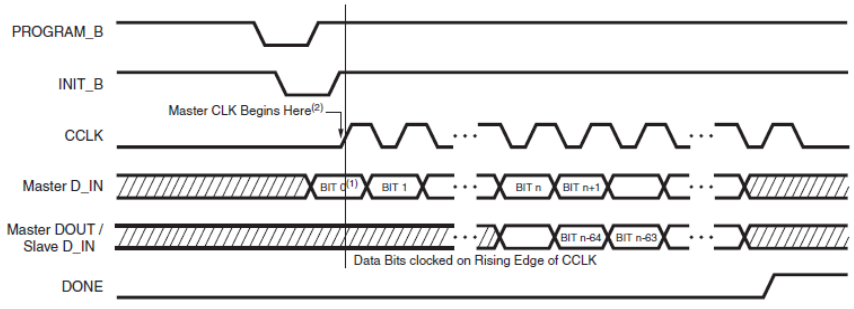



Figure 2: Serial Configuration Clocking Sequence

Notes relevant to Figure 2:

1. Bit 0 represents the MSB of the first byte. For example, if the first byte is 0xAA (1010_1010), bit 0 = 1, bit 1 = 0, bit 2 = 1, etc.
2. For Master configuration mode, CCLK does not transition until after the Mode pins are

sampled, as indicated by the arrow.

3. CCLK can be free-running in Slave serial mode.

**Master Serial Configuration**

The Master Serial mode is designed so that the FPGA can be configured from a Xilinx/BMTI configuration PROM, as shown in Figure 3.

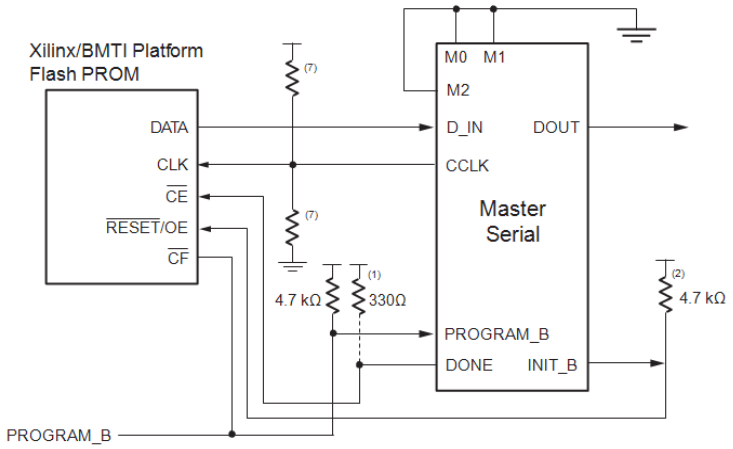



Figure 3: Master Serial Mode Configuration

Notes relevant to Figure 3:

1. The DONE pin is by default an open-drain output requiring an external pull-up resistor. The DONE pin has a programmable active driver. To enable it, enable the DriveDONE option in BitGen.
2. The INIT_B pin is a bidirectional, open-drain pin. An external pull-up resistor is required.
3. The BitGen startup clock setting must be set for CCLK for serial configuration.
4. The PROM in this diagram represents one or more Xilinx PROMs. Multiple Xilinx PROMs can be cascaded to increase the overall configuration storage capacity.
5. The BIT file must be reformatted into a PROM file before it can be stored on the Xilinx PROM. Refer to the “Generating PROM Files” section.
6. On some Xilinx PROMs, the reset polarity is programmable. RESET should be configured as active Low when using this setup.
7. The CCLK net requires Thevenin parallel termination.
8. Master serial mode configuration is specific to the Platform Flash XCFS and XCFP PROM only.

**Slave Serial Configuration**

Slave serial configuration is typically used for devices in a serial daisy chain or when configuring a single device from an external microprocessor or CPLD. Design considerations are similar to Master serial configuration except for the direction of CCLK. CCLK must be driven from an external clock source.

**Serial Daisy Chains**

Multiple BQ5V devices can be configured from a single configuration source by arranging the

devices in a serial daisy chain. In a serial daisy chain, devices receive their configuration data through their D_IN pin, passing configuration data along to downstream devices through their DOUT pin. The device closest to the configuration data source is considered the most upstream device, while the device furthest from the configuration data source is considered the most downstream device.

In a serial daisy chain, the configuration clock is typically provided by the most upstream device in Master serial mode. All other devices are set for Slave serial mode. Figure 4 illustrates this configuration.

Another alternative is to use SPI mode for the first device. The daisy chain data is still sent out through DOUT in SPI mode.

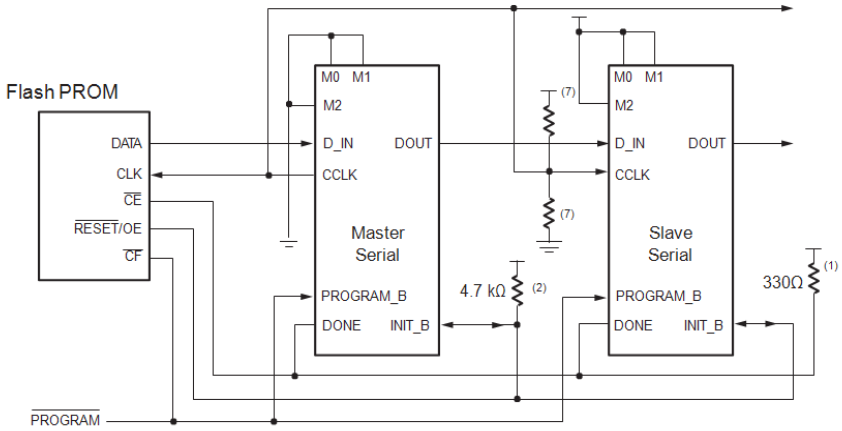



Figure 4: Master/Slave Serial Mode Daisy Chain Configuration

Notes relevant to Figure 4:

1. The DONE pin is by default an open-drain output requiring an external pull-up resistor. For all devices except the first, the active driver on DONE must be disabled. For the first device in the chain, the active driver on DONE can be enabled. See “Guidelines and Design Considerations for Serial Daisy Chains.”
2. The INIT_B pin is a bidirectional, open-drain pin. An external pull-up resistor is required.
3. The BitGen startup clock setting must be set for CCLK for serial configuration.
4. The PROM in this diagram represents one or more Xilinx PROMs. Multiple Xilinx PROMs can be cascaded to increase the overall configuration storage capacity.
5. The BIT file must be reformatted into a PROM file before it can be stored on the Xilinx PROM. Refer to the “Generating PROM Files” section.
6. On some Xilinx PROMs, the reset polarity is programmable. RESET should be configured as active Low when using this setup.
7. The CCLK net requires Thevenin parallel termination.
8. Serial daisy chains are specific to the Platform Flash XCFS and XCFP PROM only.

The first device in a serial daisy chain is the last to be configured. CRC checks only include the data for the current device, not for any others in the chain. (See “Cyclic Redundancy Check (Step 7)”.) After the last device in the chain finishes configuration and passes its CRC check, it enters the Startup sequence. At the Release DONE pin phase in the Startup sequence, the device places its DONE pin in a High-Z state while the next to the last device in the chain is configured. After all devices release their DONE pins, the common DONE signal is either pulled High externally or

driven High by the first device in the chain. On the next rising CCLK edge, all devices move out of the Release DONE pin phase and complete their startup sequences.

It is important that all DONE pins in a Slave serial daisy chain be connected. Only the first device in the serial daisy chain should have the DONE active pull-up driver enabled. Enabling the DONE driver on downstream devices causes contention on the DONE signal.

**Mixed Serial Daisy Chains**

BQ5V devices can be daisy-chained with the Virtex, Spartan™-II, Virtex-E, Spartan-IIE, Virtex-II, Virtex-II Pro, Spartan-3, and Virtex-4 families. There are three important design considerations when designing a mixed serial daisy chain:

- Many older FPGA devices cannot accept as fast a CCLK frequency as a BQ5V device can generate. Select a configuration CCLK speed supported by all devices in the chain.
- BQ5V devices should always be at the beginning of the serial daisy chain, with older family devices located at the end of the chain.
- All Virtex/BMTI device families have similar BitGen options. The guidelines provided for BQ5V BitGen options should be applied to all Virtex/BMTI devices in a serial daisy chain.
- The number of configuration bits that a device can pass through its DOUT pin is limited. This limit varies for different families (Table 4). The sum of the bitstream lengths for all downstream devices must not exceed the number in Table 4 for each family.

Table 4: Maximum Number of Configuration Bits, Various Device Families

| Architecture | Maximum DOUT Bits |
|---|---|
| BQ5V , BQR2V, Virtex-5, Virtex-4, Virtex-II Pro, and Virtex-II Devices | 32 x ($2^{27}$ – 1) = 4,294,967,264 |
| Spartan-3 Devices | 32 x ($2^{27}$ – 1) = 4,294,967,264 |
| BQVR, Virtex, Virtex-E, Spartan-II, and Spartan-IIE Devices | 32 x ($2^{20}$ – 1) = 33,554,216 |

**Guidelines and Design Considerations for Serial Daisy Chains**

There are a number of important considerations for serial daisy chains:

**Startup Sequencing (GTS)**

GTS should be released before DONE or during the same cycle as DONE to ensure the BQ5V device is operational when all DONE pins have been released.

**Active DONE Driver**

All devices except the first should disable the driver on the DONE pin (refer to the BitGen section of the Development System Reference Guide for software settings). The first device in a chain is programmed last:

- DriveDone is disabled (all devices except the first)
- DriveDone is enabled (first device)

Alternatively, the driver can be disabled for all DONE pins and an external pull-up resistor can be added to pull the signal High after all devices have released it.

**Connect All DONE Pins**

It is important to connect the DONE pins for all devices in a serial daisy chain. Failing to connect the DONE pins can cause configuration to fail. For debugging purposes, it is often helpful to have a way

of disconnecting individual DONE pins from the common DONE signal, so that devices can be individually configured through the serial or JTAG interface.

**DONE Pin Rise Time**

After all DONE pins are released, the DONE pin should rise from logic 0 to logic 1 in one CCLK cycle. External pull-up resistors are required. If additional time is required for the DONE signal to rise, the BitGen donepipe option can be set for all devices in the serial daisy chain. (Refer to the BitGen section of the Development System Reference Guide for software settings.)

**Ganged Serial Configuration**

More than one device can be configured simultaneously from the same bitstream using a ganged serial configuration setup (Figure 5). In this arrangement, the serial configuration pins are tied together such that each device sees the same signal transitions. One device is typically set for Master serial mode (to drive CCLK) while the others are set for Slave serial mode. For ganged serial configuration, all devices must be identical. Configuration can be driven from a configuration PROM or from an external configuration controller.

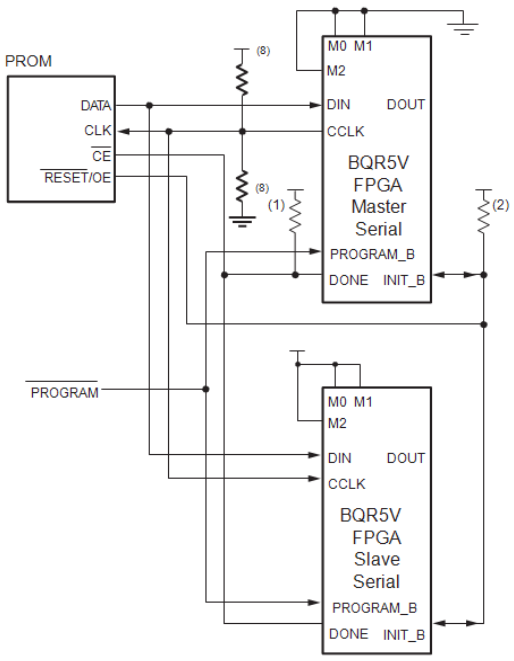



Figure 5: Ganged Serial Configuration

Notes relevant to Figure 5:

1. For ganged serial configuration, the optional DONE driver must be disabled for all devices if one device is set for Master mode because each device might not start up on exactly the same CCLK cycle. An external pull-up resistor is required in this case.
2. The INIT_B pin is a bidirectional, open-drain pin. An external pull-up resistor is required.
3. The BitGen startup clock setting must be set for CCLK for serial configuration.
4. The PROM in this diagram represents one or more Xilinx PROMs. Multiple PROMs can be cascaded to increase the overall configuration storage capacity.
5. The BIT file must be reformatted into a PROM file before it can be stored on the PROM. Refer to the “Generating PROM Files” section.

6. On some Xilinx PROMs, the reset polarity is programmable. RESET should be configured as active Low when using this setup.
7. For ganged serial configuration, all devices must be identical (same IDCODE) and must be configured with the same bitstream.
8. The CCLK net requires Thevenin parallel termination.
9. Ganged serial configuration is specific to the Platform Flash XCFS and XCFP PROM only.
10. Fallback and Multiboot are not supported in ganged serial configuration. There are a number of important considerations for ganged serial configuration:

- Startup Sequencing (GTS)

GTS should be released before DONE or during the same cycle as DONE to ensure all devices are operational when all DONE pins have been released.

- Disable the Active DONE Driver for All Devices

For ganged serial configuration, the active DONE driver must be disabled for all devices if the DONE pins are tied together, because there can be variations in the startup sequencing of each device. A pull-up resistor is therefore required on the common DONE signal.

-g DriveDone:no (BitGen option, all devices)

- Connect all DONE pins if using a Master Device

It is important to connect the DONE pins for all devices in ganged serial configuration if one FPGA is used as the Master device. Failing to connect the DONE pins can cause configuration to fail for individual devices in this case. If all devices are set for Slave serial mode, the DONE pins can be disconnected (if the external CCLK source continues toggling until all DONE pins go High).

For debugging purposes, it is often helpful to have a way of disconnecting individual DONE pins from the common DONE signal.

- DONE Pin Rise Time

After all DONE pins are released, the DONE pin should rise from logic 0 to logic 1 in one CCLK cycle. If additional time is required for the DONE signal to rise, the BitGen donepipe option can be set for all devices in the serial daisy chain.

- Configuration Clock (CCLK) as Clock Signal for Board Layout

The CCLK signal is relatively slow, but the edge rates on the BQ5V input buffers are very fast. Even minor signal integrity problems on the CCLK signal can cause the configuration to fail. (Typical failure mode: DONE Low and INIT_B High.) Therefore, design practices that focus on signal integrity, including signal integrity simulation with IBIS, are recommended.

- Signal Fanout

Designers must focus on good signal integrity when using ganged serial configuration. Signal integrity simulation is recommended.

- PROM Files for Ganged Serial Configuration

PROM files for ganged serial configuration are identical to the PROM files used to configure single devices. There are no special PROM file considerations.

## 4.2 SelectMAP Configuration Interface

The SelectMAP configuration interface (Figure 6) provides an 8-bit, 16-bit, or 32-bit bidirectional data bus interface to the BQ5V configuration logic that can be used for both configuration and

readback. (For details, refer to “Readback and Configuration Verification.”) The bus width of SelectMAP is automatically detected (see “Bus Width Auto Detection”).

CCLK is an output in Master SelectMAP mode; in Slave SelectMAP, CCLK is an input. One or more BQ5V devices can be configured through the SelectMAP bus.

There are four methods of configuring an FPGA in SelectMAP mode:

- Single device Master SelectMAP
- Single device Slave SelectMAP
- Multiple device SelectMAP bus
- Multiple device ganged SelectMAP

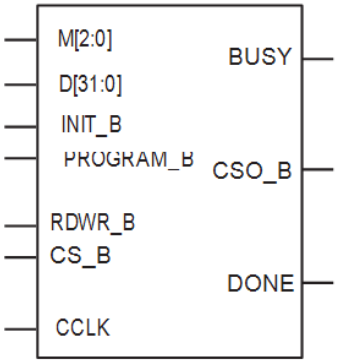



Figure 6:BQ5V Device SelectMAP Configuration Interface

Table 5 describes the SelectMAP configuration interface.

Table 5:BQ5V Device SelectMAP Configuration Interface Pins

| Pin Name | Type | Dedicated or Dual-Purpose | Description |
|---|---|---|---|
| M[2:0] | Input | Dedicated | Mode pins - determine configuration mode |
| CCLK | Input and Output | Dedicated | Configuration clock source for all configuration modes except JTAG |
| D[31:0] | Three-State Bidirectional | Dual-Purpose | Configuration and readback data bus, clocked on the rising edge of CCLK. |
| BUSY | Three-State Output | Dedicated | Indicates that the device is not ready to send readback data. For BQ5V devices, the BUSY signal is only needed for readback; it is not needed for configuration (see “SelectMAP Data Loading”). |
| DONE | Bidirectional, Open-Drain or active | Dedicated | Active-High signal indicating configuration is complete:<br>0 = FPGA not configured<br>1 = FPGA configured |
| INIT_B | Input or Output, | Dedicated | Before the Mode pins are sampled, INIT_B is an input that can be held Low to delay configuration.<br>After the Mode pins are sampled, INIT_B is an open-drain, active-Low output indicating whether a CRC error occurred during |

| | | | |
|---|---|---|---|
| | Open-Drain | | configuration:<br>0 = CRC error<br>1 = No CRC error<br>When the SEU detection function is enabled, INIT_B is optionally driven Low when a read back CRC error is detected. |
| PROGRAM_B | Input | Dedicated | Active-Low asynchronous full-chip reset. |
| CS_B | Input | Dedicated | Active-Low chip select to enable the SelectMAP data bus (see "SelectMAP Data Loading"):<br>0 = SelectMAP data bus enabled<br>1 = SelectMAP data bus disabled |
| RDWR_B | Input | Dedicated | Determines the direction of the D[x:0] data bus (see "SelectMAP Data Loading"):<br>0 = inputs<br>1 = outputs<br>RDWR_B input can only be changed while CS_B is deasserted, otherwise an ABORT occurs (see "SelectMAP ABORT"). |
| CSO_B | Output | Dual-Purpose | Parallel daisy chain active-Low chip select output. Not used in single FPGA applications. |

**Single Device SelectMAP Configuration**

**High-Performance Platform Flash XL SelectMAP Configuration**

The Platform Flash XL is specially optimized for high-performance BQ5V FPGA configuration and ease-of-use. Platform Flash XL integrates 128 Mb of in-system programmable flash storage and performance features for configuration within a small-footprint FT64 package. Power-on burst read mode and dedicated I/O power supply enable Platform Flash XL to mate seamlessly with the BQ5V FPGA SelectMAP configuration interface. A wide, 16-bit data bus delivers the FPGA configuration bitstream at speeds to 800 Mb/s without wait states. A simplified model of the Platform Flash XL configuration solution for a BQ5V FPGA is shown in Figure 7.

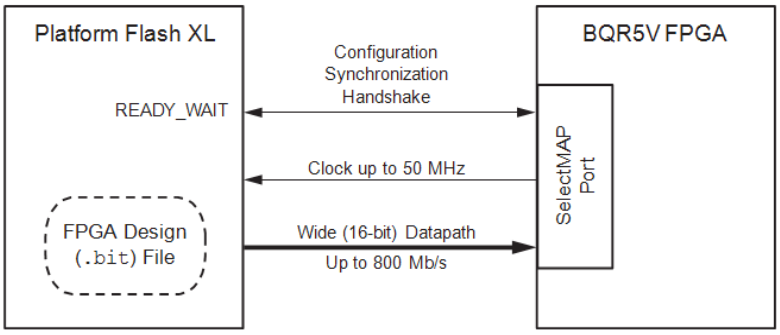



Figure 7: Platform Flash XL High-Performance FPGA Configuration

For BQ5V FPGA configuration, the Platform Flash XL takes advantage of the 16-bit SelectMAP feature to accomplish high-speed configuration. Minimal configuration time is achieved with an external, free-running oscillator driving the configuration clock in Slave SelectMAP mode. After configuration, the BQ5V FPGA can access any remaining memory space, beyond the bitstream, in the Platform Flash XL. The Platform Flash XL has a standard BPI NOR Flash interface. In addition

to the 16-bit data bus, which is dually used for SelectMAP configuration, the Platform Flash XL has a standard address bus and read/write control pins for random access reads and for sending CFI-compliant commands.

For prototype designs, the ISE® iMPACT software provides an indirect Platform Flash XL programming solution through the IEEE Standard 1149.1 (JTAG) port of the BQ5V FPGA. The iMPACT software downloads a pre-built design bitstream into the BQ5V FPGA that bridges the FPGA JTAG port to the FPGA BPI Flash configuration interface. The FPGA BPI Flash configuration interface is a superset of the FPGA SelectMAP interface. When the Platform Flash XL's standard address and control pins are connected to the corresponding FPGA BPI Flash interface pins, the iMPACT indirect programming solution can program the Platform Flash XL with the prototype design bitstream, as shown in Figure 8.

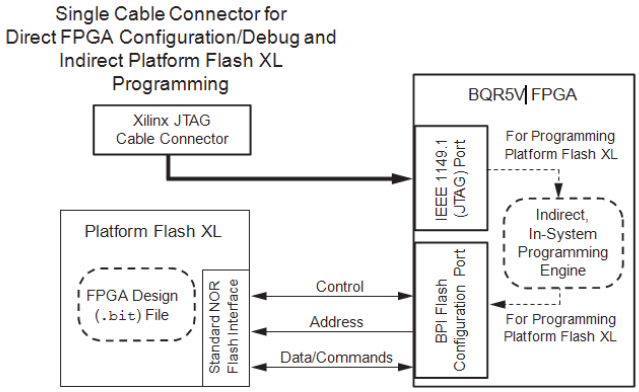



Figure 8: Indirect Programming Solution for Platform Flash XL

**Platform Flash PROM SelectMap Configuration**

The simplest way to configure a single device in SelectMAP mode is to connect it directly to a configuration PROM, as shown in Figure 9. In this arrangement, the device is set for Master SelectMAP mode, and the RDWR_B and CS_B pins are tied to ground for continuous data loading (see “SelectMAP Data Loading”).

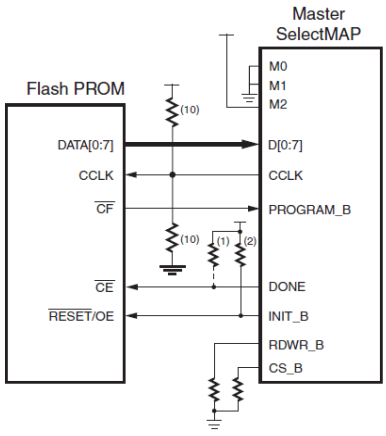



Figure 9: Single Device Master SelectMAP Configuration

Notes relevant to Figure 9:

1. The DONE pin is by default an open-drain output requiring an external pull-up resistor. In this arrangement, the active DONE driver can be enabled, eliminating the need for an external pull-up resistor.

The INIT_B pin is a bidirectional, open-drain pin. An external pull-up resistor is required.

2. The BitGen startup clock setting must be set for CCLK for SelectMAP configuration.
3. The PROM in this diagram represents one or more Xilinx PROMs. Multiple PROMs can be cascaded to increase the overall configuration storage capacity.
4. The BIT file must be reformatted into a PROM file before it can be stored on the PROM. Refer to the “Generating PROM Files” section.
5. On some Xilinx PROMs, the reset polarity is programmable. RESET should be configured as active Low when using this setup.
6. The Xilinx PROM must be set for parallel mode. This mode is not available for all devices.
7. When configuring a BQ5V device in SelectMAP mode from a Xilinx configuration PROM, the RDWR_B and CS_B signals can be tied Low (see “SelectMAP Data Loading”).
8. The BUSY signal does not need to be monitored for this setup and can be left unconnected (see “SelectMAP Data Loading”).
9. The CCLK net requires Thevenin parallel termination.
10. The D bus can be x8 or x16 for Master SelectMAP configuration.
11. Platform Flash PROM SelectMap configuration is specific to the Platform Flash XCFS and XCFP PROM only.

**Microprocessor-driven SelectMAP Configuration**

For custom applications where a microprocessor or CPLD is used to configure a single BQ5V device, either Master SelectMAP mode (use CCLK from the FPGA) or Slave SelectMAP mode can be used (Figure 10). Slave SelectMAP mode is preferred. See XAPP502, Using a Microprocessor to Configure Xilinx FPGAs via Slave Serial or SelectMAP Mode, for information on configuring Virtex devices using a microprocessor). Refer to the “Data Loading” section for details on handling the CS_B, RDWR_B, and BUSY signals.

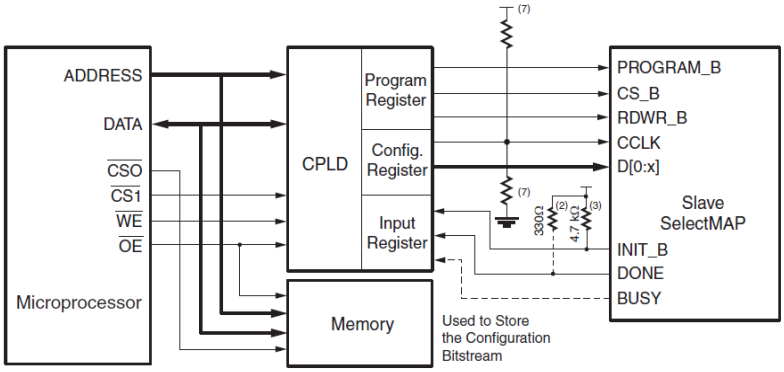



Figure 10: Single Slave Device SelectMAP Configuration from Microprocessor and CPLD

Notes relevant to Figure 10:

1. It is one of many possible implementations.
2. The DONE pin is by default an open-drain output requiring an external pull-up resistor. In this arrangement, the active DONE driver can be enabled, eliminating the need for an external pull-up resistor.
3. The INIT_B pin is a bidirectional, open-drain pin. An external pull-up resistor is required.
4. The BitGen startup clock setting must be set for CCLK for SelectMAP configuration.
5. The BUSY signal can be left unconnected if readback is not needed.

6. The CS_B and RDWR_B signals can be tied to ground if only one FPGA is going to be configured and readback is not needed.
7. The CCLK net requires Thevenin parallel termination.
8. The D bus can be x8, x16, or x32 for Slave SelectMAP configuration.

**Multiple Device SelectMAP Configuration**

Multiple BQ5V devices in Slave SelectMAP mode can be connected on a common SelectMAP bus (Figure 11). In a SelectMAP bus, the DATA, CCLK, RDWR_B, BUSY, PROGRAM_B, DONE, and INIT_B pins share a common connection between all of the devices. To allow each device to be accessed individually, the CS_B (Chip Select) inputs must not be tied together. External control of the CS_B signal is required and is usually provided by a microprocessor or CPLD.
If Readback is going to be performed on the device after configuration, the RDWR_B and BUSY signals must be handled appropriately.
Otherwise, RDWR_B can be tied Low and BUSY can be ignored. Unlike earlier Virtex devices, the BUSY signal never needs to be monitored when configuring BQ5V devices.

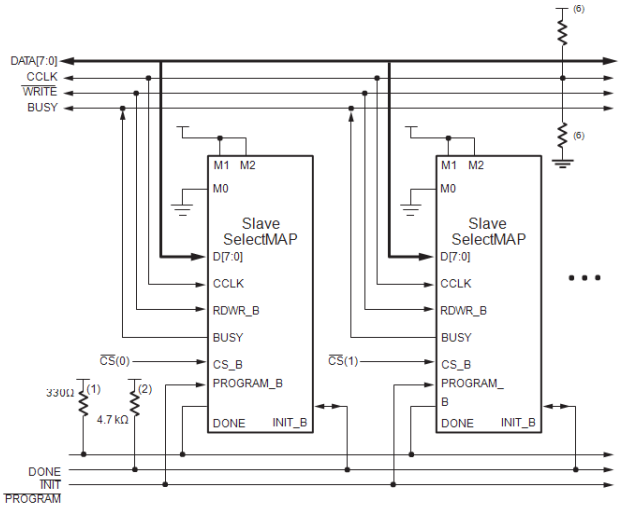



Figure 11: Multiple Slave Device Configuration on an 8-Bit SelectMAP Bus

Notes relevant to Figure 11:

1. The DONE pin is by default an open-drain output requiring an external pull-up resistor. In this arrangement, the active DONE driver must be disabled.
2. The INIT_B pin is a bidirectional, open-drain pin. An external pull-up resistor is required.
3. The BitGen startup clock setting must be set for CCLK for SelectMAP configuration.
4. The BUSY signals can be left unconnected if readback is not needed.
5. An external controller such as a microprocessor or CPLD is needed to control configuration.
6. The CCLK net requires Thevenin parallel termination.
7. The data bus can be x8, x16, or x32.

**Parallel Daisy Chain**

BQ5V FPGA configuration supports parallel daisy-chain. Figure 12 shows an example schematic of the leading device in BPI mode. The leading device can also be in Master or Slave SelectMAP modes. The D[15:0], CCLK, RDWR_B, PROGRAM_B, DONE, and INIT_B pins share a common

connection between all of the devices. The CS_B pins are daisy chained.

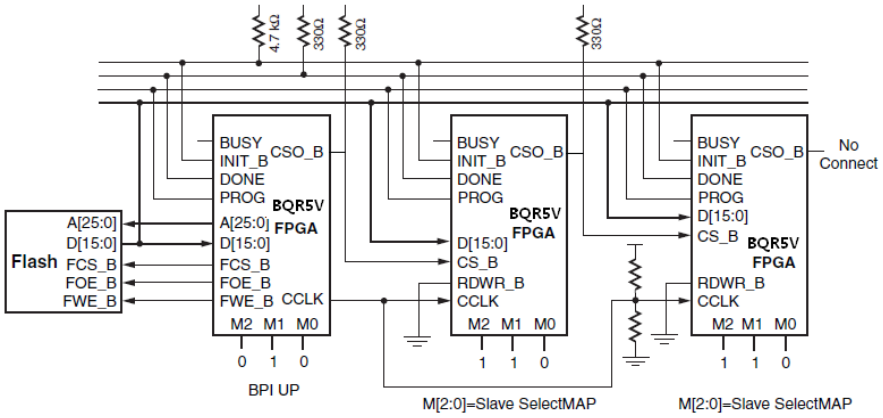



Figure 12: Parallel Daisy Chain

Notes relevant to Figure 12:

1. The DONE pin is by default an open-drain output requiring an external pull-up resistor. In this arrangement, the active DONE driver must be disabled.
2. The INIT_B pin is a bidirectional, open-drain pin. An external pull-up is required.
3. The BitGen startup clock setting must be set for CCLK for SelectMAP configuration.
4. The BUSY signals can be left unconnected if readback is not needed.
5. The CCLK net requires Thevenin parallel termination.
6. The FCS_B, FWE_B, FOE_B, CSO_B weak pull-up resistors should be enabled, otherwise external pull-up resistors are required for each pin. By default, all dual- mode I/Os have weak pull-downs after configuration.
7. The first device in the chain can be Master SelectMAP, Slave SelectMAP, BPI-Up, or BPI-Down.
8. Readback in the parallel daisy chain scheme is currently not supported.
9. AES decryption is not available in x16 or x32 mode, only in x8 mode.
10. Fallback is not supported in parallel daisy-chain.

**Ganged SelectMAP**

It is also possible to configure simultaneously multiple devices with the same configuration bitstream by using a ganged SelectMAP configuration. In a ganged SelectMAP arrangement, the CS_B pins of two or more devices are connected together (or tied to ground), causing all devices to recognize data presented on the D pins. All devices can be set for Slave SelectMAP mode if an external oscillator is available, or one device can be designated as the Master device, as illustrated in Figure 13.

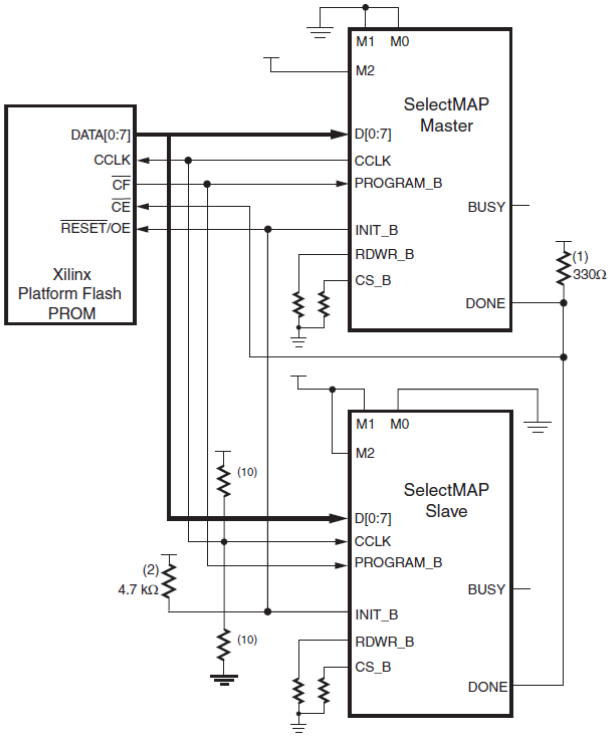



Figure 13:Ganged x8 SelectMAP Configuration

Notes relevant to Figure 13:

1. The DONE pin is by default an open-drain output requiring an external pull-up resistor. In this arrangement, the active DONE driver must be disabled for both devices.
2. The INIT_B pin is a bidirectional, open-drain pin. An external pull-up resistor is required.
3. The BitGen startup clock setting must be set for CCLK for SelectMAP configuration.
4. The BUSY signal is not used for ganged SelectMAP configuration.
5. The PROM in this diagram represents one or more Xilinx PROMs. Multiple Xilinx PROMs can be cascaded to increase the overall configurations storage capacity.
6. The BIT file must be reformatted into a PROM file before it can be stored on the Xilinx PROM. Refer to the “Generating PROM Files” section.
7. On some Xilinx PROMs, the reset polarity is programmable. Reset should be configured as active Low when using this setup.
8. The Xilinx PROM must be set for parallel mode. This mode is not available for all devices.
9. When configuring a BQ5V device in SelectMAP mode from a Xilinx configuration PROM, the RDWR_B and CS_B signals can be tied Low (see “SelectMAP Data Loading”).
10. The CCLK net requires Thevenin parallel termination.
11. Ganged SelectMap configuration is specific to the Platform Flash XCFS and XCFP PROM only.

If one device is designated as the Master, the DONE pins of all devices must be connected with the active DONE drivers disabled. An external pull-up resistor is required on the common DONE signal. Designers must carefully focus on signal integrity due to the increased fanout of the outputs from the PROM. Signal integrity simulation is recommended.

Readback is not possible if the CS_B signals are tied together, because all devices simultaneously attempt to drive the D signals.

**SelectMAP Data Loading**

The SelectMAP interface allows for either continuous or non-continuous data loading. Data loading is controlled by the CS_B, RDWR_B, CCLK, and BUSY signals.

**CS_B**

The Chip Select input (CS_B) enables the SelectMAP bus. When CS_B is High, the BQ5V device ignores the SelectMAP interface, neither registering any inputs nor driving any outputs. D and BUSY are placed in a High-Z state, and RDWR_B is ignored.

- If CS_B = 0, the device's SelectMAP interface is enabled.
- If CS_B = 1, the device's SelectMAP interface is disabled.

For a multiple device SelectMAP configuration, refer to Figure 12.

If only one device is being configure through the SelectMAP and readback is not required, or if ganged SelectMAP configuration is used, the CS_B signal can be tied to ground, as illustrated in Figure 9 and Figure 13.

**RDWR_B**

RDWR_B is an input to the BQ5V device that controls whether the data pins are inputs or outputs:

- If RDWR_B = 0, the data pins are inputs (writing to the FPGA).
- If RDWR_B = 1, the data pins are outputs (reading from the FPGA).

For configuration, RDWR_B must be set for write control (RDWR_B = 0). For readback, RDWR_B must be set for read control (RDWR_B = 1) while CS_B is deasserted. (For details, refer to "Readback and Configuration Verification.")

Changing the value of RDWR_B while CS_B is asserted triggers an ABORT if the device gets a rising CCLK edge (see "SelectMAP ABORT"). If readback is not needed, RDWR_B can be tied to ground or used for debugging with SelectMAP ABORT.

The RDWR_B signal is ignored while CS_B is deasserted. Read/write control of the 3-stating of the data pins is asynchronous. The FPGA actively drives SelectMAP data without regard to CCLK if RDWR_B is set for read control (RDWR_B = 1, Readback) while CS_B is asserted.

**CCLK**

All activity on the SelectMAP data bus is synchronous to CCLK. When RDWR_B is set for write control (RDWR_B = 0, Configuration), the FPGA samples the SelectMAP data pins on rising CCLK edges. When RDWR_B is set for read control (RDWR_B = 1, Readback), the FPGA updates the SelectMAP data pins on rising CCLK edges.

In Slave SelectMAP mode, configuration can be paused by stopping CCLK (see "Non- Continuous SelectMAP Data Loading").

**BUSY**

BUSY is an output from the FPGA indicating when the device is ready to drive readback data. Unlike earlier Virtex devices, BQ5V FPGAs never drive the BUSY signal during configuration, even at the maximum configuration frequency with an encrypted bitstream. The BQ5V device only drives BUSY during readback.

- If BUSY = 0 during readback, the SelectMAP data pins are driving valid readback data.
- If BUSY = 1 during readback, the SelectMAP data pins are not driving valid readback data.

When CS_B is deasserted (CS_B = 1), the BUSY pin is placed in a High-Z state.

BUSY remains in a High-Z state until CS_B is asserted. If CS_B is asserted before power-up (that is,

if the pin is tied to ground), BUSY initially is in a High-Z state, then driven Low after POR finishes, usually a few milliseconds (TBUSY), after VCCINT reaches VPOR but before INIT_B goes High. Unless readback is used, the BUSY pin can be left unconnected.

**Continuous SelectMAP Data Loading**

Continuous data loading is used in applications where the configuration controller can provide an uninterrupted stream of configuration data. After power-up, the configuration controller sets the RDWR_B signal for write control (RDWR_B = 0) and asserts the CS_B signal (CS_B = 0), causing the device to drive BUSY Low (this transition is asynchronous). RDWR_B must be driven Low before CS_B is asserted, otherwise an ABORT occurs (see "SelectMAP ABORT").

On the next rising CCLK edge, the device begins sampling the data pins. Only D[0:7] are sampled by Configuration until the bus width is determined. See "Bus Width Auto Detection" for details. After bus width is determined, the proper width of the data bus is sampled for the Synchronization word search. Configuration begins after the synchronization word is clocked into the device.

After the configuration bitstream is loaded, the device enters the startup sequence. The device asserts its DONE signal High in the phase of the startup sequence that is specified by the bitstream (see "Startup (Step 8)"). The configuration controller should continue sending CCLK pulses until after the startup sequence has finished. (This can require several CCLK pulses after DONE goes High. See "Startup (Step 8)" for details).

After configuration, the CS_B and RDWR_B signals can be deasserted, or they can remain asserted. Because the SelectMAP port is inactive, toggling RDWR_B at this time does not cause an abort. Figure 14 summarizes the timing of SelectMAP configuration with continuous data loading.

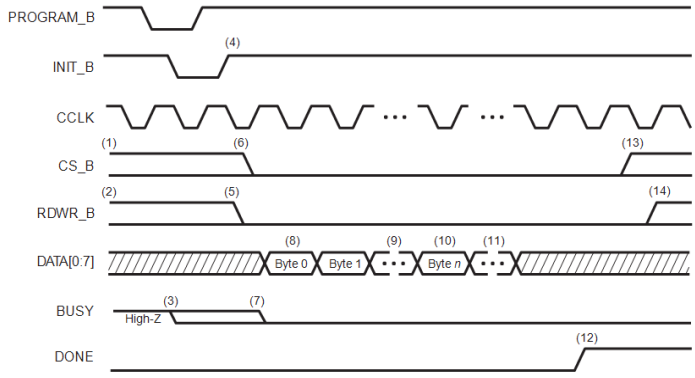



Figure 14:Continuous x8 SelectMAP Data Loading

Notes relevant to Figure 14:

1. CS_B signal can be tied Low if there is only one device on the SelectMAP bus. If CS_B is not tied Low, it can be asserted at any time.
2. RDWR_B can be tied Low if readback is not needed. RDWR_B should not be toggled after CS_B has been asserted because this triggers an ABORT. (See "SelectMAP ABORT").
3. If CS_B is tied Low, BUSY is driven Low before INIT_B toggles High.
4. The Mode pins are sampled when INIT_B goes High.
5. RDWR_B should be asserted before CS_B to avoid causing an abort.
6. CS_B is asserted, enabling the SelectMAP interface.
7. BUSY remains in High-Z state until CS_B is asserted.
8. The first byte is loaded on the first rising CCLK edge after CS_B is asserted.

9. The configuration bitstream is loaded one byte per rising CCLK edge.
10. After the last byte is loaded, the device enters the startup sequence.
11. The startup sequence lasts a minimum of eight CCLK cycles.
12. The DONE pin goes High during the startup sequence. Additional CCLKs can be required to complete the startup sequence. (See “Startup (Step 8)” .)
13. After configuration has finished, the CS_B signal can be deasserted.
14. After the CS_B signal is deasserted, RDWR_B can be deasserted.
15. The data bus can be x8, x16, or x32.

**Non-Continuous SelectMAP Data Loading**

Non-continuous data loading is used in applications where the configuration controller cannot provide an uninterrupted stream of configuration data—for example, if the controller pauses configuration while it fetches additional data.

Configuration can be paused in two ways: by deasserting the CS_B signal (Free-Running CCLK method, Figure 15) or by halting CCLK (Controlled CCLK method, Figure 16).

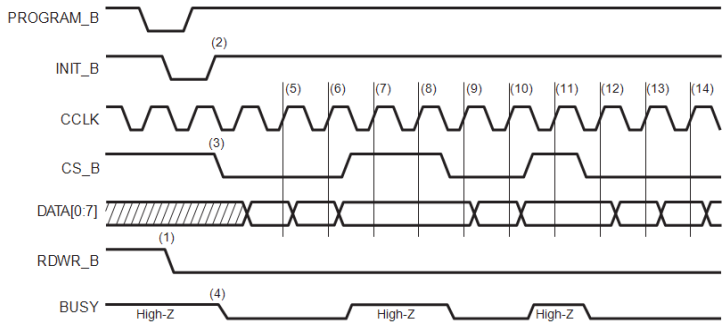



Figure 15:Non-Continuous SelectMAP Data Loading with Free-Running CCLK

Notes relevant to Figure 15:

1. RDWR_B is driven Low by the user, setting the D[0:7] pins as inputs for configuration. RDWR_B can be tied Low if readback is not needed. RDWR_B should not be toggled after CS_B has been asserted because this triggers an ABORT.
2. The device is ready for configuration after INIT_B toggles High.
3. The user asserts CS_B Low, enabling the SelectMAP data bus. CS_B signal can be tied Low if there is only one device on the SelectMAP bus. If CS_B is not tied Low, it can be asserted at any time.
4. BUSY goes Low shortly after CS_B is asserted. If CS_B is tied Low, BUSY is driven Low before INIT_B toggles High.
5. A byte is loaded on the rising CCLK edge. The data bus can be x8, x16, or x32 wide.
6. A byte is loaded on the rising CCLK edge.
7. The user deasserts CS_B, and the byte is ignored.
8. The user deasserts CS_B, and the byte is ignored.
9. A byte is loaded on the rising CCLK edge.
10. A byte is loaded on the rising CCLK edge.
11. The user deasserts CS_B, and the byte is ignored.
12. A byte is loaded on the rising CCLK edge.
13. A byte is loaded on the rising CCLK edge.

14. A byte is loaded on the rising CCLK edge.

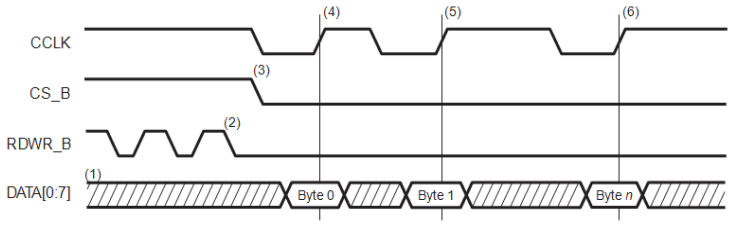



Figure 16: Non-Continuous SelectMAP Data Loading with Controlled CCLK

Notes relevant to Figure 16:

1. The Data pins are in the High-Z state while CS_B is deasserted. The data bus can be x8, x16, or x32.
2. RDWR_B has no effect on the device while CS_B is deasserted.
3. CS_B is asserted by the user. The device begins loading configuration data on rising CCLK edges.
4. A byte is loaded on the rising CCLK edge.
5. A byte is loaded on the rising CCLK edge.
6. A byte is loaded on the rising CCLK edge.

**SelectMAP ABORT**

An ABORT is an interruption in the SelectMAP configuration or readback sequence occurring when the state of RDWR_B changes while CS_B is asserted. During a configuration ABORT, internal status is driven onto the D[7:4] pins over the next four CCLK cycles. The other D pins are always High. After the ABORT sequence finishes, the user can resynchronize the configuration logic and resume configuration. For applications that must deassert RDWR_B between bytes, see Controlled CCLK method, Figure 16.

Configuration Abort Sequence Description

An ABORT is signaled during configuration as follows:

1. The configuration sequence begins normally.
2. The user pulls the RDWR_B pin High while the device is selected (CS_B asserted Low).
3. BUSY goes High if CS_B remains asserted (Low). The FPGA drives the status word onto the data pins if RDWR_B remains set for read control (logic High).
4. The ABORT lasts for four clock cycles, and Status is updated.

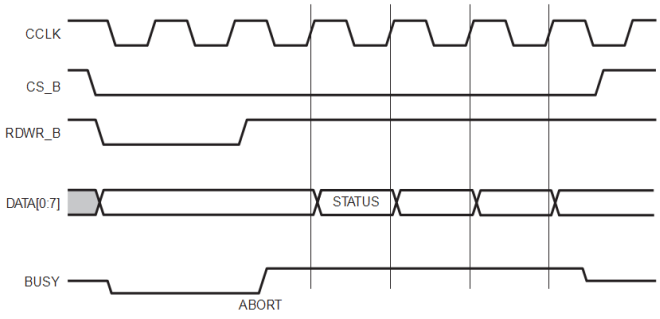


Figure 17:Configuration Abort Sequence for SelectMAP Modes

**Readback Abort Sequence Description**

An ABORT is signaled during readback as follows:

1. The readback sequence begins normally.
2. The user pulls the RDWR_B pin Low while the device is selected (CS_B asserted Low).
3. BUSY goes High if CS_B remains asserted (Low).
4. The ABORT ends when CS_B is deasserted.

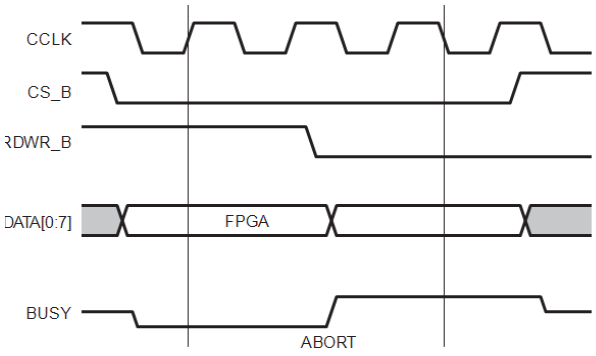



Figure 18:Readback Abort Sequence

ABORTs during readback are not followed by a status word because the RDWR_B signal is set for write control (FPGA D[x:0] pins are inputs).

**ABORT Status Word**

During the configuration ABORT sequence, the device drives a status word onto the D[7:0] pins. The status bits do not bit-swap. The other data pins are always High. The key for that status word is given in Table 6.

Table 6: ABORT Status Word

| Bit Number | Status Bit Name | Meaning |
|---|---|---|
| D7 | CFGERR_B | Configuration error (active Low)<br>0 = A configuration error has occurred.<br>1 = No configuration error. |
| D6 | DALIGN | Sync word received (active High)<br>0 = No sync word received.<br>1 = Sync word received by interface logic. |
| D5 | RIP | Readback in progress (active High)<br>0 = No readback in progress.<br>1 = A readback is in progress. |
| D4 | IN_ABORT_B | ABORT in progress (active Low)<br>0 = Abort is in progress.<br>1 = No abort in progress. |
| D3-D0 | 1111 | Fixed to ones. |

The ABORT sequence lasts four CCLK cycles. During those cycles, the status word changes to reflect data alignment and ABORT status. A typical sequence might be:

11011111 => DALIGN = 1, IN_ABORT_B = 1

11001111 => DALIGN = 1, IN_ABORT_B = 0

10001111 => DALIGN = 0, IN_ABORT_B = 0

10011111 => DALIGN = 0, IN_ABORT_B = 1

After the last cycle, the synchronization word can be reloaded to establish data alignment.

Resuming Configuration or Readback After an Abort

There are two ways to resume configuration or readback after an ABORT:

- The device can be resynchronized after the ABORT completes.
- The device can be reset by pulsing PROGRAM_B Low at any time.

To resynchronize the device, CS_B must be deasserted then reasserted. Configuration or readback can be resumed by sending the last configuration or readback packet that was in progress when the ABORT occurred. Alternatively, configuration or readback can be restarted from the beginning.

**SelectMAP Reconfiguration**

The term reconfiguration refers to reprogramming an FPGA after its DONE pin has gone High. Reconfiguration can be initiated by pulsing the PROGRAM_B pin (this method is identical to configuration) or by resynchronizing the device and sending configuration data.

To reconfigure a device in SelectMAP mode without pulsing PROGRAM_B, the BitGen persist option must be set—otherwise, the DATA pins become user I/O after configuration. The persist option must also be selected for the new bitstream reconfiguring the device. RS[1:0], CSO_B, and A[19:16] pins are not available for User mode when persist is on. Reconfiguration must be enabled in BitGen. By default, the SelectMAP 8 interface (D0–D7) is preserved unless another SelectMAP width has been selected with the CONFIG_MODE constraint.

Reconfiguration begins when the synchronization word is clocked into the SelectMAP port. The remainder of the operation is identical to configuration as described above.

**SelectMAP Data Ordering**

In many cases, SelectMAP configuration is driven by a user application residing on a microprocessor, CPLD, or in some cases another FPGA. In these applications, it is important to understand how the data ordering in the configuration data file corresponds to the data ordering expected by the FPGA.

In SelectMAP x8 mode, configuration data is loaded at one byte per CCLK, with the MSB of each byte presented to the D0 pin. This convention (D0 = MSB, D7 = LSB) differs from many other devices. For x16 and x32 modes, see “Parallel Bus Bit Order.” This convention can be a source of confusion when designing custom configuration solutions. Table 7 shows how to load the hexadecimal value 0xABCD into the SelectMAP data bus.

Table 7: Bit Ordering for SelectMAP 8-Bit Mode

| CCLK Cycle | Hex Equivalent | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0xAB | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 2 | 0xCD | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |

Notes:

1. D[0:7] represent the SelectMAP DATA pins.

Some applications can accommodate the non-conventional data ordering without difficulty. For other applications, it can be more convenient for the source configuration data file to be bit swapped, meaning that the bits in each byte of the data stream are reversed. For these applications, the Xilinx PROM file generation software can generate bit-swapped PROM files (see “Configuration Data File Formats”).

Figure 19 shows the bit ordering for x8, x16, and x32 modes. It also shows the bit ordering for Virtex-4 FPGA x32 mode.

| BQR5V Mode | Pin | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| x32 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| x16 | | | | | | | | | | | | | | | | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| x8 | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Virtex-4 x32 Mode | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Figure 19:Bit Ordering

## 4.3 SPI Configuration Interface

In SPI serial Flash mode, M[2:0]=001. The BQ5V FPGA configures itself from an attached industry-standard SPI serial Flash PROM. Although SPI is a standard four-wire interface, various available SPI Flash memories use different read commands and protocol. Besides M[2:0], FS[2:0] pins are sampled by the INIT_B rising edge to determine the type of read commands used by SPI Flash. For BQ5V FPGA configurations, the default address always starts from 0. Figure 20 shows the SPI related configuration pins, and the standard connection between BQ5V devices and SPI Flash.

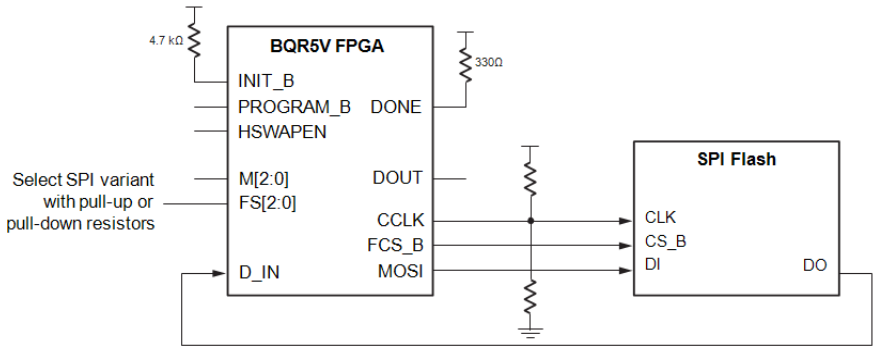



Figure 20:BQ5V Device SPI Configuration Interface

Notes related to Figure 20:

- FCS_B and MOSI are clocked by the CCLK falling edge.
- D_IN is clocked on the rising edge of the CCLK.
- CCLK and D_IN are dedicated Configuration I/Os.
- FCS_B is a dual-mode I/O. MOSI is a dual-mode I/O, muxed with FOE_B. FS[2:0] are dual-mode I/Os sampled on the INIT_B rising edge, muxed with D[2:0].
- The internal I/O pull-up resistors should be enabled for FCS_B, MOSI, and D_IN.
- There are additional pins on the SPI Flash side, such as Write Protect and Hold. These pins are not used in FPGA configuration (read only). But they should be tied off appropriately according to the SPI vendor's specification.
- If HSWAPEN is left unconnected or tied High, a pull-up resistor is required for FCS_B and MOSI.
- If HSWAPEN is tied Low, the FCS_B and MOSI pins have internal weak pull-up resistors during configuration. After configuration, FCS_B and MOSI can be either controlled by I/O in user mode or by enabling a weak pull-up resistor through constraints.
- HSWAPEN must be connected to either disable or enable the pull-up resistors.

- CCLK always has a weak internal pull-up resistor. The CCLK frequency can be adjusted using the ConfigRate BitGen option.
- To enable the active driver on DONE, the DriveDONE option in BitGen must be enabled.
- When DCI match wait or DCM lock wait is enabled before the DONE release cycle during startup, the FPGA continues to clock in data until the startup wait condition is met and DONE is released.

Table 8 describes the SPI configuration interface pins.

Table 8: BQ5V Device SPI Configuration Interface Pins

| Pin Name | Type | Dedicated or Dual-Purpose | Description |
|---|---|---|---|
| M[2:0] | Input | Dedicated | Mode pins – 001 for SPI |
| HSWAPEN | Input | Dedicated | Controls I/O (except bank0 dedicated I/Os) Pull-up during configuration. A weak pull-up resistor is built into this pin.<br>0 = Pull-up during configuration<br>1 = 3-stated during configuration |
| DOUT | Three-State Output | Dedicated | Used for serial daisy chain configuration. |
| DONE | Bidirectional, Open-Drain, or Active | Dedicated | Active-High signal indicating configuration is complete:<br>0 = FPGA not configured<br>1 = FPGA configured |
| INIT_B | Input or Output, Open-Drain | Dedicated | Before the Mode pins are sampled, INIT_B is an input that can be held Low to delay configuration. After the Mode pins are sampled, INIT_B is an open-drain active Low output indicating whether a CRC error occurred during configuration:<br>0 = CRC error<br>1 = No CRC error<br>When the SEU detection function is enabled, INIT_B is optionally driven Low when read back CRC error is detected. |
| PROGRAM_B | Input | Dedicated | Active-Low asynchronous full-chip reset |
| FS[2:0] | Input | Dual-Purpose | SPI Variant Select pins, sampled by the INIT_B rising edge. They are multiplexed with the DATA[2:0] pins. |
| CCLK | Output | Dedicated | Configuration clock output (to SPI). |
| FCS_B | Output | Dual-Purpose | Active-Low chip select output, clocked by the CCLK falling edge. |
| MOSI | Output | Dual-Purpose | FPGA serial data output, clocked by the CCLK falling edge. This pin is multiplexed with the FOE_B pin. |
| D_IN | Input | Dedicated | FPGA serial data input (from SPI), sampled by the CCLK rising edge. |

| | | | |
|---|---|---|---|
| RCMD[7:0] | Input | Dual-Purpose | SPI read command strapping inputs RCMD[7:0] (muxed on ADDR[7:0]) when FS[2:0] = 001. Sampled on the rising edge of INIT_B when used for SPI read command strapping. |

Table 9 defines the SPI read command based on the FS[2:0] settings.

Table 9: BQ5V Device SPI Read Command Variant Select Table

| FS[2:0] | SPI Read Command | Comments |
|---|---|---|
| 000 | 0xFF | |
| 001 | RCMD[7:0] | RCMD[7:0] on ADDR[7:0] are sampled by the INIT_B rising edge, along with M[2:0] and FS[2:0]. RCMD[7:0] can be used to support any SPI read commands not supported here. The timing requirements for FS[2:0] and RCMD[7:0] are the same as for M[2:0]. |
| 010 | 0x52 | |
| 011 | Reserved | |
| 100 | 0x55 | |
| 101 | 0x03 | |
| 110 | 0xE8 | |
| 111 | 0x0B | |

The BQ5V SPI flash timing diagram is shown in Figure 21.

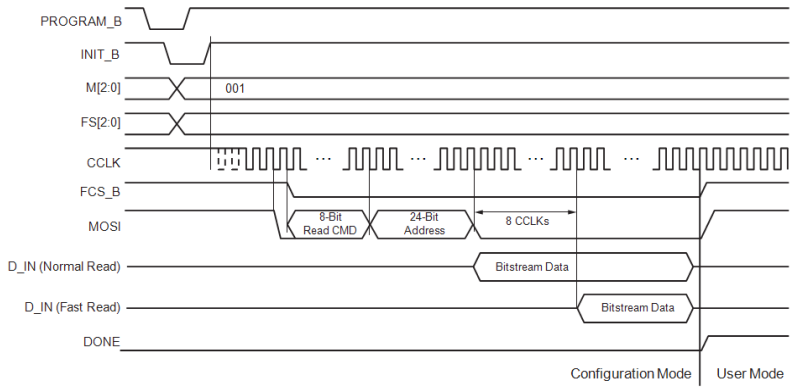



Figure 21: BQ5V Device SPI Flash Timing Diagram

Notes related to Figure 21:

- The BQ5V FPGA stops loading the bitstream after the DONE pin goes High. FCS_B and MOSI can be used as user I/Os.
- FCS_B is either controlled by user logic after configuration or pulled up by a pull-up resistor enabled through constraints.

For supported flash devices, consult the iMPACT help menu indirect programming tables for BQ5V FPGA support. Other flash devices not listed in the help menu can be compatible with BQ5V devices.

**Power-On Sequence Precautions**

At power-on, the FPGA automatically starts its configuration procedure. When the FPGA is in Master SPI configuration mode, the FPGA asserts FCS_B Low to select the SPI Flash and drives a read command to the SPI Flash. The SPI Flash must be awake and ready to receive commands before

the FPGA drives FCS_B Low and sends the read command.

Because different power rails can supply the FPGA and SPI Flash or because the FPGA and SPI flash can respond at different times along the ramp of a shared power supply, special attention to the FPGA and SPI Flash power-on sequence or power-on ramps is essential. The power-on sequence or power supply ramps can cause the FPGA to awake before the SPI Flash or vice versa. In addition, some SPI Flash devices specify a minimum time period, which can be several milliseconds from power-on, during which the device must not be selected. For many systems with near-simultaneous power supply ramps, the FPGA power-on reset time (TPOR) can sufficiently delay the start of the FPGA configuration procedure such that the SPI Flash becomes ready before the start of the FPGA configuration procedure. In general, the system design must consider the affect of the power sequence, the power ramps, FPGA power-on reset timing, and SPI Flash power-up timing on the timing relation between the start of FPGA configuration and the readiness of the SPI Flash.

One of the following system design approaches can ensure that the SPI Flash is ready to receive commands before the FPGA starts its configuration procedure:

- Control the sequence of the power supplies such that the SPI Flash is certain to be powered and ready for asynchronous reads before the FPGA begins its configuration procedure.
- Hold the FPGA PROGRAM_B pin Low from power-up to delay the start of the FPGA configuration procedure and release the PROGRAM_B pin to High after the SPI flash is fully powered and is able to receive commands.
- Hold the FPGA INIT_B pin Low from power-up to delay the start of the FPGA configuration procedure and release the INIT_B pin to High after the SPI flash becomes ready to receive commands.

**SPI Serial Daisy Chain**

In a serial daisy chain application, the leading device can be in SPI mode and all downstream devices in Slave Serial mode. In this case, all configuration bitstreams can be stored inside one SPI device. The bitstream format for master and slave serial daisy chains is exactly the same. See “Serial Daisy Chains” for details.

## 4.4 Byte Peripheral Interface Parallel Flash Mode

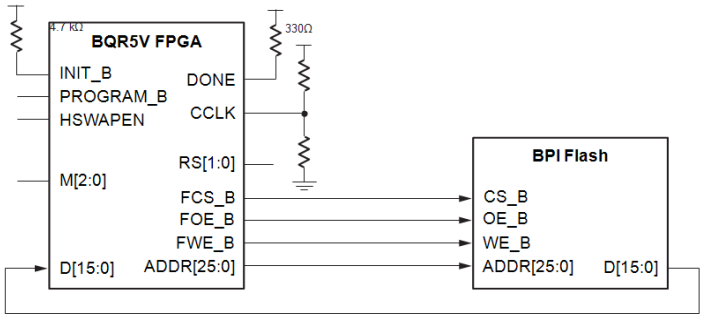
In BPI-Up (M[2:0]=010) or BPI-Down (M[2:0] = 011) mode, the BQ5V FPGA configures itself from an industry-standard parallel NOR Flash PROM, as illustrated in Figure 22. The FPGA drives up to 26 address lines to access the attached parallel Flash. For configuration, only async read mode is used, where the FPGA drives the address bus, and the Flash PROM drives back the bitstream data. Bus widths of x8 and x16 are supported. Bus widths are auto detected, as described in “Bus Width Auto Detection.” Platform Flash XL High-Density Configuration and Storage Device data sheet for the BPI-compatible Flash device from Xilinx.

In BPI modes, the CCLK output is not connected to the BPI Flash device. However, Flash data is still sampled on the rising edge of CCLK. The CCLK output is driven during the BPI modes and therefore must receive the same parallel termination as in the other Master modes. The timing parameters related to BPI use CCLK as a reference. BQ5V BPI modes also support asynchronous page-mode reads to allow an increase in the CCLK frequency. See “Page Mode Support,”.

In the BPI-Up mode, the address starts at 0 and increments by 1 until the DONE pin is asserted. If the address reaches the maximum value (26’h3FFFFFF) and configuration is not done (DONE is not

asserted), an error flag is raised in the status register, and fallback reconfiguration starts.

In the BPI-Down mode, the address start at 26'h3FFFFFF and decrements by 1 until the DONE pin is asserted. If the address reaches the bottom (26'h0), and configuration is still not done (DONE is not asserted), an error flag is raised in the status register and fallback reconfiguration starts.




Note: The BPI Flash vendor data sheet should be referred to for details on the specific Flash signal connectivity.

To prevent address misalignment, close attention should be paid to the Flash family address LSB for the byte/word mode used. Not all Flash families use the A0 as the address LSB.

Figure 22:BQ5V BPI Configuration Interface

Additional notes related to Figure 22:

- M[2:0] = 010 for BPI-Up mode and M[2:0]=011 for BPI-Down mode.
- Figure 22 shows the x16 BPI interface. For x8 BPI interfaces, only D[7:0] are used.See "Bus Width Auto Detection."
- Sending a bitstream to the data pin follows the same bit-swapping rule as in SelectMAP mode. See "Parallel Bus Bit Order."
- If Flash programming is not required, FCS_B, FOE_B, and FWE_B can be tied off; that is, DONE is connected to FCS_B, FOE_B is tied Low, and FWE_B is tied High.
- The CCLK outputs are not used to connect to Flash but are used to sample Flash read data during configuration. All timings are referenced to CCLK. The CCLK pin must not be driven or tied High or Low.
- The RS[1:0] pins are not connected as shown in Figure 22.
- HSWAPEN must be connected to either disable or enable the pull-up resistors.
- If HSWAPEN is left unconnected or tied High, a pull-up resistor is required for FCS_B.
- If HSWAPEN is tied Low, the FCB_B, FOE_B, FWE_B, and the address pins have internal weak pull-up resistors during configuration. After configuration, FCS_B can be either controlled by I/O in user mode or by enabling a weak pull-up resistor through constraints.
- To enable the active driver on DONE, the DriveDONE option in BitGen must be enabled.
- For daisy chaining FPGAs in BPI mode, see Figure 12.
- The BPI Flash vendor data sheet should be referred to for details on the specific Flash signal connectivity. To prevent address misalignment, close attention should be paid to the Flash family address LSB for the byte/word mode used. Not all Flash families use the A0 as the address LSB.

Table 10 defines the BPI configuration interface pins.

If the FPGA is subject to reprogramming or fallback during configuration from the BPI flash, then the INIT pin can be connected to the BPI reset to set the BPI into a known state.

Table 10: BQ5V Device BPI Configuration Interface Pins

| | | | |
|---|---|---|---|

| | | | |
|---|---|---|---|
| M[2:0] | Input | Dedicated | The Mode pins determine the BPI mode:<br>010=BPI-Up mode<br>011=BPI-Down mode |
| HSWAPEN | Input | Dedicated | Controls I/O (except Bank 0 dedicated I/Os) pull-up resistors during configuration. This pin has a built-in weak pull-up resistor.<br>0 = Pull-up during configuration<br>1 = 3-state during configuration |
| DONE | Bidirectional, Open-Drain, or Active | Dedicated | Active-High signal indicating configuration is complete:<br>0 = FPGA not configured<br>1=FPGA configured |
| INIT_B | Input or Output, Open-Drai n | Dedicated | Before the Mode pins are sampled, INIT_B is an input that can be held Low to delay configuration. After the Mode pins are sampled, INIT_B is an open-drain, active-Low output indicating whether a CRC error occurred during configuration:<br>0 = CRC error<br>1 = No CRC error<br>When the SEU detection function is enabled, INIT_B is optionally driven Low when a read back CRC error is detected. |
| PROGRAM_B | Input | Dedicated | Active-Low asynchronous full-chip reset |
| CCLK | Output | Dedicated | Configuration clock output. CCLK does not directly connect to BPI Flash but is used internally to generate the address and sample read data. |
| FCS_B | Output | Dual | Active-Low Flash chip select output. This output is actively driven Low during configuration and 3-stated after configuration. It has a weak pull-up resistor during configuration. By default, this signal has a weak pull-down resistor after configuration. |
| FOE_B | Output | Dual | Active-Low Flash output enable. This output is actively driven Low during configuration and 3-stated after configuration. It has a weak pull-up resistor during configuration. By default, this signal has a weak pull-down resistor after configuration. |
| FWE_B | Output | Dual | Active-Low Flash write enable. This output is actively driven High during configuration and 3-stated after configuration. It has a |

| | | | |
|---|---|---|---|
| | | | weak pull-up resistor during configuration. By default, this signal has a weak pull-down resistor after configuration. |
| ADDR[25:0] | Output | Dual | Address output. For I/O bank locations. |
| D[15:0] | Input | Dual | Data input, sampled by the rising edge of the FPGA CCLK. For I/O bank location. |
| RS[1:0] | Output | Dual | Revision Select pins. Not used for typical single bitstream applications. RS[1:0] are 3-stated and pulled up with weak resistors during the initial configuration if the HSWAP pin enables the pull ups. If pull ups are disabled, then a weak external pull up is required (after power-up or assertion of PROGRAM_B). RS[1:0] are actively driven Low to load the fallback bitstream when a configuration error is detected. RS[1:0] can also be controlled by the user through the bitstream or ICAP. |
| CSO_B | Output | Dual | Parallel daisy chain active-Low chip select output. Not used in single FPGA applications. |

Figure 23 shows the BPI-Up configuration waveforms.

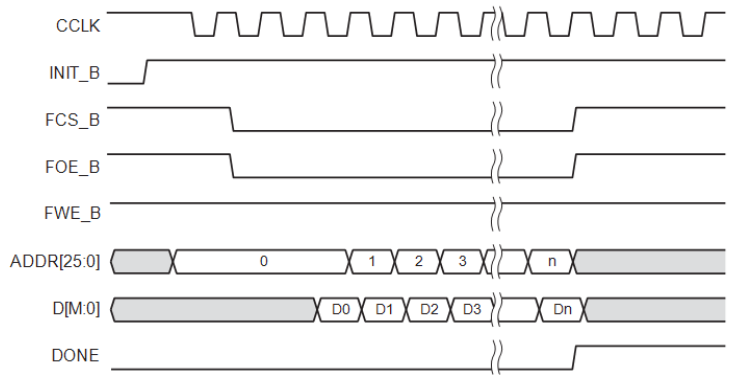



Figure 23:BQ5V Device BPI-Up Configuration Waveforms

Notes related to Figure 23:

- CCLK is output in BPI modes. The BPI Flash does not require CCLK, but the BQ5V FPGA uses the rising edge of CCLK to sample D[max:0] pins.
- The BQ5V FPGA stops loading the bitstream after the DONE pin goes High.
- Dual-mode configuration I/O switches to User mode after the GTS_cycle. By default, this is one cycle after DONE goes High.
- M can be 7 or 15.
- FCS_B, FOE_B, and FWE_B should have weak pull-ups after configuration through either I/O constraints or external pull-up resistors.
- The first address 0 for BPI-Up is extended for multiple cycles due to the initial latency.

**Power-On Sequence Precautions**

At power-on, the FPGA automatically starts its configuration procedure. When the FPGA is in a Master-BPI configuration mode, the FPGA asserts FCS_B Low and drives a sequence of addresses to read the bitstream from a BPI Flash. The BPI Flash must be ready for asynchronous reads before the FPGA drives FCS_B Low and outputs the first address to ensure the BPI Flash can output the stored bitstream.

Because different power rails can supply the FPGA and BPI Flash or because the FPGA and BPI flash can respond at different times along the ramp of a shared power supply, special attention to the FPGA and BPI Flash power-on sequence or power-on ramps is essential. The power-on sequence or power supply ramps can cause the FPGA to awake before the BPI Flash or vice versa. For many systems with near-simultaneous power supply ramps, the FPGA power-on reset time (TPOR) can sufficiently delay the start of the FPGA configuration procedure such that the BPI Flash becomes ready before the start of the FPGA configuration procedure. In general, the system design must consider the effect of the power sequence, the power ramps, FPGA power-on reset time, and BPI Flash power-on reset time on the timing relation between the start of FPGA configuration and the readiness of the BPI Flash for asynchronous reads.

One of the following system design approaches can ensure that the BPI Flash is ready for asynchronous reads before the FPGA starts its configuration procedure:

- Control the sequence of the power supplies such that the BPI Flash is certain to be powered and ready for asynchronous reads before the FPGA begins its configuration procedure.
- Hold the FPGA PROGRAM_B pin Low from power-up to delay the start of the FPGA configuration procedure and release the PROGRAM_B pin to High after the BPI flash is fully powered and is able to perform asynchronous reads.
- Hold the FPGA INIT_B pin Low from power-up to delay the start of the FPGA configuration procedure and release the INIT_B pin to High after the BPI flash becomes ready for asynchronous reads.

See the Power-On Precautions if 3.3V Supply is Last in Sequence subsection of the Master BPI Mode section in Xillinx UG332, Spartan-3 Generation Configuration User Guide, for reference.

**Page Mode Support**

Many NOR Flash devices support asynchronous page reads. The first access to a page usually takes the longest time (~100 ns), subsequent accesses to the same page take less time (~25 ns). The following parameters are bitstream programmable in BQ5V devices to take advantage of page reads and maximize the CCLK frequency:

- Page sizes of 1 (default), 4, or 8.

If the actual Flash page size is larger then 8, the value of 8 should be used to maximize the efficiency.

- First access CCLK cycles of 1 (default), 2, 3, or 4. CCLK cycles must be 1 if the page size is 1.
- CCLK frequency

The sequence of page-mode operation is controlled by the BQ5V bitstream. After an FPGA reset, the default page size is 1, the first access CCLK is 1, and the master CCLK is running at slowest default frequency. The COR0 register contains master CCLK frequency control bits (see “Configuration Options Register 0 (COR0)”. The COR1 register contains BPI flash page mode

control bits (see “Configuration Options Register 1 (COR1)”). After the COR1 register is programmed, the BPI address timing switches at the page boundary as shown in Figure 24. When the SWITCH command is received, the master CCLK switches to a user- desired frequency, using it to load the rest of the configuration.

Refer to the “BitGen” section of the Development System Reference Guide for details on BitGen options.

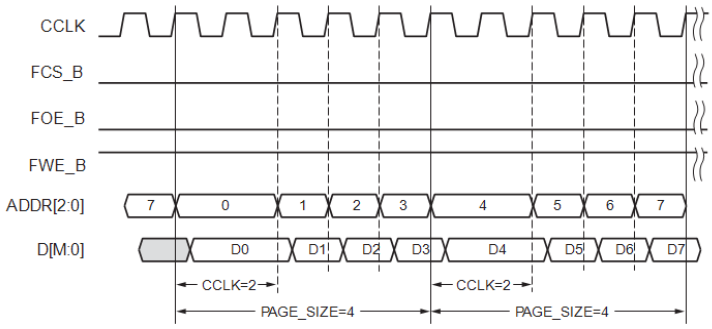



Figure 24: BPI-Up Waveforms (Page Size = 4 and First Access CCLK = 2)

Notes related to Figure 24:

- Figure 24 shows BPI-Up mode, a page size of 4, and a first access CCLK of 2.
- M can be 7 or 15.
- For BPI-Down mode, the ADDR[25:0] bus is extended for the desired CCLK cycles when ADDR[1:0]= 2’b11 for a page size of 4.

For supported flash devices, consult the iMPACT help menu indirect programming tables for BQ5V FPGA support. Other flash devices not listed in the help menu can be compatible with BQ5V devices.

# 5. Electrical Characteristics

BQ5V DC and AC characteristics are specified for military and space grade.All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

## 5.1 DC Characteristics

Table 11 Absolute Maximum Ratings

| Symbol | Description | | Units |
|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND | –0.5 to 1.1 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | –0.5 to 3.0 | V |
| VCCO | Output drivers supply voltage relative to GND | –0.5 to 3.75 | V |
| $V_{BATT}$ | Key memory battery backup supply | –0.5 to 4.05 | V |
| VREF | Input reference voltage | –0.5 to 3.75 | V |

| Symbol | Description | | Units |
|---|---|---|---|
| $V_{IN}$[2] | 3.3V I/O input voltage relative to GND (user and dedicated I/Os) | –0.75 to 4.05 | V |
| | 3.3V I/O input voltage relative to GND (restricted to maximum of 100 user I/Os) [3] | –0.95 to 4.4 (Commercial Temperature) | V |
| | | V–0.85 to 4.3 (Industrial Temperature) | |
| | 2.5V or below I/O input voltage relative to GND (user and dedicated I/Os) | –0.75 to VCCO +0.5 | V |
| $I_{IN}$ | Current applied to an I/O pin, powered or unpowered | ±100 | mA |
| | Total current applied to all I/O pins, powered or unpowered | ±100 | mA |
| $V_{TS}$ | Voltage applied to 3-state 3.3V output (user and dedicated I/Os) | –0.75 to 4.05 | V |
| | Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os) | –0.75 to VCCO +0.5 | V |
| $T_{STG}$ | Storage temperature (ambient) | –65 to 150 | ℃ |
| TSOL | Maximum soldering temperature | 220 | ℃ |
| $T_J$ | Maximum junction temperature | 125 | ℃ |

**Notes:**

1.Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

2. 3.3V I/O absolute maximum limit applied to DC and AC signals.

3. For more flexibility in specific designs, a maximum of 100 user I/Os can be stressed beyond the normal specification for no more than 20% of a data period.

Table 12 :Recommended Operating Conditions

| Symbol | Description | Temperature Range | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND, TJ =0 ℃ to +85 ℃ | Commercial | 0.95 | 1.05 | V |
| | Internal supply voltage relative to GND, TJ = –40 ℃ to +100 ℃ | Industrial | 0.95 | 1.05 | V |
| $V_{CCAUX}$[1] | Auxiliary supply voltage relative to GND, TJ =0 ℃ to +85 ℃ | Commercial | 2.375 | 2.625 | V |
| | Auxiliary supply voltage relative | Industrial | 2.37 | 2.62 | V |

| Symbol | Description | Temperature Range | Min | Max | Units |
|---|---|---|---|---|---|
| | to GND, TJ =–40 ℃ to +100 ℃ | | 5 | 5 | |
| $V_{CCO}$(2,4,5) | Supply voltage relative to GND, TJ =0 ℃ to +85 ℃ | Commercial | 1.14 | 3.45 | V |
| | Supply voltage relative to GND, TJ =–40 ℃ to +100 ℃ | Industrial | 1.14 | 3.45 | V |
| $V_{IN}$ | 3.3V supply voltage relative to GND, TJ =0 ℃ to +85 ℃ | Commercial | GND – 0.20 | 3.45 | V |
| | 3.3V supply voltage relative to GND, TJ = –40 ℃ to +100 ℃ | Industrial | GND – 0.20 | 3.45 | V |
| | 2.5V and below supply voltage relative to GND, TJ =0 ℃ to +85 ℃ | Commercial | GND – 0.20 V | VCCO +0 | V |
| | 2.5V and below supply voltage relative to GND, TJ = –40 ℃ to +100 ℃ | Industrial | GND – 0.20 V | VCCO +0 | V |
| $I_{IN}$(6) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode | Commercial | | 10 | mA |
| | | Industrial | | 10 | mA |
| $V_{BATT}$(3) | Battery voltage relative to GND, TJ =0 ℃ to +85 ℃ | Commercial | 1 | 3.6 | V |
| | Battery voltage relative to GND, TJ =–40 ℃ to +100 ℃ | Industrial | 1 | 3.6 | V |

**Notes:**

1. Recommended maximum voltage drop for VCCAUX is 10 mV/ms.
2. Configuration data is retained even if VCCO drops to 0V.
3. VBATT is required only when using bitstream encryption. If battery is not used, connect VBATT to either ground or VCCAUX.
4. Includes VCCO of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The configuration supply voltage VCC_CONFIG is also known as VCCO_0.
6. A total of 100 mA per bank should not be exceeded.

Table 13 DC Characteristics Over Recommended Operating Conditions

| Symbol | Description | Data Rate | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | | 0.75 | | | V |
| $V_{DRI}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | | 2.0 | | | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin | | | | 10 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) | | | | 10 | µA |
| $C_{IN}$ | Input capacitance (sample-tested) | | | | 8 | pF |
| $I_{RPU}$(1) | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V | | 20 | | 150 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | | 10 | | 90 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | | 5 | | 45 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | | 3 | | 30 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | | 2 | | 15 | µA |
| $I_{RPD}$(1) | Pad pull-down (when selected) @ $V_{IN}$ = 2.5V | | 5 | | 110 | µA |
| $I_{BATT}$(2) | Battery supply current | | | | 150 | nA |
| n | Temperature diode ideality factor | | | 1.0002 | | n |
| r | Series resistance | | | 5.0 | | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25 ℃.
2. Maximum value specified for worst case process at 25 ℃.

## 5.2 Power-On Power Supply Requirements

BQ5V FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The power supplies can be turned on in any sequence, though the specifications shown in Table 15 are for the recommended power-on sequence of VCCINT, VCCAUX, and VCCO. The I/O will remain 3-stated through power-on if the recommended power-on sequence is followed. Xilinx does not specify the current or I/O behavior for other power-on sequences.

Table 15 shows the minimum current required by BQ5V devices for proper power-on and configuration.If the current minimums shown in Table 15 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.The FPGA must be configured after VCCINT is applied.Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 15 Power On Current for BQ5V Devices

| Device | ICCINTMIN | ICCAUXMIN | ICCOMIN | Units |
|---|---|---|---|---|
| | Typ(1) | Typ(1) | Typ(1) | |
| XC5VSX35T | 307 | 98 | 50 | mA |
| XC5VSX50T | 472 | 148 | 50 | mA |
| XC5VSX95T | 804 | 262 | 100 | mA |

| Device | ICCINTMIN | ICCAUXMIN | ICCOMIN | Units |
|---|---|---|---|---|
| | Typ(1) | Typ(1) | Typ(1) | |
| XC5VSX240T | 1632 | 662 | 150 | mA |
| XC5VLX155T | 728 | 368 | 100 | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 25℃.

2. The maximum startup current can be obtained using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools and adding the quiescent plus dynamic current consumption.

Table 16 Power Supply Ramp Time

| Symbol | Description | Ramp Time | Units |
|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND | 0.20 to 50.0 | ms |
| $V_{CCO}$ | Output drivers supply voltage relative to GND | 0.20 to 50.0 | ms |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | 0.20 to 50.0 | ms |

## 5.3 SelectIO™ DC Input and Output Levels

Values for VIL and VIH are recommended input voltages. Values for IOL and IOH are guaranteed over the recommended operating conditions at the VOL and VOH test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum VCCO with the respective VOL and VOH voltage levels shown. Other standards are sample tested.

Table 17 Power Supply Ramp Time

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVTTL | –0.3 | 0.8 | 2.0 | 3.45 | 0.4 | 2.4 | Note(3) | Note(3) |
| LVCMOS33, LVDCI33 | –0.3 | 0.8 | 2.0 | 3.45 | 0.4 | $V_{CCO}$ – 0.4 | Note(3) | Note(3) |
| LVCMOS25, LVDCI25 | –0.3 | 0.7 | 1.7 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | Note(3) | Note(3) |
| LVCMOS18, LVDCI18 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 0.45 | $V_{CCO}$ – 0.45 | Note(4) | Note(4) |
| LVCMOS15, LVDCI15 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note(4) | Note(4) |
| LVCMOS12 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note(6) | Note(6) |
| PCI33_3(5) | –0.2 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note(5) | Note(5) |
| PCI66_3(5) | –0.2 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note(5) | Note(5) |
| PCI-X(5) | –0.2 | 35% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note(5) | Note(5) |
| GTLP | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | – | 0.6 | N/A | 36 | N/A |
| GTL | –0.3 | $V_{REF}$ – 0.05 | $V_{REF}$ + 0.05 | – | 0.4 | N/A | 32 | N/A |
| HSTL I_12 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | 6.3 | 6.3 |
| HSTL I(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 8 | –8 |
| HSTL II(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 16 | –16 |
| HSTL III(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 24 | –8 |
| HSTL IV(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 48 | –8 |
| DIFF HSTL I(2) | –0.3 | 50% $V_{CCO}$ – 0.1 | 50% $V_{CCO}$ + 0.1 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF HSTL II(2) | –0.3 | 50% $V_{CCO}$ – 0.1 | 50% $V_{CCO}$ + 0.1 | $V_{CCO}$ + 0.3 | – | – | – | – |
| SSTL2 I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.61 | $V_{TT}$ + 0.61 | 8.1 | –8.1 |
| SSTL2 II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| DIFF SSTL2 I | –0.3 | 50% $V_{CCO}$ – 0.15 | 50% $V_{CCO}$ + 0.15 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF SSTL2 II | –0.3 | 50% $V_{CCO}$ – 0.15 | 50% $V_{CCO}$ + 0.15 | $V_{CCO}$ + 0.3 | – | – | – | – |
| SSTL18 I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.47 | $V_{TT}$ + 0.47 | 6.7 | –6.7 |
| SSTL18 II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.60 | $V_{TT}$ + 0.60 | 13.4 | –13.4 |
| DIFF SSTL18 I | –0.3 | 50% $V_{CCO}$ – 0.125 | 50% $V_{CCO}$ + 0.125 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF SSTL18 II | –0.3 | 50% $V_{CCO}$ – 0.125 | 50% $V_{CCO}$ + 0.125 | $V_{CCO}$ + 0.3 | – | – | – | – |

**Notes:**

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. For more information on PCI33_3, PCI66_3, and PCI-X, refer to 3.3V I/O Design Guidelines.
6. Supported drive strengths of 2, 4, 6, or 8 mA.

## 5.4 HT DC Specifications (HT_25)

Table 18 HT DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OD}$ | Differential Output Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 495 | 600 | 715 | mV |
| Δ $V_{OD}$ | Change in $V_{OD}$ Magnitude | | –15 | | 15 | mV |
| $V_{OCM}$ | Output Common Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 495 | 600 | 715 | mV |
| Δ $V_{OCM}$ | Change in $V_{OCM}$ Magnitude | | –15 | | 15 | mV |
| $V_{ID}$ | Input Differential Voltage | | 200 | 600 | 1000 | mV |
| Δ $V_{ID}$ | Change in $V_{ID}$ Magnitude | | –15 | | 15 | mV |
| $V_{ICM}$ | Input Common Mode Voltage | | 440 | 600 | 780 | mV |
| Δ $V_{ICM}$ | Change in $V_{ICM}$ Magnitude | | –15 | | 15 | mV |

## 5.5 LVDS DC Specifications (LVDS_25)

Table 19 LVDS DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | | | 1.675 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.825 | | | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.125 | 1.250 | 1.375 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | | 0.3 | 1.2 | 2.2 | V |

## 5.6 Extended LVDS DC Specifications (LVDSEXT_25)

Table 20 Extended LVDS DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | | – | 1.785 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.715 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 350 | – | 820 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.125 | 1.250 | 1.375 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | Common-mode input voltage = 1.25V | 100 | – | 1000 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | Differential input voltage = ±350 mV | 0.3 | 1.2 | 2.2 | V |

## 5.7 LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The VOH levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 21 summarizes the DC output specifications of LVPECL.

Table 21 LVPECL DC Specifications

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $V_{CC}$ – 1.025 | 1.545 | $V_{CC}$ – 0.88 | V |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$ – 1.81 | 0.795 | $V_{CC}$ – 1.62 | V |
| $V_{ICM}$ | Input Common-Mode Voltage | 0.6 | | 2.2 | V |
| $V_{IDIFF}$ | Differential Input Voltage[1,2] | 0.100 | | 1.5 | V |

**Notes:**

1. Recommended input maximum voltage not to exceed VCCO +0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

# 6. Pin Definitions

Table 22 provides a description of each pin type listed in BQ5V pinout tables.

Table 22 BQ5V Pin Definitions

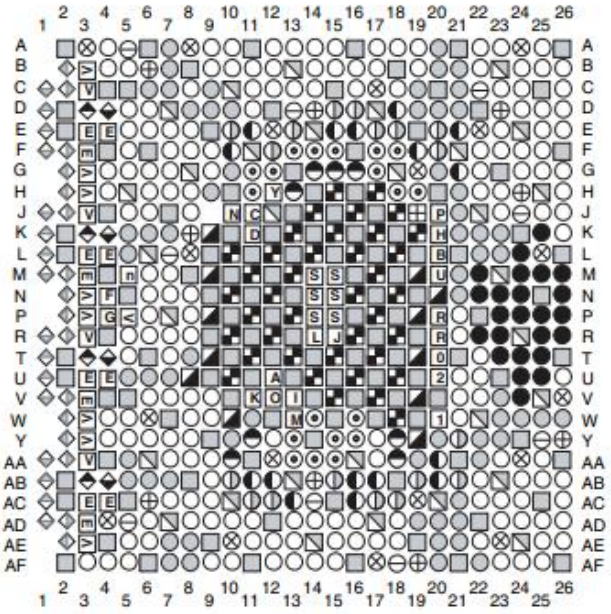
| Pin Name | Direction | Description |
|---|---|---|
| **User I/O Pins** | | |
| IO_LXXY_# | Input/ Output | All user I/O pins are capable of differential signaling and can implement pairs. Each user I/O is labeled "**IO_LXXY_#**", where:<br>**IO** indicates a user I/O pin.<br>**LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = [P\|N]** for the positive/negative sides of the differential pair. |
| **Multi-Function Pins** | | |
| IO_LXXY_ZZZ_# | | Multi-function pins are labelled "**IO_LXXY_ZZZ_#**", where **ZZZ** represents one or more of the following functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O. |
| Dn | Input | In SelectMAP mode, D0 through D31 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. |
| ADDRn | Output | ADDR0–ADDR25 BPI address output. These pins become user I/O after configuration. |
| RSn | Output | RS0 and RS1 revision select output. |
| FCS_B | Output | BPI and SPI flash chip select. |
| FOE_B | Output | BPI flash output enable. |
| FWE_B | Output | BPI flash write enable. |
| MOSI | Output | SPI flash data output enable. |
| CSO_B | Output | Parallel daisy chain chip select. |
| FSn | Input | FS0–FS2 SPI Flash vendor selection. |
| CC | Input | These clock pins connect to Clock Capable I/Os. These pins become regular user I/Os when not needed for clocks. If a single-ended clock is connected to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. Clock capable I/Os in the center column can not drive BUFRs. |
| GC | Input | These clock pins connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks. If a single-ended clock is connected to the differential GC pair of pins, it must be connected to the positive (P) side of the pair. |
| SMnP/SMnN | Input | System Monitor analog inputs. |
| VREF | N/A | These are input threshold voltage pins. They become user |

| | | |
|---|---|---|
| | | I/Os when an external threshold voltage is not needed (per bank). |
| VRN | N/A | This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor). |
| VRP | N/A | This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor). |
| **Dedicated Configuration Pins** | | |
| CCLK_0 | Input/ Output | Configuration clock. Output and input in Master mode or Input in Slave mode. |
| CS_B_0 | Input | In SelectMAP mode, this is the active-low Chip Select signal. |
| D_IN_0 | Input | In bit-serial modes, D_IN is the single-data input. |
| DONE_0 | Input/ Output | DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence. |
| D_OUT_BUSY_0 | Output | In SelectMAP mode, BUSY controls the rate at which configuration data is loaded.<br>In bit-serial modes, DOUT gives preamble and configuration data to down- stream devices in a daisy chain. |
| HSWAPEN_0 | Input | Enable I/O pullups during configuration |
| INIT_B_0 | Bidirectional (open-drain) | When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. |
| M0_0, M1_0, M2_0 | Input | Configuration mode selection |
| PROGRAM_B | Input | Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor. |
| RDWR_B_0 | Input | In SelectMAP mode, this is the active-low Write Enable signal. |
| TCK_0 | Input | Boundary-Scan Clock. |
| TDI_0 | Input | Boundary-Scan Data Input. |
| TDO_0 | Output | Boundary-Scan Data Output. |
| TMS_0 | Input | Boundary-Scan Mode Select. |
| DXP_0, DXN_0 | N/A | Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). |
| **Reserved Pins** | | |
| RSVD | N/A | Reserved pins—must be tied to ground. |
| FLOAT | N/A | Do not connect this pin to the board. Leave floating. |
| **Other Pins** | | |

| | | |
|---|---|---|
| GND | N/A | Ground. |
| VBATT_0 | N/A | Decryptor key memory backup supply; this pin should be tied to VCC or GND. |
| VCCAUX | N/A | Power-supply pins for auxiliary circuits. |
| VCCINT | N/A | Power-supply pins for the internal core logic. |
| VCCO_# | N/A | Power-supply pins for the output drivers (per bank). |
| **Dedicated System Monitor Pins** | | |
| AVDD_0 | N/A | System Monitor's ADC analog positive supply voltage. |
| AVSS_0 | N/A | System Monitor's ADC analog ground reference. |
| VP_0 | Input | System Monitor dedicated differential analog input (positive side). |
| VN_0 | Input | System Monitor dedicated differential analog input (negative side). |
| VREFP_0 | N/A | External System Monitor 2.5V positive reference voltage. |
| VREFN_ 0 | N/A | External System Monitor 2.5V ground reference voltage. |
| **RocketIO Serial Transceiver Pins (GTP_DUAL or GTX_DUAL)** | | |
| MGTAVCC | N/A | Power-supply pin for transceiver mixed-signal circuitry. |
| MGTAVCCPLL | N/A | Power-supply pin for PLL. |
| MGTAVTTRX | N/A | Power-supply pin for RX circuitry. |
| MGTAVTTRXC | N/A | Power-supply pin for the resistor calibration circuit. |
| MGTAVTTTX | N/A | Power-supply pin for TX circuitry. |
| MGTREFCLKP | Input | Positive differential reference clock. |
| MGTREFCLKN | Input | Negative differential reference clock (negative). |
| MGTRREF | Input | Precision reference resistor pin for internal calibration termination. |
| MGTRXP | Input | Positive differential receive port. |
| MGTRXN | Input | Negative differential receive port. |
| MGTTXP | Output | Positive differential transmit port. |
| MGTTXN | Output | Negative differential transmit port. |

# Appendix I Pinout Information and Package

As shown in Table 23, the BQ5VSX35T device is available in the BGA665 packages.



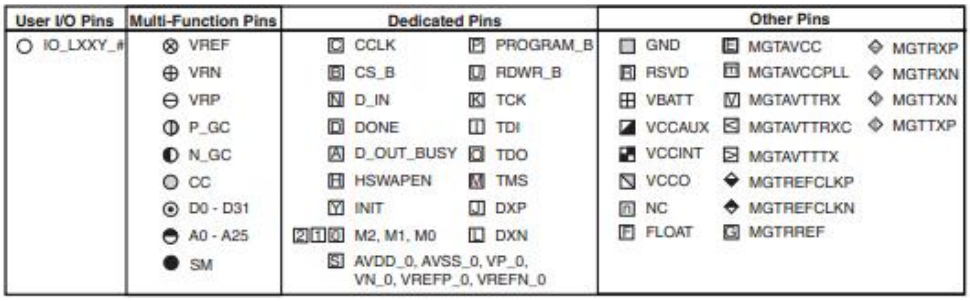



Table 23 BQ5VSX35T packages

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 0 | DXP_0 | R15 | 13 | IO_L17N_13 | U22 | NA | MGTTXN1_118 | AD2 |
| 0 | DXN_0 | R14 | 13 | IO_L18P_13 | U21 | NA | MGTAVTTTX_118 | AE3 |
| 0 | AVDD_0 | M15 | 13 | IO_L18N_13 | V22 | NA | MGTTXP1_118 | AE2 |
| 0 | AVSS_0 | M14 | 13 | IO_L19P_13 | V21 | NA | GND | A2 |
| 0 | VP_0 | N15 | 13 | IO_L19N_13 | W21 | NA | GND | D2 |
| 0 | VN_0 | P14 | 15 | IO_L0P_15 | C13 | NA | GND | E2 |
| 0 | VREFP_0 | P15 | 15 | IO_L0N_15 | C14 | NA | GND | K2 |
| 0 | VREFN_0 | N14 | 15 | IO_L1P_15 | B14 | NA | GND | L2 |
| 0 | VBATT_0 | J19 | 15 | IO_L1N_15 | A13 | NA | GND | T2 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 0 | PROGRAM_B_0 | J20 | 15 | IO_L2P_15 | A14 | NA | GND | U2 |
| 0 | HSWAPEN_0 | K20 | 15 | IO_L2N_15 | A15 | NA | GND | AB2 |
| 0 | D_IN_0 | J10 | 15 | IO_L3P_15 | B15 | NA | GND | AC2 |
| 0 | DONE_0 | K11 | 15 | IO_L3N_15 | C16 | NA | GND | AF2 |
| 0 | CCLK_0 | J11 | 15 | IO_L4P_15 | B16 | NA | GND | C4 |
| 0 | INIT_B_0 | H12 | 15 | IO_L4N_VREF_15 | C17 | NA | GND | F4 |
| 0 | CS_B_0 | L20 | 15 | IO_L5P_15 | B17 | NA | GND | J4 |
| 0 | RDWR_B_0 | M20 | 15 | IO_L5N_15 | A17 | NA | GND | M4 |
| 0 | RSVD(3) | P20 | 15 | IO_L6P_15 | A18 | NA | GND | R4 |
| 0 | RSVD(3) | R20 | 15 | IO_L6N_15 | A19 | NA | GND | V4 |
| 0 | TCK_0 | V11 | 15 | IO_L7P_15 | B19 | NA | GND | AA4 |
| 0 | M0_0 | T20 | 15 | IO_L7N_15 | C18 | NA | GND | AE4 |
| 0 | M2_0 | U20 | 15 | IO_L8P_CC_15 | A20 | NA | GND | C5 |
| 0 | M1_0 | W20 | 15 | IO_L8N_CC_15 | B20 | NA | GND | N5 |
| 0 | TMS_0 | W13 | 15 | IO_L9P_CC_15 | C19 | NA | GND | V5 |
| 0 | TDI_0 | V13 | 15 | IO_L9N_CC_15 | D19 | NA | GND | AC5 |
| 0 | D_OUT_BUSY_0 | U12 | 15 | IO_L10P_CC_15 | D21 | NA | GND | A6 |
| 0 | TDO_0 | V12 | 15 | IO_L10N_CC_15 | D20 | NA | GND | F6 |
| 1 | IO_L0P_A19_1 | G15 | 15 | IO_L11P_CC_15 | B21 | NA | GND | T6 |
| 1 | IO_L0N_A18_1 | G16 | 15 | IO_L11N_CC_15 | C21 | NA | GND | AF6 |
| 1 | IO_L1P_A17_1 | H13 | 15 | IO_L12P_VRN_15 | D23 | NA | GND | J7 |
| 1 | IO_L1N_A16_1 | G14 | 15 | IO_L12N_VRP_15 | C22 | NA | GND | W7 |
| 1 | IO_L2P_A15_D31_1 | G17 | 15 | IO_L13P_15 | B22 | NA | GND | B8 |
| 1 | IO_L2N_A14_D30_1 | F17 | 15 | IO_L13N_15 | A22 | NA | GND | M8 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 1 | IO_L3P_A13_D29_1 | F15 | 15 | IO_L14P_15 | A23 | NA | GND | AB8 |
| 1 | IO_L3N_A12_D28_1 | F14 | 15 | IO_L14N_VREF_15 | A24 | NA | GND | E9 |
| 1 | IO_L4P_A11_D27_1 | F18 | 15 | IO_L15P_15 | B24 | NA | GND | L9 |
| 1 | IO_L4N_VREF_A10_D26_1 | G19 | 15 | IO_L15N_15 | C23 | NA | GND | N9 |
| 1 | IO_L5P_A9_D25_1 | F13 | 15 | IO_L16P_15 | D24 | NA | GND | R9 |
| 1 | IO_L5N_A8_D24_1 | G12 | 15 | IO_L16N_15 | C24 | NA | GND | U9 |
| 1 | IO_L6P_A7_D23_1 | H18 | 15 | IO_L17P_15 | B25 | NA | GND | Y9 |
| 1 | IO_L6N_A6_D22_1 | H19 | 15 | IO_L17N_15 | A25 | NA | GND | AE9 |
| 1 | IO_L7P_A5_D21_1 | G11 | 15 | IO_L18P_15 | B26 | NA | GND | H10 |
| 1 | IO_L7N_A4_D20_1 | H11 | 15 | IO_L18N_15 | C26 | NA | GND | K10 |
| 1 | IO_L8P_CC_A3_D19_1 | G20 | 15 | IO_L19P_15 | D26 | NA | GND | M10 |
| 1 | IO_L8N_CC_A2_D18_1 | H21 | 15 | IO_L19N_15 | D25 | NA | GND | P10 |
| 1 | IO_L9P_CC_A1_D17_1 | G10 | 16 | IO_L0P_16 | H7 | NA | GND | T10 |
| 1 | IO_L9N_CC_A0_D16_1 | H9 | 16 | IO_L0N_16 | G7 | NA | GND | V10 |
| 2 | IO_L0P_CC_RS1_2 | W11 | 16 | IO_L1P_16 | F7 | NA | GND | A11 |
| 2 | IO_L0N_CC_RS0_2 | Y10 | 16 | IO_L1N_16 | F8 | NA | GND | L11 |
| 2 | IO_L1P_CC_A25_2 | Y20 | 16 | IO_L2P_16 | F9 | NA | GND | N11 |
| 2 | IO_L1N_CC_A24_2 | AA19 | 16 | IO_L2N_16 | G9 | NA | GND | R11 |
| 2 | IO_L2P_A23_2 | AA10 | 16 | IO_L3P_16 | H8 | NA | GND | U11 |
| 2 | IO_L2N_A22 | Y11 | 16 | IO_L3N_16 | J8 | NA | GND | AA11 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| | _2 | | | | | | | |
| 2 | IO_L3P_A21_2 | AA18 | 16 | IO_L4P_16 | A9 | NA | GND | AF11 |
| 2 | IO_L3N_A20_2 | Y18 | 16 | IO_L4N_VREF_16 | A8 | NA | GND | D12 |
| 2 | IO_L4P_FCS_B_2 | Y12 | 16 | IO_L5P_16 | E8 | NA | GND | K12 |
| 2 | IO_L4N_VREF_FOE_B_MOSI_2 | AA12 | 16 | IO_L5N_16 | E7 | NA | GND | M12 |
| 2 | IO_L5P_FWE_B_2 | AA17 | 16 | IO_L6P_16 | B9 | NA | GND | P12 |
| 2 | IO_L5N_CSO_B_2 | Y17 | 16 | IO_L6N_16 | C8 | NA | GND | T12 |
| 2 | IO_L6P_D7_2 | AA13 | 16 | IO_L7P_16 | E6 | NA | GND | W12 |
| 2 | IO_L6N_D6_2 | AA14 | 16 | IO_L7N_16 | D6 | NA | GND | AD12 |
| 2 | IO_L7P_D5_2 | Y16 | 16 | IO_L8P_CC_16 | C9 | NA | GND | G13 |
| 2 | IO_L7N_D4_2 | W16 | 16 | IO_L8N_CC_16 | D8 | NA | GND | J13 |
| 2 | IO_L8P_D3_2 | Y13 | 16 | IO_L9P_CC_16 | C7 | NA | GND | L13 |
| 2 | IO_L8N_D2_FS2_2 | W14 | 16 | IO_L9N_CC_16 | C6 | NA | GND | N13 |
| 2 | IO_L9P_D1_FS1_2 | Y15 | 16 | IO_L10P_CC_16 | A7 | NA | GND | R13 |
| 2 | IO_L9N_D0_FS0_2 | AA15 | 16 | IO_L10N_CC_16 | B7 | NA | GND | U13 |
| 3 | IO_L0P_CC_GC_3 | D15 | 16 | IO_L11P_CC_16 | D9 | NA | GND | H14 |
| 3 | IO_L0N_CC_GC_3 | E15 | 16 | IO_L11N_CC_16 | D10 | NA | GND | K14 |
| 3 | IO_L1P_CC_GC_3 | D16 | 16 | IO_L12P_VRN_16 | B6 | NA | GND | T14 |
| 3 | IO_L1N_CC_GC_3 | E16 | 16 | IO_L12N_VRP_16 | A5 | NA | GND | V14 |
| 3 | IO_L2P_GC_VRN_3 | D14 | 16 | IO_L13P_16 | B10 | NA | GND | Y14 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 3 | IO_L2N_GC_VRP_3 | D13 | 16 | IO_L13N_16 | A10 | NA | GND | C15 |
| 3 | IO_L3P_GC_3 | E17 | 16 | IO_L14P_16 | A4 | NA | GND | J15 |
| 3 | IO_L3N_GC_3 | D18 | 16 | IO_L14N_VREF_16 | A3 | NA | GND | L15 |
| 3 | IO_L4P_GC_3 | E13 | 16 | IO_L15P_16 | B11 | NA | GND | U15 |
| 3 | IO_L4N_GC_VREF_3 | E12 | 16 | IO_L15N_16 | A12 | NA | GND | W15 |
| 3 | IO_L5P_GC_3 | E18 | 16 | IO_L16P_16 | B4 | NA | GND | AC15 |
| 3 | IO_L5N_GC_3 | F19 | 16 | IO_L16N_16 | B5 | NA | GND | A16 |
| 3 | IO_L6P_GC_3 | F12 | 16 | IO_L17P_16 | B12 | NA | GND | F16 |
| 3 | IO_L6N_GC_3 | E11 | 16 | IO_L17N_16 | C12 | NA | GND | H16 |
| 3 | IO_L7P_GC_3 | E20 | 16 | IO_L18P_16 | D5 | NA | GND | K16 |
| 3 | IO_L7N_GC_3 | E21 | 16 | IO_L18N_16 | E5 | NA | GND | M16 |
| 3 | IO_L8P_GC_3 | E10 | 16 | IO_L19P_16 | C11 | NA | GND | P16 |
| 3 | IO_L8N_GC_3 | F10 | 16 | IO_L19N_16 | D11 | NA | GND | T16 |
| 3 | IO_L9P_GC_3 | F20 | 17 | IO_L0P_17 | AC26 | NA | GND | V16 |
| 3 | IO_L9N_GC_3 | G21 | 17 | IO_L0N_17 | AD26 | NA | GND | AF16 |
| 4 | IO_L0P_GC_D15_4 | Y21 | 17 | IO_L1P_17 | AD25 | NA | GND | J17 |
| 4 | IO_L0N_GC_D14_4 | AA20 | 17 | IO_L1N_17 | AD24 | NA | GND | L17 |
| 4 | IO_L1P_GC_D13_4 | AB10 | 17 | IO_L2P_17 | AE25 | NA | GND | N17 |
| 4 | IO_L1N_GC_D12_4 | AB11 | 17 | IO_L2N_17 | AE26 | NA | GND | R17 |
| 4 | IO_L2P_GC_D11_4 | AB21 | 17 | IO_L3P_17 | AF25 | NA | GND | U17 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 4 | IO_L2N_GC_D10_4 | AB20 | 17 | IO_L3N_17 | AF24 | NA | GND | W17 |
| 4 | IO_L3P_GC_D9_4 | AC11 | 17 | IO_L4P_17 | AF23 | NA | GND | B18 |
| 4 | IO_L3N_GC_D8_4 | AB12 | 17 | IO_L4N_VREF_17 | AE23 | NA | GND | K18 |
| 4 | IO_L4P_GC_4 | AB19 | 17 | IO_L5P_17 | AE22 | NA | GND | M18 |
| 4 | IO_L4N_GC_VREF_4 | AC19 | 17 | IO_L5N_17 | AD23 | NA | GND | P18 |
| 4 | IO_L5P_GC_4 | AC12 | 17 | IO_L6P_17 | AC24 | NA | GND | T18 |
| 4 | IO_L5N_GC_4 | AC13 | 17 | IO_L6N_17 | AC23 | NA | GND | V18 |
| 4 | IO_L6P_GC_4 | AC18 | 17 | IO_L7P_17 | AC22 | NA | GND | AB18 |
| 4 | IO_L6N_GC_4 | AB17 | 17 | IO_L7N_17 | AB22 | NA | GND | E19 |
| 4 | IO_L7P_GC_VRN_4 | AB14 | 17 | IO_L8P_CC_17 | AF22 | NA | GND | L19 |
| 4 | IO_L7N_GC_VRP_4 | AC14 | 17 | IO_L8N_CC_17 | AE21 | NA | GND | N19 |
| 4 | IO_L8P_CC_GC_4 | AC17 | 17 | IO_L9P_CC_17 | AF20 | NA | GND | R19 |
| 4 | IO_L8N_CC_GC_4 | AB16 | 17 | IO_L9N_CC_17 | AE20 | NA | GND | U19 |
| 4 | IO_L9P_CC_GC_4 | AB15 | 17 | IO_L10P_CC_17 | AD19 | NA | GND | W19 |
| 4 | IO_L9N_CC_GC_4 | AC16 | 17 | IO_L10N_CC_17 | AD20 | NA | GND | AE19 |
| 11 | IO_L0P_11 | E26 | 17 | IO_L11P_CC_17 | AC21 | NA | GND | C20 |
| 11 | IO_L0N_11 | E25 | 17 | IO_L11N_CC_17 | AD21 | NA | GND | H20 |
| 11 | IO_L1P_11 | F25 | 17 | IO_L12P_VRN_17 | AF19 | NA | GND | V20 |
| 11 | IO_L1N_11 | G26 | 17 | IO_L12N_VRP_17 | AF18 | NA | GND | A21 |
| 11 | IO_L2P_11 | H26 | 17 | IO_L13P_17 | AE18 | NA | GND | L21 |
| 11 | IO_L2N_11 | G25 | 17 | IO_L13N_17 | AD18 | NA | GND | T21 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 11 | IO_L3P_11 | F24 | 17 | IO_L14P_17 | AE17 | NA | GND | AA21 |
| 11 | IO_L3N_11 | G24 | 17 | IO_L14N_VREF_17 | AF17 | NA | GND | AF21 |
| 11 | IO_L4P_11 | E23 | 17 | IO_L15P_17 | AE16 | NA | GND | D22 |
| 11 | IO_L4N_VREF_11 | E22 | 17 | IO_L15N_17 | AD16 | NA | GND | P22 |
| 11 | IO_L5P_11 | F23 | 17 | IO_L16P_17 | AD15 | NA | GND | AD22 |
| 11 | IO_L5N_11 | F22 | 17 | IO_L16N_17 | AE15 | NA | GND | G23 |
| 11 | IO_L6P_11 | G22 | 17 | IO_L17P_17 | AF15 | NA | GND | U23 |
| 11 | IO_L6N_11 | H22 | 17 | IO_L17N_17 | AF14 | NA | GND | K24 |
| 11 | IO_L7P_11 | H23 | 17 | IO_L18P_17 | AF13 | NA | GND | Y24 |
| 11 | IO_L7N_11 | J23 | 17 | IO_L18N_17 | AE13 | NA | GND | C25 |
| 11 | IO_L8P_CC_11 | J21 | 17 | IO_L19P_17 | AD13 | NA | GND | N25 |
| 11 | IO_L8N_CC_11 | K21 | 17 | IO_L19N_17 | AD14 | NA | GND | AC25 |
| 11 | IO_L9P_CC_11 | K22 | 18 | IO_L0P_18 | AF12 | NA | GND | A26 |
| 11 | IO_L9N_CC_11 | K23 | 18 | IO_L0N_18 | AE12 | NA | GND | F26 |
| 11 | IO_L10P_CC_SM15P_11 | L23 | 18 | IO_L1P_18 | V8 | NA | GND | L26 |
| 11 | IO_L10N_CC_SM15N_11 | L22 | 18 | IO_L1N_18 | V9 | NA | GND | T26 |
| 11 | IO_L11P_CC_SM14P_11 | M21 | 18 | IO_L2P_18 | AE11 | NA | GND | AA26 |
| 11 | IO_L11N_CC_SM14N_11 | N21 | 18 | IO_L2N_18 | AD11 | NA | GND | AF26 |
| 11 | IO_L12P_VRN_11 | H24 | 18 | IO_L3P_18 | W9 | NA | VCCAUX | U8 |
| 11 | IO_L12N_VRP_11 | J24 | 18 | IO_L3N_18 | W8 | NA | VCCAUX | K9 |
| 11 | IO_L13P_11 | J25 | 18 | IO_L4P_18 | AD10 | NA | VCCAUX | M9 |
| 11 | IO_L13N_11 | J26 | 18 | IO_L4N_VREF_18 | AE10 | NA | VCCAUX | P9 |
| 11 | IO_L14P_11 | K26 | 18 | IO_L5P_18 | Y7 | NA | VCCAUX | T9 |
| 11 | IO_L14N_VREF_11 | L25 | 18 | IO_L5N_18 | Y8 | NA | VCCAUX | W10 |
| 11 | IO_L15P_SM13P_11 | L24 | 18 | IO_L6P_18 | AF9 | NA | VCCAUX | M19 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 11 | IO_L15N_SM13N_11 | K25 | 18 | IO_L6N_18 | AF10 | NA | VCCAUX | P19 |
| 11 | IO_L16P_SM12P_11 | N26 | 18 | IO_L7P_18 | AA7 | NA | VCCAUX | T19 |
| 11 | IO_L16N_SM12N_11 | M26 | 18 | IO_L7N_18 | AA8 | NA | VCCAUX | V19 |
| 11 | IO_L17P_SM11P_11 | M25 | 18 | IO_L8P_CC_18 | AF7 | NA | VCCAUX | Y19 |
| 11 | IO_L17N_SM11N_11 | M24 | 18 | IO_L8N_CC_18 | AF8 | NA | VCCAUX | N20 |
| 11 | IO_L18P_SM10P_11 | N24 | 18 | IO_L9P_CC_18 | AA5 | NA | VCCINT | L10 |
| 11 | IO_L18N_SM10N_11 | N23 | 18 | IO_L9N_CC_18 | AB5 | NA | VCCINT | N10 |
| 11 | IO_L19P_SM9P_11 | N22 | 18 | IO_L10P_CC_18 | AB6 | NA | VCCINT | R10 |
| 11 | IO_L19N_SM9N_11 | M22 | 18 | IO_L10N_CC_18 | AB7 | NA | VCCINT | U10 |
| 12 | IO_L0P_12 | Y6 | 18 | IO_L11P_CC_18 | AE8 | NA | VCCINT | M11 |
| 12 | IO_L0N_12 | Y5 | 18 | IO_L11N_CC_18 | AE7 | NA | VCCINT | P11 |
| 12 | IO_L1P_12 | G6 | 18 | IO_L12P_VRN_18 | AC6 | NA | VCCINT | T11 |
| 12 | IO_L1N_12 | H6 | 18 | IO_L12N_VRP_18 | AD5 | NA | VCCINT | L12 |
| 12 | IO_L2P_12 | Y4 | 18 | IO_L13P_18 | AE6 | NA | VCCINT | N12 |
| 12 | IO_L2N_12 | W4 | 18 | IO_L13N_18 | AF5 | NA | VCCINT | R12 |
| 12 | IO_L3P_12 | G5 | 18 | IO_L14P_18 | AE5 | NA | VCCINT | K13 |
| 12 | IO_L3N_12 | F5 | 18 | IO_L14N_VREF_18 | AD4 | NA | VCCINT | M13 |
| 12 | IO_L4P_12 | W5 | 18 | IO_L15P_18 | AF4 | NA | VCCINT | P13 |
| 12 | IO_L4N_VREF_12 | W6 | 18 | IO_L15N_18 | AF3 | NA | VCCINT | T13 |
| 12 | IO_L5P_12 | G4 | 18 | IO_L16P_18 | AD6 | NA | VCCINT | J14 |
| 12 | IO_L5N_12 | H4 | 18 | IO_L16N_18 | AC7 | NA | VCCINT | L14 |
| 12 | IO_L6P_12 | V6 | 18 | IO_L17P_18 | AC8 | NA | VCCINT | U14 |
| 12 | IO_L6N_12 | V7 | 18 | IO_L17N_18 | AD8 | NA | VCCINT | H15 |
| 12 | IO_L7P_12 | J5 | 18 | IO_L18P_18 | AD9 | NA | VCCINT | K15 |
| 12 | IO_L7N_12 | J6 | 18 | IO_L18N_18 | AC9 | NA | VCCINT | T15 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 12 | IO_L8P_CC_12 | U7 | 18 | IO_L19P_18 | AB9 | NA | VCCINT | V15 |
| 12 | IO_L8N_CC_12 | T8 | 18 | IO_L19N_18 | AA9 | NA | VCCINT | J16 |
| 12 | IO_L9P_CC_12 | K5 | NA | MGTTXP0_112 | H2 | NA | VCCINT | L16 |
| 12 | IO_L9N_CC_12 | L5 | NA | MGTAVTTTX_112 | H3 | NA | VCCINT | N16 |
| 12 | IO_L10P_CC_12 | K6 | NA | MGTTXN0_112 | J2 | NA | VCCINT | R16 |
| 12 | IO_L10N_CC_12 | K7 | NA | MGTRXP0_112 | J1 | NA | VCCINT | U16 |
| 12 | IO_L11P_CC_12 | U6 | NA | MGTAVTTRX_112 | J3 | NA | VCCINT | H17 |
| 12 | IO_L11N_CC_12 | U5 | NA | MGTRXN0_112 | K1 | NA | VCCINT | K17 |
| 12 | IO_L12P_VRN_12 | K8 | NA | MGTAVCCPLL_112 | M3 | NA | VCCINT | M17 |
| 12 | IO_L12N_VRP_12 | L7 | NA | MGTRXN1_112 | L1 | NA | VCCINT | P17 |
| 12 | IO_L13P_12 | T5 | NA | MGTREFCLKN_112 | K3 | NA | VCCINT | T17 |
| 12 | IO_L13N_12 | R5 | NA | MGTRXP1_112 | M1 | NA | VCCINT | V17 |
| 12 | IO_L14P_12 | M7 | NA | MGTREFCLKP_112 | K4 | NA | VCCINT | J18 |
| 12 | IO_L14N_VREF_12 | L8 | NA | MGTTXN1_112 | M2 | NA | VCCINT | L18 |
| 12 | IO_L15P_12 | R6 | NA | MGTAVTTTX_112 | N3 | NA | VCCINT | N18 |
| 12 | IO_L15N_12 | T7 | NA | MGTTXP1_112 | N2 | NA | VCCINT | R18 |
| 12 | IO_L16P_12 | P6 | NA | MGTAVTTRXC | P5 | NA | VCCINT | U18 |
| 12 | IO_L16N_12 | N6 | NA | MGTRREF_112 | P4 | NA | VCCINT | W18 |
| 12 | IO_L17P_12 | M6 | NC | NC | M5 | NA | VCCINT | K19 |
| 12 | IO_L17N_12 | N7 | NA | MGTTXP0_114 | P2 | 0 | VCCO_0 | F11 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 12 | IO_L18P_12 | N8 | NA | MGTAVTTTX_114 | P3 | 0 | VCCO_0 | J12 |
| 12 | IO_L18N_12 | P8 | NA | MGTTXN0_114 | R2 | 1 | VCCO_1 | B13 |
| 12 | IO_L19P_12 | R8 | NA | MGTRXP0_114 | R1 | 1 | VCCO_1 | E14 |
| 12 | IO_L19N_12 | R7 | NA | MGTAVTTRX_114 | R3 | 2 | VCCO_2 | AA16 |
| 13 | IO_L0P_SM8P_13 | P26 | NA | MGTRXN0_114 | T1 | 2 | VCCO_2 | AD17 |
| 13 | IO_L0N_SM8N_13 | R26 | NA | MGTAVCCPLL_114 | V3 | 3 | VCCO_3 | D17 |
| 13 | IO_L1P_SM7P_13 | P25 | NA | MGTRXN1_114 | U1 | 3 | VCCO_3 | G18 |
| 13 | IO_L1N_SM7N_13 | R25 | NA | MGTREFCLKN_114 | T3 | 4 | VCCO_4 | AB13 |
| 13 | IO_L2P_SM6P_13 | P24 | NA | MGTRXP1_114 | V1 | 4 | VCCO_4 | AE14 |
| 13 | IO_L2N_SM6N_13 | P23 | NA | MGTREFCLKP_114 | T4 | 11 | VCCO_11 | J22 |
| 13 | IO_L3P_SM5P_13 | R23 | NA | MGTTXN1_114 | V2 | 11 | VCCO_11 | M23 |
| 13 | IO_L3N_SM5N_13 | R22 | NA | MGTAVTTTX_114 | W3 | 11 | VCCO_11 | H25 |
| 13 | IO_L4P_13 | U26 | NA | MGTTXP1_114 | W2 | 12 | VCCO_12 | H5 |
| 13 | IO_L4N_VREF_13 | V26 | NA | MGTTXP0_116 | B2 | 12 | VCCO_12 | L6 |
| 13 | IO_L5P_SM4P_13 | U25 | NA | MGTAVTTTX_116 | B3 | 12 | VCCO_12 | P7 |
| 13 | IO_L5N_SM4N_13 | T25 | NA | MGTTXN0_116 | C2 | 13 | VCCO_13 | W22 |
| 13 | IO_L6P_SM3P_13 | T24 | NA | MGTRXP0_116 | C1 | 13 | VCCO_13 | R24 |
| 13 | IO_L6N_SM3N_13 | T23 | NA | MGTAVTTRX_116 | C3 | 13 | VCCO_13 | V25 |
| 13 | IO_L7P_SM2P_13 | U24 | NA | MGTRXN0_116 | D1 | 15 | VCCO_15 | F21 |
| 13 | IO_L7N_SM2N_13 | V24 | NA | MGTAVCCPLL_116 | F3 | 15 | VCCO_15 | B23 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 13 | IO_L8P_CC_SM1P_13 | W26 | NA | MGTRXN1_116 | E1 | 15 | VCCO_15 | E24 |
| 13 | IO_L8N_CC_SM1N_13 | W25 | NA | MGTREFCLKN_116 | D3 | 16 | VCCO_16 | D7 |
| 13 | IO_L9P_CC_SM0P_13 | W24 | NA | MGTRXP1_116 | F1 | 16 | VCCO_16 | G8 |
| 13 | IO_L9N_CC_SM0N_13 | V23 | NA | MGTREFCLKP_116 | D4 | 16 | VCCO_16 | C10 |
| 13 | IO_L10P_CC_13 | AA22 | NA | MGTTXN1_116 | F2 | 17 | VCCO_17 | AC20 |
| 13 | IO_L10N_CC_13 | Y22 | NA | MGTAVTTTX_116 | G3 | 17 | VCCO_17 | AB23 |
| 13 | IO_L11P_CC_13 | Y23 | NA | MGTTXP1_116 | G2 | 17 | VCCO_17 | AE24 |
| 13 | IO_L11N_CC_13 | W23 | NA | MGTTXP0_118 | Y2 | 18 | VCCO_18 | AA6 |
| 13 | IO_L12P_VRN_13 | Y26 | NA | MGTAVTTTX_118 | Y3 | 18 | VCCO_18 | AD7 |
| 13 | IO_L12N_VRP_13 | Y25 | NA | MGTTXN0_118 | AA2 | 18 | VCCO_18 | AC10 |
| 13 | IO_L13P_13 | AA25 | NA | MGTRXP0_118 | AA1 | NA | MGTAVCC_112 | L3 |
| 13 | IO_L13N_13 | AB26 | NA | MGTAVTTRX_118 | AA3 | NA | MGTAVCC_112 | L4 |
| 13 | IO_L14P_13 | AB25 | NA | MGTRXN0_118 | AB1 | NA | MGTAVCC_114 | U3 |
| 13 | IO_L14N_VREF_13 | AA24 | NA | MGTAVCCPLL_118 | AD3 | NA | MGTAVCC_114 | U4 |
| 13 | IO_L15P_13 | AB24 | NA | MGTRXN1_118 | AC1 | NA | MGTAVCC_116 | E3 |
| 13 | IO_L15N_13 | AA23 | NA | MGTREFCLKN_118 | AB3 | NA | MGTAVCC_116 | E4 |
| 13 | IO_L16P_13 | P21 | NA | MGTRXP1_118 | AD1 | NA | MGTAVCC_118 | AC3 |
| 13 | IO_L16N_13 | R21 | NA | MGTREFCLKP_118 | AB4 | NA | MGTAVCC_118 | AC4 |
| 13 | IO_L17P_13 | T22 | | | | NA | FLOAT | N4 |

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.

2. Do not connect a single-ended clock to the N-side of clock capable pins, for example,

IO_L8N_CC_11.

3. RSVD pins must be tied to GND (logic 0).

As shown in Table 24, the BQ5VSX50T device is available in the BGA665 packages.

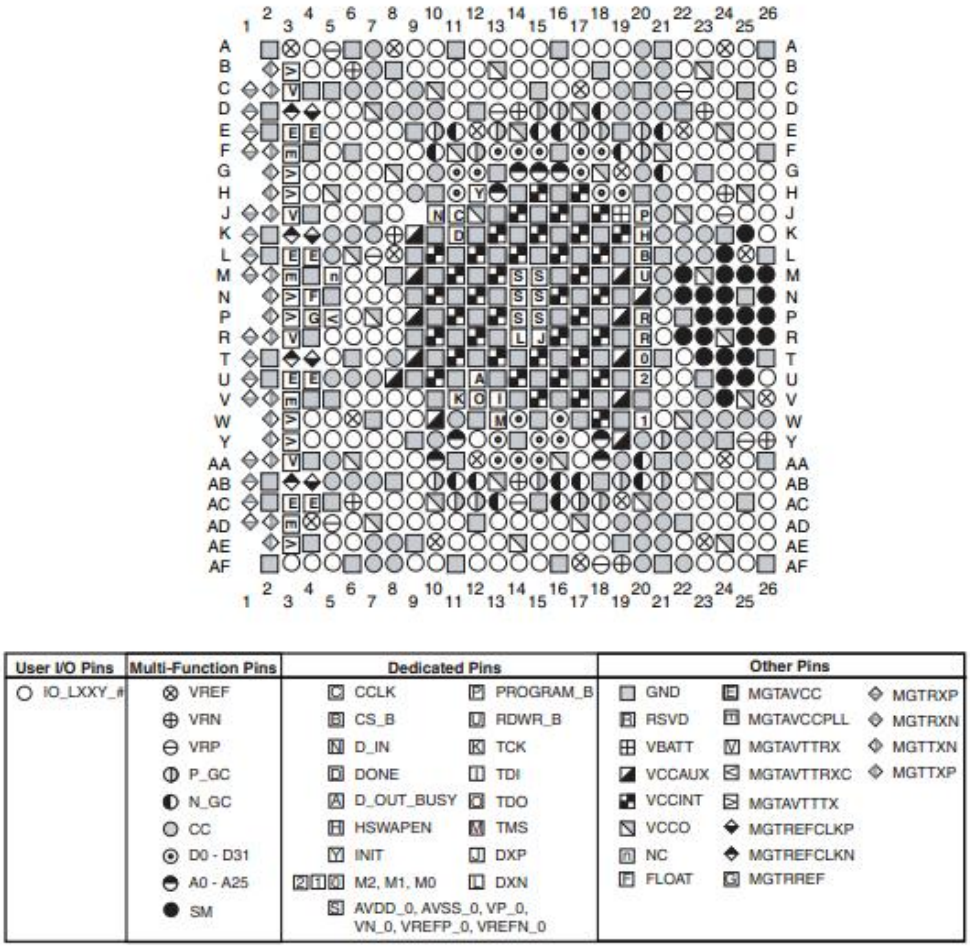



Table 24 BQ5VSX50T packages

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 0 | DXP_0 | R15 | 13 | IO_L17N_13 | U22 | NA | MGTTXN1_118 | AD2 |
| 0 | DXN_0 | R14 | 13 | IO_L18P_13 | U21 | NA | MGTAVTTTX_118 | AE3 |
| 0 | AVDD_0 | M15 | 13 | IO_L18N_13 | V22 | NA | MGTTXP1_118 | AE2 |
| 0 | AVSS_0 | M14 | 13 | IO_L19P_13 | V21 | NA | GND | A2 |
| 0 | VP_0 | N15 | 13 | IO_L19N_13 | W21 | NA | GND | D2 |
| 0 | VN_0 | P14 | 15 | IO_L0P_15 | C13 | NA | GND | E2 |
| 0 | VREFP_0 | P15 | 15 | IO_L0N_15 | C14 | NA | GND | K2 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 0 | VREFN_0 | N14 | 15 | IO_L1P_15 | B14 | NA | GND | L2 |
| 0 | VBATT_0 | J19 | 15 | IO_L1N_15 | A13 | NA | GND | T2 |
| 0 | PROGRAM_B_0 | J20 | 15 | IO_L2P_15 | A14 | NA | GND | U2 |
| 0 | HSWAPEN_0 | K20 | 15 | IO_L2N_15 | A15 | NA | GND | AB2 |
| 0 | D_IN_0 | J10 | 15 | IO_L3P_15 | B15 | NA | GND | AC2 |
| 0 | DONE_0 | K11 | 15 | IO_L3N_15 | C16 | NA | GND | AF2 |
| 0 | CCLK_0 | J11 | 15 | IO_L4P_15 | B16 | NA | GND | C4 |
| 0 | INIT_B_0 | H12 | 15 | IO_L4N_VREF_15 | C17 | NA | GND | F4 |
| 0 | CS_B_0 | L20 | 15 | IO_L5P_15 | B17 | NA | GND | J4 |
| 0 | RDWR_B_0 | M20 | 15 | IO_L5N_15 | A17 | NA | GND | M4 |
| 0 | RSVD(3) | P20 | 15 | IO_L6P_15 | A18 | NA | GND | R4 |
| 0 | RSVD(3) | R20 | 15 | IO_L6N_15 | A19 | NA | GND | V4 |
| 0 | TCK_0 | V11 | 15 | IO_L7P_15 | B19 | NA | GND | AA4 |
| 0 | M0_0 | T20 | 15 | IO_L7N_15 | C18 | NA | GND | AE4 |
| 0 | M2_0 | U20 | 15 | IO_L8P_CC_15 | A20 | NA | GND | C5 |
| 0 | M1_0 | W20 | 15 | IO_L8N_CC_15 | B20 | NA | GND | N5 |
| 0 | TMS_0 | W13 | 15 | IO_L9P_CC_15 | C19 | NA | GND | V5 |
| 0 | TDI_0 | V13 | 15 | IO_L9N_CC_15 | D19 | NA | GND | AC5 |
| 0 | D_OUT_BUSY_0 | U12 | 15 | IO_L10P_CC_15 | D21 | NA | GND | A6 |
| 0 | TDO_0 | V12 | 15 | IO_L10N_CC_15 | D20 | NA | GND | F6 |
| 1 | IO_L0P_A19_1 | G15 | 15 | IO_L11P_CC_15 | B21 | NA | GND | T6 |
| 1 | IO_L0N_A18_1 | G16 | 15 | IO_L11N_CC_15 | C21 | NA | GND | AF6 |
| 1 | IO_L1P_A17_1 | H13 | 15 | IO_L12P_VRN_15 | D23 | NA | GND | J7 |
| 1 | IO_L1N_A16_1 | G14 | 15 | IO_L12N_VRP_15 | C22 | NA | GND | W7 |
| 1 | IO_L2P_A15_D31_1 | G17 | 15 | IO_L13P_15 | B22 | NA | GND | B8 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 1 | IO_L2N_A14_D30_1 | F17 | 15 | IO_L13N_15 | A22 | NA | GND | M8 |
| 1 | IO_L3P_A13_D29_1 | F15 | 15 | IO_L14P_15 | A23 | NA | GND | AB8 |
| 1 | IO_L3N_A12_D28_1 | F14 | 15 | IO_L14N_VREF_15 | A24 | NA | GND | E9 |
| 1 | IO_L4P_A11_D27_1 | F18 | 15 | IO_L15P_15 | B24 | NA | GND | L9 |
| 1 | IO_L4N_VREF_A10_D26_1 | G19 | 15 | IO_L15N_15 | C23 | NA | GND | N9 |
| 1 | IO_L5P_A9_D25_1 | F13 | 15 | IO_L16P_15 | D24 | NA | GND | R9 |
| 1 | IO_L5N_A8_D24_1 | G12 | 15 | IO_L16N_15 | C24 | NA | GND | U9 |
| 1 | IO_L6P_A7_D23_1 | H18 | 15 | IO_L17P_15 | B25 | NA | GND | Y9 |
| 1 | IO_L6N_A6_D22_1 | H19 | 15 | IO_L17N_15 | A25 | NA | GND | AE9 |
| 1 | IO_L7P_A5_D21_1 | G11 | 15 | IO_L18P_15 | B26 | NA | GND | H10 |
| 1 | IO_L7N_A4_D20_1 | H11 | 15 | IO_L18N_15 | C26 | NA | GND | K10 |
| 1 | IO_L8P_CC_A3_D19_1 | G20 | 15 | IO_L19P_15 | D26 | NA | GND | M10 |
| 1 | IO_L8N_CC_A2_D18_1 | H21 | 15 | IO_L19N_15 | D25 | NA | GND | P10 |
| 1 | IO_L9P_CC_A1_D17_1 | G10 | 16 | IO_L0P_16 | H7 | NA | GND | T10 |
| 1 | IO_L9N_CC_A0_D16_1 | H9 | 16 | IO_L0N_16 | G7 | NA | GND | V10 |
| 2 | IO_L0P_CC_RS1_2 | W11 | 16 | IO_L1P_16 | F7 | NA | GND | A11 |
| 2 | IO_L0N_CC_RS0_2 | Y10 | 16 | IO_L1N_16 | F8 | NA | GND | L11 |
| 2 | IO_L1P_CC_A25_2 | Y20 | 16 | IO_L2P_16 | F9 | NA | GND | N11 |
| 2 | IO_L1N_CC_A24_2 | AA19 | 16 | IO_L2N_16 | G9 | NA | GND | R11 |
| 2 | IO_L2P_A23 | AA10 | 16 | IO_L3P_16 | H8 | NA | GND | U11 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| | _2 | | | | | | | |
| 2 | IO_L2N_A22_2 | Y11 | 16 | IO_L3N_16 | J8 | NA | GND | AA11 |
| 2 | IO_L3P_A21_2 | AA18 | 16 | IO_L4P_16 | A9 | NA | GND | AF11 |
| 2 | IO_L3N_A20_2 | Y18 | 16 | IO_L4N_VREF_16 | A8 | NA | GND | D12 |
| 2 | IO_L4P_FCS_B_2 | Y12 | 16 | IO_L5P_16 | E8 | NA | GND | K12 |
| 2 | IO_L4N_VREF_FOE_B_MOSI_2 | AA12 | 16 | IO_L5N_16 | E7 | NA | GND | M12 |
| 2 | IO_L5P_FWE_B_2 | AA17 | 16 | IO_L6P_16 | B9 | NA | GND | P12 |
| 2 | IO_L5N_CSO_B_2 | Y17 | 16 | IO_L6N_16 | C8 | NA | GND | T12 |
| 2 | IO_L6P_D7_2 | AA13 | 16 | IO_L7P_16 | E6 | NA | GND | W12 |
| 2 | IO_L6N_D6_2 | AA14 | 16 | IO_L7N_16 | D6 | NA | GND | AD12 |
| 2 | IO_L7P_D5_2 | Y16 | 16 | IO_L8P_CC_16 | C9 | NA | GND | G13 |
| 2 | IO_L7N_D4_2 | W16 | 16 | IO_L8N_CC_16 | D8 | NA | GND | J13 |
| 2 | IO_L8P_D3_2 | Y13 | 16 | IO_L9P_CC_16 | C7 | NA | GND | L13 |
| 2 | IO_L8N_D2_FS2_2 | W14 | 16 | IO_L9N_CC_16 | C6 | NA | GND | N13 |
| 2 | IO_L9P_D1_FS1_2 | Y15 | 16 | IO_L10P_CC_16 | A7 | NA | GND | R13 |
| 2 | IO_L9N_D0_FS0_2 | AA15 | 16 | IO_L10N_CC_16 | B7 | NA | GND | U13 |
| 3 | IO_L0P_CC_GC_3 | D15 | 16 | IO_L11P_CC_16 | D9 | NA | GND | H14 |
| 3 | IO_L0N_CC_GC_3 | E15 | 16 | IO_L11N_CC_16 | D10 | NA | GND | K14 |
| 3 | IO_L1P_CC_GC_3 | D16 | 16 | IO_L12P_VRN_16 | B6 | NA | GND | T14 |
| 3 | IO_L1N_CC_GC_3 | E16 | 16 | IO_L12N_VRP_16 | A5 | NA | GND | V14 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 3 | IO_L2P_GC_VRN_3 | D14 | 16 | IO_L13P_16 | B10 | NA | GND | Y14 |
| 3 | IO_L2N_GC_VRP_3 | D13 | 16 | IO_L13N_16 | A10 | NA | GND | C15 |
| 3 | IO_L3P_GC_3 | E17 | 16 | IO_L14P_16 | A4 | NA | GND | J15 |
| 3 | IO_L3N_GC_3 | D18 | 16 | IO_L14N_VREF_16 | A3 | NA | GND | L15 |
| 3 | IO_L4P_GC_3 | E13 | 16 | IO_L15P_16 | B11 | NA | GND | U15 |
| 3 | IO_L4N_GC_VREF_3 | E12 | 16 | IO_L15N_16 | A12 | NA | GND | W15 |
| 3 | IO_L5P_GC_3 | E18 | 16 | IO_L16P_16 | B4 | NA | GND | AC15 |
| 3 | IO_L5N_GC_3 | F19 | 16 | IO_L16N_16 | B5 | NA | GND | A16 |
| 3 | IO_L6P_GC_3 | F12 | 16 | IO_L17P_16 | B12 | NA | GND | F16 |
| 3 | IO_L6N_GC_3 | E11 | 16 | IO_L17N_16 | C12 | NA | GND | H16 |
| 3 | IO_L7P_GC_3 | E20 | 16 | IO_L18P_16 | D5 | NA | GND | K16 |
| 3 | IO_L7N_GC_3 | E21 | 16 | IO_L18N_16 | E5 | NA | GND | M16 |
| 3 | IO_L8P_GC_3 | E10 | 16 | IO_L19P_16 | C11 | NA | GND | P16 |
| 3 | IO_L8N_GC_3 | F10 | 16 | IO_L19N_16 | D11 | NA | GND | T16 |
| 3 | IO_L9P_GC_3 | F20 | 17 | IO_L0P_17 | AC26 | NA | GND | V16 |
| 3 | IO_L9N_GC_3 | G21 | 17 | IO_L0N_17 | AD26 | NA | GND | AF16 |
| 4 | IO_L0P_GC_D15_4 | Y21 | 17 | IO_L1P_17 | AD25 | NA | GND | J17 |
| 4 | IO_L0N_GC_D14_4 | AA20 | 17 | IO_L1N_17 | AD24 | NA | GND | L17 |
| 4 | IO_L1P_GC_D13_4 | AB10 | 17 | IO_L2P_17 | AE25 | NA | GND | N17 |
| 4 | IO_L1N_GC_D12_4 | AB11 | 17 | IO_L2N_17 | AE26 | NA | GND | R17 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 4 | IO_L2P_GC_D11_4 | AB21 | 17 | IO_L3P_17 | AF25 | NA | GND | U17 |
| 4 | IO_L2N_GC_D10_4 | AB20 | 17 | IO_L3N_17 | AF24 | NA | GND | W17 |
| 4 | IO_L3P_GC_D9_4 | AC11 | 17 | IO_L4P_17 | AF23 | NA | GND | B18 |
| 4 | IO_L3N_GC_D8_4 | AB12 | 17 | IO_L4N_VREF_17 | AE23 | NA | GND | K18 |
| 4 | IO_L4P_GC_4 | AB19 | 17 | IO_L5P_17 | AE22 | NA | GND | M18 |
| 4 | IO_L4N_GC_VREF_4 | AC19 | 17 | IO_L5N_17 | AD23 | NA | GND | P18 |
| 4 | IO_L5P_GC_4 | AC12 | 17 | IO_L6P_17 | AC24 | NA | GND | T18 |
| 4 | IO_L5N_GC_4 | AC13 | 17 | IO_L6N_17 | AC23 | NA | GND | V18 |
| 4 | IO_L6P_GC_4 | AC18 | 17 | IO_L7P_17 | AC22 | NA | GND | AB18 |
| 4 | IO_L6N_GC_4 | AB17 | 17 | IO_L7N_17 | AB22 | NA | GND | E19 |
| 4 | IO_L7P_GC_VRN_4 | AB14 | 17 | IO_L8P_CC_17 | AF22 | NA | GND | L19 |
| 4 | IO_L7N_GC_VRP_4 | AC14 | 17 | IO_L8N_CC_17 | AE21 | NA | GND | N19 |
| 4 | IO_L8P_CC_GC_4 | AC17 | 17 | IO_L9P_CC_17 | AF20 | NA | GND | R19 |
| 4 | IO_L8N_CC_GC_4 | AB16 | 17 | IO_L9N_CC_17 | AE20 | NA | GND | U19 |
| 4 | IO_L9P_CC_GC_4 | AB15 | 17 | IO_L10P_CC_17 | AD19 | NA | GND | W19 |
| 4 | IO_L9N_CC_GC_4 | AC16 | 17 | IO_L10N_CC_17 | AD20 | NA | GND | AE19 |
| 11 | IO_L0P_11 | E26 | 17 | IO_L11P_CC_17 | AC21 | NA | GND | C20 |
| 11 | IO_L0N_11 | E25 | 17 | IO_L11N_CC_17 | AD21 | NA | GND | H20 |
| 11 | IO_L1P_11 | F25 | 17 | IO_L12P_VRN_17 | AF19 | NA | GND | V20 |
| 11 | IO_L1N_11 | G26 | 17 | IO_L12N_VRP_17 | AF18 | NA | GND | A21 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 11 | IO_L2P_11 | H26 | 17 | IO_L13P_17 | AE18 | NA | GND | L21 |
| 11 | IO_L2N_11 | G25 | 17 | IO_L13N_17 | AD18 | NA | GND | T21 |
| 11 | IO_L3P_11 | F24 | 17 | IO_L14P_17 | AE17 | NA | GND | AA21 |
| 11 | IO_L3N_11 | G24 | 17 | IO_L14N_VREF_17 | AF17 | NA | GND | AF21 |
| 11 | IO_L4P_11 | E23 | 17 | IO_L15P_17 | AE16 | NA | GND | D22 |
| 11 | IO_L4N_VREF_11 | E22 | 17 | IO_L15N_17 | AD16 | NA | GND | P22 |
| 11 | IO_L5P_11 | F23 | 17 | IO_L16P_17 | AD15 | NA | GND | AD22 |
| 11 | IO_L5N_11 | F22 | 17 | IO_L16N_17 | AE15 | NA | GND | G23 |
| 11 | IO_L6P_11 | G22 | 17 | IO_L17P_17 | AF15 | NA | GND | U23 |
| 11 | IO_L6N_11 | H22 | 17 | IO_L17N_17 | AF14 | NA | GND | K24 |
| 11 | IO_L7P_11 | H23 | 17 | IO_L18P_17 | AF13 | NA | GND | Y24 |
| 11 | IO_L7N_11 | J23 | 17 | IO_L18N_17 | AE13 | NA | GND | C25 |
| 11 | IO_L8P_CC_11 | J21 | 17 | IO_L19P_17 | AD13 | NA | GND | N25 |
| 11 | IO_L8N_CC_11 | K21 | 17 | IO_L19N_17 | AD14 | NA | GND | AC25 |
| 11 | IO_L9P_CC_11 | K22 | 18 | IO_L0P_18 | AF12 | NA | GND | A26 |
| 11 | IO_L9N_CC_11 | K23 | 18 | IO_L0N_18 | AE12 | NA | GND | F26 |
| 11 | IO_L10P_CC_SM15P_11 | L23 | 18 | IO_L1P_18 | V8 | NA | GND | L26 |
| 11 | IO_L10N_CC_SM15N_11 | L22 | 18 | IO_L1N_18 | V9 | NA | GND | T26 |
| 11 | IO_L11P_CC_SM14P_11 | M21 | 18 | IO_L2P_18 | AE11 | NA | GND | AA26 |
| 11 | IO_L11N_CC_SM14N_11 | N21 | 18 | IO_L2N_18 | AD11 | NA | GND | AF26 |
| 11 | IO_L12P_VRN_11 | H24 | 18 | IO_L3P_18 | W9 | NA | VCCAUX | U8 |
| 11 | IO_L12N_VRP_11 | J24 | 18 | IO_L3N_18 | W8 | NA | VCCAUX | K9 |
| 11 | IO_L13P_11 | J25 | 18 | IO_L4P_18 | AD10 | NA | VCCAUX | M9 |
| 11 | IO_L13N_11 | J26 | 18 | IO_L4N_VREF_18 | AE10 | NA | VCCAUX | P9 |
| 11 | IO_L14P_11 | K26 | 18 | IO_L5P_18 | Y7 | NA | VCCAUX | T9 |
| 11 | IO_L14N_VREF_11 | L25 | 18 | IO_L5N_18 | Y8 | NA | VCCAUX | W10 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 11 | IO_L15P_SM13P_11 | L24 | 18 | IO_L6P_18 | AF9 | NA | VCCAUX | M19 |
| 11 | IO_L15N_SM13N_11 | K25 | 18 | IO_L6N_18 | AF10 | NA | VCCAUX | P19 |
| 11 | IO_L16P_SM12P_11 | N26 | 18 | IO_L7P_18 | AA7 | NA | VCCAUX | T19 |
| 11 | IO_L16N_SM12N_11 | M26 | 18 | IO_L7N_18 | AA8 | NA | VCCAUX | V19 |
| 11 | IO_L17P_SM11P_11 | M25 | 18 | IO_L8P_CC_18 | AF7 | NA | VCCAUX | Y19 |
| 11 | IO_L17N_SM11N_11 | M24 | 18 | IO_L8N_CC_18 | AF8 | NA | VCCAUX | N20 |
| 11 | IO_L18P_SM10P_11 | N24 | 18 | IO_L9P_CC_18 | AA5 | NA | VCCINT | L10 |
| 11 | IO_L18N_SM10N_11 | N23 | 18 | IO_L9N_CC_18 | AB5 | NA | VCCINT | N10 |
| 11 | IO_L19P_SM9P_11 | N22 | 18 | IO_L10P_CC_18 | AB6 | NA | VCCINT | R10 |
| 11 | IO_L19N_SM9N_11 | M22 | 18 | IO_L10N_CC_18 | AB7 | NA | VCCINT | U10 |
| 12 | IO_L0P_12 | Y6 | 18 | IO_L11P_CC_18 | AE8 | NA | VCCINT | M11 |
| 12 | IO_L0N_12 | Y5 | 18 | IO_L11N_CC_18 | AE7 | NA | VCCINT | P11 |
| 12 | IO_L1P_12 | G6 | 18 | IO_L12P_VRN_18 | AC6 | NA | VCCINT | T11 |
| 12 | IO_L1N_12 | H6 | 18 | IO_L12N_VRP_18 | AD5 | NA | VCCINT | L12 |
| 12 | IO_L2P_12 | Y4 | 18 | IO_L13P_18 | AE6 | NA | VCCINT | N12 |
| 12 | IO_L2N_12 | W4 | 18 | IO_L13N_18 | AF5 | NA | VCCINT | R12 |
| 12 | IO_L3P_12 | G5 | 18 | IO_L14P_18 | AE5 | NA | VCCINT | K13 |
| 12 | IO_L3N_12 | F5 | 18 | IO_L14N_VREF_18 | AD4 | NA | VCCINT | M13 |
| 12 | IO_L4P_12 | W5 | 18 | IO_L15P_18 | AF4 | NA | VCCINT | P13 |
| 12 | IO_L4N_VREF_12 | W6 | 18 | IO_L15N_18 | AF3 | NA | VCCINT | T13 |
| 12 | IO_L5P_12 | G4 | 18 | IO_L16P_18 | AD6 | NA | VCCINT | J14 |
| 12 | IO_L5N_12 | H4 | 18 | IO_L16N_18 | AC7 | NA | VCCINT | L14 |
| 12 | IO_L6P_12 | V6 | 18 | IO_L17P_18 | AC8 | NA | VCCINT | U14 |
| 12 | IO_L6N_12 | V7 | 18 | IO_L17N_18 | AD8 | NA | VCCINT | H15 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 12 | IO_L7P_12 | J5 | 18 | IO_L18P_18 | AD9 | NA | VCCINT | K15 |
| 12 | IO_L7N_12 | J6 | 18 | IO_L18N_18 | AC9 | NA | VCCINT | T15 |
| 12 | IO_L8P_CC_12 | U7 | 18 | IO_L19P_18 | AB9 | NA | VCCINT | V15 |
| 12 | IO_L8N_CC_12 | T8 | 18 | IO_L19N_18 | AA9 | NA | VCCINT | J16 |
| 12 | IO_L9P_CC_12 | K5 | NA | MGTTXP0_112 | H2 | NA | VCCINT | L16 |
| 12 | IO_L9N_CC_12 | L5 | NA | MGTAVTTTX_112 | H3 | NA | VCCINT | N16 |
| 12 | IO_L10P_CC_12 | K6 | NA | MGTTXN0_112 | J2 | NA | VCCINT | R16 |
| 12 | IO_L10N_CC_12 | K7 | NA | MGTRXP0_112 | J1 | NA | VCCINT | U16 |
| 12 | IO_L11P_CC_12 | U6 | NA | MGTAVTTRX_112 | J3 | NA | VCCINT | H17 |
| 12 | IO_L11N_CC_12 | U5 | NA | MGTRXN0_112 | K1 | NA | VCCINT | K17 |
| 12 | IO_L12P_VRN_12 | K8 | NA | MGTAVCCPLL_112 | M3 | NA | VCCINT | M17 |
| 12 | IO_L12N_VRP_12 | L7 | NA | MGTRXN1_112 | L1 | NA | VCCINT | P17 |
| 12 | IO_L13P_12 | T5 | NA | MGTREFCLKN_112 | K3 | NA | VCCINT | T17 |
| 12 | IO_L13N_12 | R5 | NA | MGTRXP1_112 | M1 | NA | VCCINT | V17 |
| 12 | IO_L14P_12 | M7 | NA | MGTREFCLKP_112 | K4 | NA | VCCINT | J18 |
| 12 | IO_L14N_VREF_12 | L8 | NA | MGTTXN1_112 | M2 | NA | VCCINT | L18 |
| 12 | IO_L15P_12 | R6 | NA | MGTAVTTTX_112 | N3 | NA | VCCINT | N18 |
| 12 | IO_L15N_12 | T7 | NA | MGTTXP1_112 | N2 | NA | VCCINT | R18 |
| 12 | IO_L16P_12 | P6 | NA | MGTAVTTRXC | P5 | NA | VCCINT | U18 |
| 12 | IO_L16N_12 | N6 | NA | MGTRREF_112 | P4 | NA | VCCINT | W18 |
| 12 | IO_L17P_12 | M6 | NC | NC | M5 | NA | VCCINT | K19 |
| 12 | IO_L17N_12 | N7 | NA | MGTTXP0_ | P2 | 0 | VCCO_0 | F11 |

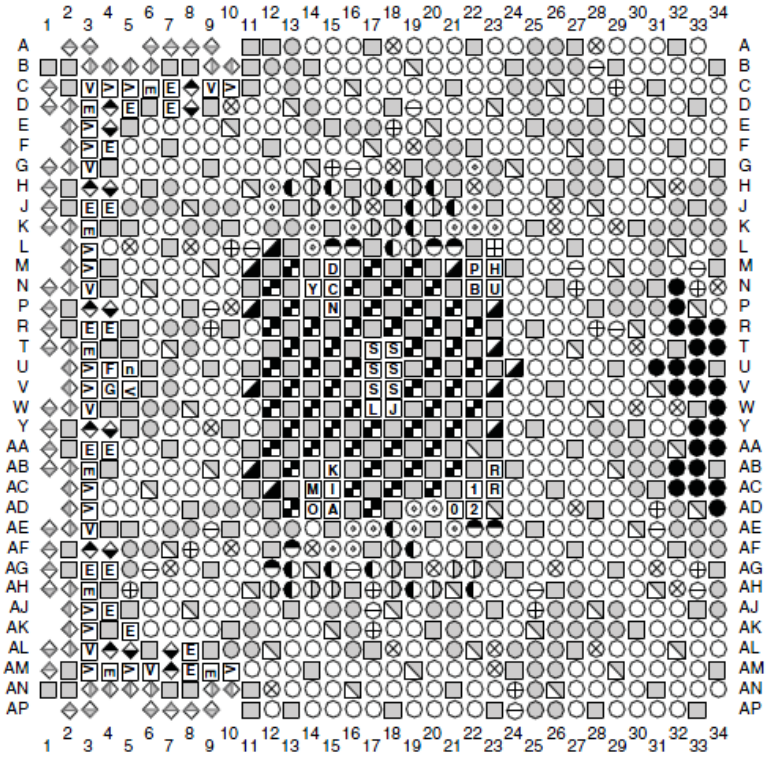
| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| | | | | 114 | | | | |
| 12 | IO_L18P_12 | N8 | NA | MGTAVTTTX_114 | P3 | 0 | VCCO_0 | J12 |
| 12 | IO_L18N_12 | P8 | NA | MGTTXN0_114 | R2 | 1 | VCCO_1 | B13 |
| 12 | IO_L19P_12 | R8 | NA | MGTRXP0_114 | R1 | 1 | VCCO_1 | E14 |
| 12 | IO_L19N_12 | R7 | NA | MGTAVTTRX_114 | R3 | 2 | VCCO_2 | AA16 |
| 13 | IO_L0P_SM8P_13 | P26 | NA | MGTRXN0_114 | T1 | 2 | VCCO_2 | AD17 |
| 13 | IO_L0N_SM8N_13 | R26 | NA | MGTAVCCPLL_114 | V3 | 3 | VCCO_3 | D17 |
| 13 | IO_L1P_SM7P_13 | P25 | NA | MGTRXN1_114 | U1 | 3 | VCCO_3 | G18 |
| 13 | IO_L1N_SM7N_13 | R25 | NA | MGTREFCLKN_114 | T3 | 4 | VCCO_4 | AB13 |
| 13 | IO_L2P_SM6P_13 | P24 | NA | MGTRXP1_114 | V1 | 4 | VCCO_4 | AE14 |
| 13 | IO_L2N_SM6N_13 | P23 | NA | MGTREFCLKP_114 | T4 | 11 | VCCO_11 | J22 |
| 13 | IO_L3P_SM5P_13 | R23 | NA | MGTTXN1_114 | V2 | 11 | VCCO_11 | M23 |
| 13 | IO_L3N_SM5N_13 | R22 | NA | MGTAVTTTX_114 | W3 | 11 | VCCO_11 | H25 |
| 13 | IO_L4P_13 | U26 | NA | MGTTXP1_114 | W2 | 12 | VCCO_12 | H5 |
| 13 | IO_L4N_VREF_13 | V26 | NA | MGTTXP0_116 | B2 | 12 | VCCO_12 | L6 |
| 13 | IO_L5P_SM4P_13 | U25 | NA | MGTAVTTTX_116 | B3 | 12 | VCCO_12 | P7 |
| 13 | IO_L5N_SM4N_13 | T25 | NA | MGTTXN0_116 | C2 | 13 | VCCO_13 | W22 |
| 13 | IO_L6P_SM3P_13 | T24 | NA | MGTRXP0_116 | C1 | 13 | VCCO_13 | R24 |
| 13 | IO_L6N_SM3N_13 | T23 | NA | MGTAVTTRX_116 | C3 | 13 | VCCO_13 | V25 |
| 13 | IO_L7P_SM2P_13 | U24 | NA | MGTRXN0_116 | D1 | 15 | VCCO_15 | F21 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 13 | IO_L7N_SM2N_13 | V24 | NA | MGTAVCCPLL_116 | F3 | 15 | VCCO_15 | B23 |
| 13 | IO_L8P_CC_SM1P_13 | W26 | NA | MGTRXN1_116 | E1 | 15 | VCCO_15 | E24 |
| 13 | IO_L8N_CC_SM1N_13 | W25 | NA | MGTREFCLKN_116 | D3 | 16 | VCCO_16 | D7 |
| 13 | IO_L9P_CC_SM0P_13 | W24 | NA | MGTRXP1_116 | F1 | 16 | VCCO_16 | G8 |
| 13 | IO_L9N_CC_SM0N_13 | V23 | NA | MGTREFCLKP_116 | D4 | 16 | VCCO_16 | C10 |
| 13 | IO_L10P_CC_13 | AA22 | NA | MGTTXN1_116 | F2 | 17 | VCCO_17 | AC20 |
| 13 | IO_L10N_CC_13 | Y22 | NA | MGTAVTTTX_116 | G3 | 17 | VCCO_17 | AB23 |
| 13 | IO_L11P_CC_13 | Y23 | NA | MGTTXP1_116 | G2 | 17 | VCCO_17 | AE24 |
| 13 | IO_L11N_CC_13 | W23 | NA | MGTTXP0_118 | Y2 | 18 | VCCO_18 | AA6 |
| 13 | IO_L12P_VRN_13 | Y26 | NA | MGTAVTTTX_118 | Y3 | 18 | VCCO_18 | AD7 |
| 13 | IO_L12N_VRP_13 | Y25 | NA | MGTTXN0_118 | AA2 | 18 | VCCO_18 | AC10 |
| 13 | IO_L13P_13 | AA25 | NA | MGTRXP0_118 | AA1 | NA | MGTAVCC_112 | L3 |
| 13 | IO_L13N_13 | AB26 | NA | MGTAVTTRX_118 | AA3 | NA | MGTAVCC_112 | L4 |
| 13 | IO_L14P_13 | AB25 | NA | MGTRXN0_118 | AB1 | NA | MGTAVCC_114 | U3 |
| 13 | IO_L14N_VREF_13 | AA24 | NA | MGTAVCCPLL_118 | AD3 | NA | MGTAVCC_114 | U4 |
| 13 | IO_L15P_13 | AB24 | NA | MGTRXN1_118 | AC1 | NA | MGTAVCC_116 | E3 |
| 13 | IO_L15N_13 | AA23 | NA | MGTREFCLKN_118 | AB3 | NA | MGTAVCC_116 | E4 |
| 13 | IO_L16P_13 | P21 | NA | MGTRXP1_118 | AD1 | NA | MGTAVCC_118 | AC3 |
| 13 | IO_L16N_13 | R21 | NA | MGTREFCLKP_118 | AB4 | NA | MGTAVCC_118 | AC4 |
| 13 | IO_L17P_13 | T22 | | | | NA | FLOAT | N4 |

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

As shown in Table 25, the BQ5VSX95T device is available in the CCGA1136 packages.



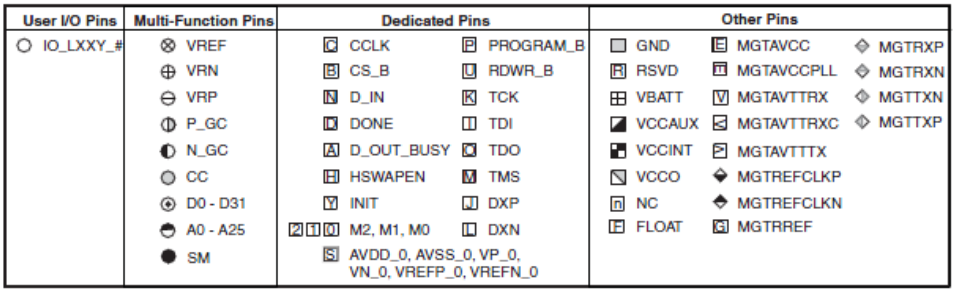



Table 25 BQ5VSX95T packages

| Bank | Pin Description | Pin Number |
|---|---|---|
| 0 | DXP_0 | W18 |
| 0 | DXN_0 | W17 |
| 0 | AVDD_0 | T18 |

| | | |
|---|---|---|
| 0 | AVSS_0 | T17 |
| 0 | VP_0 | U18 |
| 0 | VN_0 | V17 |
| 0 | VREFP_0 | V18 |
| 0 | VREFN_0 | U17 |
| 0 | VBATT_0 | L23 |
| 0 | PROGRAM_B_0 | M22 |
| 0 | HSWAPEN_0 | M23 |
| 0 | D_IN_0 | P15 |
| 0 | DONE_0 | M15 |
| 0 | CCLK_0 | N15 |
| 0 | INIT_B_0 | N14 |
| 0 | CS_B_0 | N22 |
| 0 | RDWR_B_0 | N23 |
| 0 | RSVD(3) | AB23 |
| 0 | RSVD(3) | AC23 |
| 0 | TCK_0 | AB15 |
| 0 | M0_0 | AD21 |
| 0 | M2_0 | AD22 |
| 0 | M1_0 | AC22 |
| 0 | TMS_0 | AC14 |
| 0 | TDI_0 | AC15 |
| 0 | D_OUT_BUSY_0 | AD15 |
| 0 | TDO_0 | AD14 |
| 1 | IO_L0P_A19_1 | L21 |
| 1 | IO_L0N_A18_1 | L20 |
| 1 | IO_L1P_A17_1 | L15 |
| 1 | IO_L1N_A16_1 | L16 |
| 1 | IO_L2P_A15_D31_1 | J22 |
| 1 | IO_L2N_A14_D30_1 | K21 |
| 1 | IO_L3P_A13_D29_1 | K16 |
| 1 | IO_L3N_A12_D28_1 | J15 |
| 1 | IO_L4P_A11_D27_1 | G22 |
| 1 | IO_L4N_VREF_A10_D26_1 | H22 |
| 1 | IO_L5P_A9_D25_1 | L14 |
| 1 | IO_L5N_A8_D24_1 | K14 |
| 1 | IO_L6P_A7_D23_1 | K23 |
| 1 | IO_L6N_A6_D22_1 | K22 |
| 1 | IO_L7P_A5_D21_1 | J12 |
| 1 | IO_L7N_A4_D20_1 | H12 |
| 1 | IO_L8P_CC_A3_D19_1 | G23 |
| 1 | IO_L8N_CC_A2_D18_1(2) | H23 |

| | | |
|---|---|---|
| 1 | IO_L9P_CC_A1_D17_1 | K13 |
| 1 | IO_L9N_CC_A0_D16_1(2) | K12 |
| 2 | IO_L0P_CC_RS1_2 | AE13 |
| 2 | IO_L0N_CC_RS0_2(2) | AE12 |
| 2 | IO_L1P_CC_A25_2 | AF23 |
| 2 | IO_L1N_CC_A24_2(2) | AG23 |
| 2 | IO_L2P_A23_2 | AF13 |
| 2 | IO_L2N_A22_2 | AG12 |
| 2 | IO_L3P_A21_2 | AE22 |
| 2 | IO_L3N_A20_2 | AE23 |
| 2 | IO_L4P_FCS_B_2 | AE14 |
| 2 | IO_L4N_VREF_FOE_B_MOSI_2 | AF14 |
| 2 | IO_L5P_FWE_B_2 | AF20 |
| 2 | IO_L5N_CSO_B_2 | AF21 |
| 2 | IO_L6P_D7_2 | AF15 |
| 2 | IO_L6N_D6_2 | AE16 |
| 2 | IO_L7P_D5_2 | AE21 |
| 2 | IO_L7N_D4_2 | AD20 |
| 2 | IO_L8P_D3_2 | AF16 |
| 2 | IO_L8N_D2_FS2_2 | AE17 |
| 2 | IO_L9P_D1_FS1_2 | AE19 |
| 2 | IO_L9N_D0_FS0_2 | AD19 |
| 3 | IO_L0P_CC_GC_3 | H17 |
| 3 | IO_L0N_CC_GC_3(1)(2) | H18 |
| 3 | IO_L1P_CC_GC_3 | K17 |
| 3 | IO_L1N_CC_GC_3(1)(2) | L18 |
| 3 | IO_L2P_GC_VRN_3 | G15 |
| 3 | IO_L2N_GC_VRP_3(1) | G16 |
| 3 | IO_L3P_GC_3 | K18 |
| 3 | IO_L3N_GC_3(1) | J19 |
| 3 | IO_L4P_GC_3 | J16 |
| 3 | IO_L4N_GC_VREF_3(1) | J17 |
| 3 | IO_L5P_GC_3 | L19 |
| 3 | IO_L5N_GC_3(1) | K19 |
| 3 | IO_L6P_GC_3 | H14 |
| 3 | IO_L6N_GC_3(1) | H15 |
| 3 | IO_L7P_GC_3 | J20 |
| 3 | IO_L7N_GC_3(1) | J21 |
| 3 | IO_L8P_GC_3 | J14 |
| 3 | IO_L8N_GC_3(1) | H13 |
| 3 | IO_L9P_GC_3 | H19 |
| 3 | IO_L9N_GC_3(1) | H20 |

| | | |
|---|---|---|
| 4 | IO_L0P_GC_D15_4 | AG22 |
| 4 | IO_L0N_GC_D14_4(1) | AH22 |
| 4 | IO_L1P_GC_D13_4 | AH12 |
| 4 | IO_L1N_GC_D12_4(1) | AG13 |
| 4 | IO_L2P_GC_D11_4 | AH20 |
| 4 | IO_L2N_GC_D10_4(1) | AH19 |
| 4 | IO_L3P_GC_D9_4 | AH14 |
| 4 | IO_L3N_GC_D8_4(1) | AH13 |
| 4 | IO_L4P_GC_4 | AG21 |
| 4 | IO_L4N_GC_VREF_4(1) | AG20 |
| 4 | IO_L5P_GC_4 | AH15 |
| 4 | IO_L5N_GC_4(1) | AG15 |
| 4 | IO_L6P_GC_4 | AG18 |
| 4 | IO_L6N_GC_4(1) | AF19 |
| 4 | IO_L7P_GC_VRN_4 | AH17 |
| 4 | IO_L7N_GC_VRP_4(1) | AG16 |
| 4 | IO_L8P_CC_GC_4 | AF18 |
| 4 | IO_L8N_CC_GC_4(1)(2) | AE18 |
| 4 | IO_L9P_CC_GC_4 | AH18 |
| 4 | IO_L9N_CC_GC_4(1)(2) | AG17 |
| 5 | IO_L0P_5 | B16 |
| 5 | IO_L0N_5 | B15 |
| 5 | IO_L1P_5 | A15 |
| 5 | IO_L1N_5 | A14 |
| 5 | IO_L2P_5 | B17 |
| 5 | IO_L2N_5 | A16 |
| 5 | IO_L3P_5 | C14 |
| 5 | IO_L3N_5 | C15 |
| 5 | IO_L4P_5 | E19 |
| 5 | IO_L4N_VREF_5 | F19 |
| 5 | IO_L5P_5 | C17 |
| 5 | IO_L5N_5 | D17 |
| 5 | IO_L6P_5 | E21 |
| 5 | IO_L6N_5 | D20 |
| 5 | IO_L7P_5 | D16 |
| 5 | IO_L7N_5 | D15 |
| 5 | IO_L8P_CC_5 | G20 |
| 5 | IO_L8N_CC_5(2) | F20 |
| 5 | IO_L9P_CC_5 | D14 |
| 5 | IO_L9N_CC_5(2) | E14 |
| 5 | IO_L10P_CC_5 | E17 |
| 5 | IO_L10N_CC_5(2) | E16 |

| | | |
|---|---|---|
| 5 | IO_L11P_CC_5 | F21 |
| 5 | IO_L11N_CC_5(2) | G21 |
| 5 | IO_L12P_VRN_5 | E18 |
| 5 | IO_L12N_VRP_5 | D19 |
| 5 | IO_L13P_5 | D21 |
| 5 | IO_L13N_5 | D22 |
| 5 | IO_L14P_5 | F18 |
| 5 | IO_L14N_VREF_5 | G18 |
| 5 | IO_L15P_5 | E22 |
| 5 | IO_L15N_5 | F23 |
| 5 | IO_L16P_5 | G17 |
| 5 | IO_L16N_5 | F16 |
| 5 | IO_L17P_5 | D24 |
| 5 | IO_L17N_5 | E23 |
| 5 | IO_L18P_5 | F14 |
| 5 | IO_L18N_5 | F15 |
| 5 | IO_L19P_5 | F24 |
| 5 | IO_L19N_5 | E24 |
| 6 | IO_L0P_6 | AH24 |
| 6 | IO_L0N_6 | AJ24 |
| 6 | IO_L1P_6 | AK12 |
| 6 | IO_L1N_6 | AJ12 |
| 6 | IO_L2P_6 | AH23 |
| 6 | IO_L2N_6 | AJ22 |
| 6 | IO_L3P_6 | AL13 |
| 6 | IO_L3N_6 | AK13 |
| 6 | IO_L4P_6 | AK24 |
| 6 | IO_L4N_VREF_6 | AL23 |
| 6 | IO_L5P_6 | AJ14 |
| 6 | IO_L5N_6 | AK14 |
| 6 | IO_L6P_6 | AK23 |
| 6 | IO_L6N_6 | AK22 |
| 6 | IO_L7P_6 | AL15 |
| 6 | IO_L7N_6 | AL14 |
| 6 | IO_L8P_CC_6 | AJ21 |
| 6 | IO_L8N_CC_6(2) | AJ20 |
| 6 | IO_L9P_CC_6 | AJ16 |
| 6 | IO_L9N_CC_6(2) | AJ15 |
| 6 | IO_L10P_CC_6 | AK16 |
| 6 | IO_L10N_CC_6(2) | AL16 |
| 6 | IO_L11P_CC_6 | AL21 |
| 6 | IO_L11N_CC_6(2) | AK21 |

| | | |
|---|---|---|
| 6 | IO_L12P_VRN_6 | AK17 |
| 6 | IO_L12N_VRP_6 | AJ17 |
| 6 | IO_L13P_6 | AL19 |
| 6 | IO_L13N_6 | AL20 |
| 6 | IO_L14P_6 | AK18 |
| 6 | IO_L14N_VREF_6 | AL18 |
| 6 | IO_L15P_6 | AJ19 |
| 6 | IO_L15N_6 | AK19 |
| 6 | IO_L16P_6 | AM15 |
| 6 | IO_L16N_6 | AM16 |
| 6 | IO_L17P_6 | AP16 |
| 6 | IO_L17N_6 | AP17 |
| 6 | IO_L18P_6 | AN15 |
| 6 | IO_L18N_6 | AP15 |
| 6 | IO_L19P_6 | AM17 |
| 6 | IO_L19N_6 | AN17 |
| 11 | IO_L0P_11 | B32 |
| 11 | IO_L0N_11 | A33 |
| 11 | IO_L1P_11 | B33 |
| 11 | IO_L1N_11 | C33 |
| 11 | IO_L2P_11 | C32 |
| 11 | IO_L2N_11 | D32 |
| 11 | IO_L3P_11 | C34 |
| 11 | IO_L3N_11 | D34 |
| 11 | IO_L4P_11 | G32 |
| 11 | IO_L4N_VREF_11 | H32 |
| 11 | IO_L5P_11 | F33 |
| 11 | IO_L5N_11 | E34 |
| 11 | IO_L6P_11 | E32 |
| 11 | IO_L6N_11 | E33 |
| 11 | IO_L7P_11 | G33 |
| 11 | IO_L7N_11 | F34 |
| 11 | IO_L8P_CC_11 | J32 |
| 11 | IO_L8N_CC_11(2) | H33 |
| 11 | IO_L9P_CC_11 | H34 |
| 11 | IO_L9N_CC_11(2) | J34 |
| 11 | IO_L10P_CC_SM15P_11 | L34 |
| 11 | IO_L10N_CC_SM15N_11(2) | K34 |
| 11 | IO_L11P_CC_SM14P_11 | K33 |
| 11 | IO_L11N_CC_SM14N_11(2) | K32 |
| 11 | IO_L12P_VRN_11 | N33 |
| 11 | IO_L12N_VRP_11 | M33 |

| | | |
|---|---|---|
| 11 | IO_L13P_11 | L33 |
| 11 | IO_L13N_11 | M32 |
| 11 | IO_L14P_11 | P34 |
| 11 | IO_L14N_VREF_11 | N34 |
| 11 | IO_L15P_SM13P_11 | P32 |
| 11 | IO_L15N_SM13N_11 | N32 |
| 11 | IO_L16P_SM12P_11 | T33 |
| 11 | IO_L16N_SM12N_11 | R34 |
| 11 | IO_L17P_SM11P_11 | R33 |
| 11 | IO_L17N_SM11N_11 | R32 |
| 11 | IO_L18P_SM10P_11 | U33 |
| 11 | IO_L18N_SM10N_11 | T34 |
| 11 | IO_L19P_SM9P_11 | U32 |
| 11 | IO_L19N_SM9N_11 | U31 |
| 12 | IO_L0P_12 | M6 |
| 12 | IO_L0N_12 | M5 |
| 12 | IO_L1P_12 | N8 |
| 12 | IO_L1N_12 | N7 |
| 12 | IO_L2P_12 | M7 |
| 12 | IO_L2N_12 | L6 |
| 12 | IO_L3P_12 | N5 |
| 12 | IO_L3N_12 | P5 |
| 12 | IO_L4P_12 | L4 |
| 12 | IO_L4N_VREF_12 | L5 |
| 12 | IO_L5P_12 | P7 |
| 12 | IO_L5N_12 | P6 |
| 12 | IO_L6P_12 | K7 |
| 12 | IO_L6N_12 | K6 |
| 12 | IO_L7P_12 | R6 |
| 12 | IO_L7N_12 | T6 |
| 12 | IO_L8P_CC_12 | J6 |
| 12 | IO_L8N_CC_12(2) | J5 |
| 12 | IO_L9P_CC_12 | R7 |
| 12 | IO_L9N_CC_12(2) | R8 |
| 12 | IO_L10P_CC_12 | T8 |
| 12 | IO_L10N_CC_12(2) | U7 |
| 12 | IO_L11P_CC_12 | H7 |
| 12 | IO_L11N_CC_12(2) | J7 |
| 12 | IO_L12P_VRN_12 | R9 |
| 12 | IO_L12N_VRP_12 | P9 |
| 12 | IO_L13P_12 | H5 |
| 12 | IO_L13N_12 | G5 |

| | | |
|---|---|---|
| 12 | IO_L14P_12 | R11 |
| 12 | IO_L14N_VREF_12 | P10 |
| 12 | IO_L15P_12 | F5 |
| 12 | IO_L15N_12 | F6 |
| 12 | IO_L16P_12 | T10 |
| 12 | IO_L16N_12 | T11 |
| 12 | IO_L17P_12 | G6 |
| 12 | IO_L17N_12 | G7 |
| 12 | IO_L18P_12 | T9 |
| 12 | IO_L18N_12 | U10 |
| 12 | IO_L19P_12 | E6 |
| 12 | IO_L19N_12 | E7 |
| 13 | IO_L0P_SM8P_13 | V32 |
| 13 | IO_L0N_SM8N_13 | V33 |
| 13 | IO_L1P_SM7P_13 | W34 |
| 13 | IO_L1N_SM7N_13 | V34 |
| 13 | IO_L2P_SM6P_13 | Y33 |
| 13 | IO_L2N_SM6N_13 | AA33 |
| 13 | IO_L3P_SM5P_13 | AA34 |
| 13 | IO_L3N_SM5N_13 | Y34 |
| 13 | IO_L4P_13 | Y32 |
| 13 | IO_L4N_VREF_13 | W32 |
| 13 | IO_L5P_SM4P_13 | AC34 |
| 13 | IO_L5N_SM4N_13 | AD34 |
| 13 | IO_L6P_SM3P_13 | AC32 |
| 13 | IO_L6N_SM3N_13 | AB32 |
| 13 | IO_L7P_SM2P_13 | AC33 |
| 13 | IO_L7N_SM2N_13 | AB33 |
| 13 | IO_L8P_CC_SM1P_13 | AF33 |
| 13 | IO_L8N_CC_SM1N_13(2) | AE33 |
| 13 | IO_L9P_CC_SM0P_13 | AF34 |
| 13 | IO_L9N_CC_SM0N_13(2) | AE34 |
| 13 | IO_L10P_CC_13 | AH34 |
| 13 | IO_L10N_CC_13(2) | AJ34 |
| 13 | IO_L11P_CC_13 | AD32 |
| 13 | IO_L11N_CC_13(2) | AE32 |
| 13 | IO_L12P_VRN_13 | AG33 |
| 13 | IO_L12N_VRP_13 | AH33 |
| 13 | IO_L13P_13 | AK34 |
| 13 | IO_L13N_13 | AK33 |
| 13 | IO_L14P_13 | AG32 |
| 13 | IO_L14N_VREF_13 | AH32 |

| | | |
|---|---|---|
| 13 | IO_L15P_13 | AJ32 |
| 13 | IO_L15N_13 | AK32 |
| 13 | IO_L16P_13 | AL34 |
| 13 | IO_L16N_13 | AL33 |
| 13 | IO_L17P_13 | AM33 |
| 13 | IO_L17N_13 | AM32 |
| 13 | IO_L18P_13 | AN34 |
| 13 | IO_L18N_13 | AN33 |
| 13 | IO_L19P_13 | AN32 |
| 13 | IO_L19N_13 | AP32 |
| 15 | IO_L0P_15 | E29 |
| 15 | IO_L0N_15 | F29 |
| 15 | IO_L1P_15 | G30 |
| 15 | IO_L1N_15 | F30 |
| 15 | IO_L2P_15 | H29 |
| 15 | IO_L2N_15 | J29 |
| 15 | IO_L3P_15 | F31 |
| 15 | IO_L3N_15 | E31 |
| 15 | IO_L4P_15 | L29 |
| 15 | IO_L4N_VREF_15 | K29 |
| 15 | IO_L5P_15 | H30 |
| 15 | IO_L5N_15 | G31 |
| 15 | IO_L6P_15 | J30 |
| 15 | IO_L6N_15 | J31 |
| 15 | IO_L7P_15 | L30 |
| 15 | IO_L7N_15 | M30 |
| 15 | IO_L8P_CC_15 | N29 |
| 15 | IO_L8N_CC_15(2) | P29 |
| 15 | IO_L9P_CC_15 | K31 |
| 15 | IO_L9N_CC_15(2) | L31 |
| 15 | IO_L10P_CC_15 | P31 |
| 15 | IO_L10N_CC_15(2) | P30 |
| 15 | IO_L11P_CC_15 | M31 |
| 15 | IO_L11N_CC_15(2) | N30 |
| 15 | IO_L12P_VRN_15 | R28 |
| 15 | IO_L12N_VRP_15 | R29 |
| 15 | IO_L13P_15 | T31 |
| 15 | IO_L13N_15 | R31 |
| 15 | IO_L14P_15 | U30 |
| 15 | IO_L14N_VREF_15 | T30 |
| 15 | IO_L15P_15 | T28 |
| 15 | IO_L15N_15 | T29 |

| | | |
|---|---|---|
| 15 | IO_L16P_15 | U27 |
| 15 | IO_L16N_15 | U28 |
| 15 | IO_L17P_15 | R26 |
| 15 | IO_L17N_15 | R27 |
| 15 | IO_L18P_15 | U26 |
| 15 | IO_L18N_15 | T26 |
| 15 | IO_L19P_15 | U25 |
| 15 | IO_L19N_15 | T25 |
| 17 | IO_L0P_17 | W24 |
| 17 | IO_L0N_17 | V24 |
| 17 | IO_L1P_17 | Y26 |
| 17 | IO_L1N_17 | W26 |
| 17 | IO_L2P_17 | V25 |
| 17 | IO_L2N_17 | W25 |
| 17 | IO_L3P_17 | Y27 |
| 17 | IO_L3N_17 | W27 |
| 17 | IO_L4P_17 | V30 |
| 17 | IO_L4N_VREF_17 | W30 |
| 17 | IO_L5P_17 | V28 |
| 17 | IO_L5N_17 | V27 |
| 17 | IO_L6P_17 | W31 |
| 17 | IO_L6N_17 | Y31 |
| 17 | IO_L7P_17 | W29 |
| 17 | IO_L7N_17 | V29 |
| 17 | IO_L8P_CC_17 | Y28 |
| 17 | IO_L8N_CC_17(2) | Y29 |
| 17 | IO_L9P_CC_17 | AB31 |
| 17 | IO_L9N_CC_17(2) | AA31 |
| 17 | IO_L10P_CC_17 | AB30 |
| 17 | IO_L10N_CC_17(2) | AC30 |
| 17 | IO_L11P_CC_17 | AA29 |
| 17 | IO_L11N_CC_17(2) | AA30 |
| 17 | IO_L12P_VRN_17 | AD31 |
| 17 | IO_L12N_VRP_17 | AE31 |
| 17 | IO_L13P_17 | AD30 |
| 17 | IO_L13N_17 | AC29 |
| 17 | IO_L14P_17 | AF31 |
| 17 | IO_L14N_VREF_17 | AG31 |
| 17 | IO_L15P_17 | AE29 |
| 17 | IO_L15N_17 | AD29 |
| 17 | IO_L16P_17 | AJ31 |
| 17 | IO_L16N_17 | AK31 |

| | | |
|---|---|---|
| 17 | IO_L17P_17 | AF29 |
| 17 | IO_L17N_17 | AF30 |
| 17 | IO_L18P_17 | AJ30 |
| 17 | IO_L18N_17 | AH30 |
| 17 | IO_L19P_17 | AH29 |
| 17 | IO_L19N_17 | AG30 |
| 18 | IO_L0P_18 | AC4 |
| 18 | IO_L0N_18 | AC5 |
| 18 | IO_L1P_18 | AB6 |
| 18 | IO_L1N_18 | AB7 |
| 18 | IO_L2P_18 | AA5 |
| 18 | IO_L2N_18 | AB5 |
| 18 | IO_L3P_18 | AC7 |
| 18 | IO_L3N_18 | AD7 |
| 18 | IO_L4P_18 | Y8 |
| 18 | IO_L4N_VREF_18 | Y9 |
| 18 | IO_L5P_18 | AD4 |
| 18 | IO_L5N_18 | AD5 |
| 18 | IO_L6P_18 | AA6 |
| 18 | IO_L6N_18 | Y7 |
| 18 | IO_L7P_18 | AD6 |
| 18 | IO_L7N_18 | AE6 |
| 18 | IO_L8P_CC_18 | W6 |
| 18 | IO_L8N_CC_18(2) | Y6 |
| 18 | IO_L9P_CC_18 | AE7 |
| 18 | IO_L9N_CC_18(2) | AF6 |
| 18 | IO_L10P_CC_18 | AG5 |
| 18 | IO_L10N_CC_18(2) | AF5 |
| 18 | IO_L11P_CC_18 | W7 |
| 18 | IO_L11N_CC_18(2) | V7 |
| 18 | IO_L12P_VRN_18 | AH5 |
| 18 | IO_L12N_VRP_18 | AG6 |
| 18 | IO_L13P_18 | Y11 |
| 18 | IO_L13N_18 | W11 |
| 18 | IO_L14P_18 | AH7 |
| 18 | IO_L14N_VREF_18 | AG7 |
| 18 | IO_L15P_18 | W10 |
| 18 | IO_L15N_18 | W9 |
| 18 | IO_L16P_18 | AJ7 |
| 18 | IO_L16N_18 | AJ6 |
| 18 | IO_L17P_18 | V8 |
| 18 | IO_L17N_18 | U8 |

| | | |
|---|---|---|
| 18 | IO_L18P_18 | AK7 |
| 18 | IO_L18N_18 | AK6 |
| 18 | IO_L19P_18 | V10 |
| 18 | IO_L19N_18 | V9 |
| 19 | IO_L0P_19 | K24 |
| 19 | IO_L0N_19 | L24 |
| 19 | IO_L1P_19 | L25 |
| 19 | IO_L1N_19 | L26 |
| 19 | IO_L2P_19 | J24 |
| 19 | IO_L2N_19 | J25 |
| 19 | IO_L3P_19 | M25 |
| 19 | IO_L3N_19 | M26 |
| 19 | IO_L4P_19 | J27 |
| 19 | IO_L4N_VREF_19 | J26 |
| 19 | IO_L5P_19 | G25 |
| 19 | IO_L5N_19 | G26 |
| 19 | IO_L6P_19 | H25 |
| 19 | IO_L6N_19 | H24 |
| 19 | IO_L7P_19 | F25 |
| 19 | IO_L7N_19 | F26 |
| 19 | IO_L8P_CC_19 | G27 |
| 19 | IO_L8N_CC_19(2) | H27 |
| 19 | IO_L9P_CC_19 | H28 |
| 19 | IO_L9N_CC_19(2) | G28 |
| 19 | IO_L10P_CC_19 | E28 |
| 19 | IO_L10N_CC_19(2) | F28 |
| 19 | IO_L11P_CC_19 | E26 |
| 19 | IO_L11N_CC_19(2) | E27 |
| 19 | IO_L12P_VRN_19 | N27 |
| 19 | IO_L12N_VRP_19 | M27 |
| 19 | IO_L13P_19 | K28 |
| 19 | IO_L13N_19 | L28 |
| 19 | IO_L14P_19 | K27 |
| 19 | IO_L14N_VREF_19 | K26 |
| 19 | IO_L15P_19 | M28 |
| 19 | IO_L15N_19 | N28 |
| 19 | IO_L16P_19 | P26 |
| 19 | IO_L16N_19 | P27 |
| 19 | IO_L17P_19 | N24 |
| 19 | IO_L17N_19 | P24 |
| 19 | IO_L18P_19 | P25 |
| 19 | IO_L18N_19 | N25 |

| | | |
|---|---|---|
| 19 | IO_L19P_19 | R24 |
| 19 | IO_L19N_19 | T24 |
| 20 | IO_L0P_20 | E9 |
| 20 | IO_L0N_20 | E8 |
| 20 | IO_L1P_20 | F9 |
| 20 | IO_L1N_20 | F8 |
| 20 | IO_L2P_20 | F10 |
| 20 | IO_L2N_20 | G10 |
| 20 | IO_L3P_20 | G8 |
| 20 | IO_L3N_20 | H8 |
| 20 | IO_L4P_20 | D11 |
| 20 | IO_L4N_VREF_20 | D10 |
| 20 | IO_L5P_20 | K11 |
| 20 | IO_L5N_20 | J11 |
| 20 | IO_L6P_20 | D12 |
| 20 | IO_L6N_20 | C12 |
| 20 | IO_L7P_20 | H10 |
| 20 | IO_L7N_20 | H9 |
| 20 | IO_L8P_CC_20 | A13 |
| 20 | IO_L8N_CC_20(2) | B12 |
| 20 | IO_L9P_CC_20 | J10 |
| 20 | IO_L9N_CC_20(2) | J9 |
| 20 | IO_L10P_CC_20 | K8 |
| 20 | IO_L10N_CC_20(2) | K9 |
| 20 | IO_L11P_CC_20 | B13 |
| 20 | IO_L11N_CC_20(2) | C13 |
| 20 | IO_L12P_VRN_20 | L10 |
| 20 | IO_L12N_VRP_20 | L11 |
| 20 | IO_L13P_20 | G11 |
| 20 | IO_L13N_20 | G12 |
| 20 | IO_L14P_20 | M8 |
| 20 | IO_L14N_VREF_20 | L8 |
| 20 | IO_L15P_20 | F11 |
| 20 | IO_L15N_20 | E11 |
| 20 | IO_L16P_20 | M10 |
| 20 | IO_L16N_20 | L9 |
| 20 | IO_L17P_20 | E12 |
| 20 | IO_L17N_20 | E13 |
| 20 | IO_L18P_20 | N10 |
| 20 | IO_L18N_20 | N9 |
| 20 | IO_L19P_20 | F13 |
| 20 | IO_L19N_20 | G13 |

| | | |
|---|---|---|
| 21 | IO_L0P_21 | AA25 |
| 21 | IO_L0N_21 | AA26 |
| 21 | IO_L1P_21 | AB27 |
| 21 | IO_L1N_21 | AC27 |
| 21 | IO_L2P_21 | Y24 |
| 21 | IO_L2N_21 | AA24 |
| 21 | IO_L3P_21 | AB25 |
| 21 | IO_L3N_21 | AB26 |
| 21 | IO_L4P_21 | AC28 |
| 21 | IO_L4N_VREF_21 | AD27 |
| 21 | IO_L5P_21 | AB28 |
| 21 | IO_L5N_21 | AA28 |
| 21 | IO_L6P_21 | AG28 |
| 21 | IO_L6N_21 | AH28 |
| 21 | IO_L7P_21 | AE28 |
| 21 | IO_L7N_21 | AF28 |
| 21 | IO_L8P_CC_21 | AK26 |
| 21 | IO_L8N_CC_21(2) | AJ27 |
| 21 | IO_L9P_CC_21 | AK29 |
| 21 | IO_L9N_CC_21(2) | AJ29 |
| 21 | IO_L10P_CC_21 | AK28 |
| 21 | IO_L10N_CC_21(2) | AK27 |
| 21 | IO_L11P_CC_21 | AH27 |
| 21 | IO_L11N_CC_21(2) | AJ26 |
| 21 | IO_L12P_VRN_21 | AJ25 |
| 21 | IO_L12N_VRP_21 | AH25 |
| 21 | IO_L13P_21 | AF24 |
| 21 | IO_L13N_21 | AG25 |
| 21 | IO_L14P_21 | AG27 |
| 21 | IO_L14N_VREF_21 | AG26 |
| 21 | IO_L15P_21 | AF25 |
| 21 | IO_L15N_21 | AF26 |
| 21 | IO_L16P_21 | AE27 |
| 21 | IO_L16N_21 | AE26 |
| 21 | IO_L17P_21 | AC25 |
| 21 | IO_L17N_21 | AC24 |
| 21 | IO_L18P_21 | AD26 |
| 21 | IO_L18N_21 | AD25 |
| 21 | IO_L19P_21 | AD24 |
| 21 | IO_L19N_21 | AE24 |
| 22 | IO_L0P_22 | AN14 |
| 22 | IO_L0N_22 | AP14 |

| | | |
|---|---|---|
| 22 | IO_L1P_22 | AB10 |
| 22 | IO_L1N_22 | AA10 |
| 22 | IO_L2P_22 | AN13 |
| 22 | IO_L2N_22 | AM13 |
| 22 | IO_L3P_22 | AA8 |
| 22 | IO_L3N_22 | AA9 |
| 22 | IO_L4P_22 | AP12 |
| 22 | IO_L4N_VREF_22 | AN12 |
| 22 | IO_L5P_22 | AC8 |
| 22 | IO_L5N_22 | AB8 |
| 22 | IO_L6P_22 | AM12 |
| 22 | IO_L6N_22 | AM11 |
| 22 | IO_L7P_22 | AC10 |
| 22 | IO_L7N_22 | AC9 |
| 22 | IO_L8P_CC_22 | AL11 |
| 22 | IO_L8N_CC_22(2) | AL10 |
| 22 | IO_L9P_CC_22 | AE8 |
| 22 | IO_L9N_CC_22(2) | AD9 |
| 22 | IO_L10P_CC_22 | AD10 |
| 22 | IO_L10N_CC_22(2) | AD11 |
| 22 | IO_L11P_CC_22 | AK11 |
| 22 | IO_L11N_CC_22(2) | AJ11 |
| 22 | IO_L12P_VRN_22 | AF8 |
| 22 | IO_L12N_VRP_22 | AE9 |
| 22 | IO_L13P_22 | AK8 |
| 22 | IO_L13N_22 | AK9 |
| 22 | IO_L14P_22 | AF9 |
| 22 | IO_L14N_VREF_22 | AF10 |
| 22 | IO_L15P_22 | AJ9 |
| 22 | IO_L15N_22 | AJ10 |
| 22 | IO_L16P_22 | AF11 |
| 22 | IO_L16N_22 | AE11 |
| 22 | IO_L17P_22 | AH9 |
| 22 | IO_L17N_22 | AH10 |
| 22 | IO_L18P_22 | AG8 |
| 22 | IO_L18N_22 | AH8 |
| 22 | IO_L19P_22 | AG10 |
| 22 | IO_L19N_22 | AG11 |
| 23 | IO_L0P_23 | C20 |
| 23 | IO_L0N_23 | B20 |
| 23 | IO_L1P_23 | B21 |
| 23 | IO_L1N_23 | A21 |

| | | |
|---|---|---|
| 23 | IO_L2P_23 | C19 |
| 23 | IO_L2N_23 | C18 |
| 23 | IO_L3P_23 | C22 |
| 23 | IO_L3N_23 | B22 |
| 23 | IO_L4P_23 | B18 |
| 23 | IO_L4N_VREF_23 | A18 |
| 23 | IO_L5P_23 | C23 |
| 23 | IO_L5N_23 | B23 |
| 23 | IO_L6P_23 | A19 |
| 23 | IO_L6N_23 | A20 |
| 23 | IO_L7P_23 | A23 |
| 23 | IO_L7N_23 | A24 |
| 23 | IO_L8P_CC_23 | C24 |
| 23 | IO_L8N_CC_23(2) | D25 |
| 23 | IO_L9P_CC_23 | B26 |
| 23 | IO_L9N_CC_23(2) | A25 |
| 23 | IO_L10P_CC_23 | B27 |
| 23 | IO_L10N_CC_23(2) | A26 |
| 23 | IO_L11P_CC_23 | B25 |
| 23 | IO_L11N_CC_23(2) | C25 |
| 23 | IO_L12P_VRN_23 | C29 |
| 23 | IO_L12N_VRP_23 | B28 |
| 23 | IO_L13P_23 | D26 |
| 23 | IO_L13N_23 | C27 |
| 23 | IO_L14P_23 | A29 |
| 23 | IO_L14N_VREF_23 | A28 |
| 23 | IO_L15P_23 | C28 |
| 23 | IO_L15N_23 | D27 |
| 23 | IO_L16P_23 | B31 |
| 23 | IO_L16N_23 | A31 |
| 23 | IO_L17P_23 | C30 |
| 23 | IO_L17N_23 | D29 |
| 23 | IO_L18P_23 | D31 |
| 23 | IO_L18N_23 | D30 |
| 23 | IO_L19P_23 | A30 |
| 23 | IO_L19N_23 | B30 |
| 25 | IO_L0P_25 | AL29 |
| 25 | IO_L0N_25 | AL30 |
| 25 | IO_L1P_25 | AM31 |
| 25 | IO_L1N_25 | AL31 |
| 25 | IO_L2P_25 | AN30 |
| 25 | IO_L2N_25 | AM30 |

| | | |
|---|---|---|
| 25 | IO_L3P_25 | AP30 |
| 25 | IO_L3N_25 | AP31 |
| 25 | IO_L4P_25 | AM27 |
| 25 | IO_L4N_VREF_25 | AL28 |
| 25 | IO_L5P_25 | AP29 |
| 25 | IO_L5N_25 | AN29 |
| 25 | IO_L6P_25 | AP27 |
| 25 | IO_L6N_25 | AN27 |
| 25 | IO_L7P_25 | AN28 |
| 25 | IO_L7N_25 | AM28 |
| 25 | IO_L8P_CC_25 | AN25 |
| 25 | IO_L8N_CC_25(2) | AM25 |
| 25 | IO_L9P_CC_25 | AM26 |
| 25 | IO_L9N_CC_25(2) | AL26 |
| 25 | IO_L10P_CC_25 | AP26 |
| 25 | IO_L10N_CC_25(2) | AP25 |
| 25 | IO_L11P_CC_25 | AL25 |
| 25 | IO_L11N_CC_25(2) | AL24 |
| 25 | IO_L12P_VRN_25 | AN24 |
| 25 | IO_L12N_VRP_25 | AP24 |
| 25 | IO_L13P_25 | AM21 |
| 25 | IO_L13N_25 | AM20 |
| 25 | IO_L14P_25 | AN23 |
| 25 | IO_L14N_VREF_25 | AM23 |
| 25 | IO_L15P_25 | AN20 |
| 25 | IO_L15N_25 | AP20 |
| 25 | IO_L16P_25 | AN22 |
| 25 | IO_L16N_25 | AM22 |
| 25 | IO_L17P_25 | AN18 |
| 25 | IO_L17N_25 | AM18 |
| 25 | IO_L18P_25 | AP22 |
| 25 | IO_L18N_25 | AP21 |
| 25 | IO_L19P_25 | AN19 |
| 25 | IO_L19N_25 | AP19 |
| NA | MGTTXP0_112 | M2 |
| NA | MGTAVTTTX_112 | M3 |
| NA | MGTTXN0_112 | N2 |
| NA | MGTRXP0_112 | N1 |
| NA | MGTAVTTRX_112 | N3 |
| NA | MGTRXN0_112 | P1 |
| NA | MGTAVCCPLL_112 | T3 |
| NA | MGTRXN1_112 | R1 |

| | | |
|---|---|---|
| NA | MGTREFCLKN_112 | P3 |
| NA | MGTRXP1_112 | T1 |
| NA | MGTREFCLKP_112 | P4 |
| NA | MGTTXN1_112 | T2 |
| NA | MGTAVTTTX_112 | U3 |
| NA | MGTTXP1_112 | U2 |
| NA | MGTAVTTRXC | V5 |
| NA | MGTRREF_112 | V4 |
| NA | MGTTXP0_114 | V2 |
| NA | MGTAVTTTX_114 | AC3 |
| NA | MGTTXN0_114 | W2 |
| NA | MGTRXP0_114 | W1 |
| NA | MGTAVTTRX_114 | W3 |
| NA | MGTRXN0_114 | Y1 |
| NA | MGTAVCCPLL_114 | AB3 |
| NA | MGTRXN1_114 | AA1 |
| NA | MGTREFCLKN_114 | Y3 |
| NA | MGTRXP1_114 | AB1 |
| NA | MGTREFCLKP_114 | Y4 |
| NA | MGTTXN1_114 | AB2 |
| NA | MGTAVTTTX_114 | V3 |
| NA | MGTTXP1_114 | AC2 |
| NA | MGTTXP0_116 | F2 |
| NA | MGTAVTTTX_116 | F3 |
| NA | MGTTXN0_116 | G2 |
| NA | MGTRXP0_116 | G1 |
| NA | MGTAVTTRX_116 | G3 |
| NA | MGTRXN0_116 | H1 |
| NA | MGTAVCCPLL_116 | K3 |
| NA | MGTRXN1_116 | J1 |
| NA | MGTREFCLKN_116 | H3 |
| NA | MGTRXP1_116 | K1 |
| NA | MGTREFCLKP_116 | H4 |
| NA | MGTTXN1_116 | K2 |
| NA | MGTAVTTTX_116 | L3 |
| NA | MGTTXP1_116 | L2 |
| NA | MGTTXP0_118 | AD2 |
| NA | MGTAVTTTX_118 | AD3 |
| NA | MGTTXN0_118 | AE2 |
| NA | MGTRXP0_118 | AE1 |
| NA | MGTAVTTRX_118 | AE3 |
| NA | MGTRXN0_118 | AF1 |

| | | |
|---|---|---|
| NA | MGTAVCCPLL_118 | AH3 |
| NA | MGTRXN1_118 | AG1 |
| NA | MGTREFCLKN_118 | AF3 |
| NA | MGTRXP1_118 | AH1 |
| NA | MGTREFCLKP_118 | AF4 |
| NA | MGTTXN1_118 | AH2 |
| NA | MGTAVTTTX_118 | AJ3 |
| NA | MGTTXP1_118 | AJ2 |
| NA | MGTTXP0_120 | B4 |
| NA | MGTAVTTTX_120 | C4 |
| NA | MGTTXN0_120 | B3 |
| NA | MGTRXP0_120 | A3 |
| NA | MGTAVTTRX_120 | C3 |
| NA | MGTRXN0_120 | A2 |
| NA | MGTAVCCPLL_120 | D3 |
| NA | MGTRXN1_120 | C1 |
| NA | MGTREFCLKN_120 | D4 |
| NA | MGTRXP1_120 | D1 |
| NA | MGTREFCLKP_120 | E4 |
| NA | MGTTXN1_120 | D2 |
| NA | MGTAVTTTX_120 | E3 |
| NA | MGTTXP1_120 | E2 |
| NA | MGTTXP0_122 | AK2 |
| NA | MGTAVTTTX_122 | AK3 |
| NA | MGTTXN0_122 | AL2 |
| NA | MGTRXP0_122 | AL1 |
| NA | MGTAVTTRX_122 | AL3 |
| NA | MGTRXN0_122 | AM1 |
| NA | MGTAVCCPLL_122 | AM4 |
| NA | MGTRXN1_122 | AP2 |
| NA | MGTREFCLKN_122 | AL4 |
| NA | MGTRXP1_122 | AP3 |
| NA | MGTREFCLKP_122 | AL5 |
| NA | MGTTXN1_122 | AN3 |
| NA | MGTAVTTTX_122 | AM3 |
| NA | MGTTXP1_122 | AN4 |
| NA | MGTTXP0_124 | B10 |
| NA | MGTAVTTTX_124 | C10 |
| NA | MGTTXN0_124 | B9 |
| NA | MGTRXP0_124 | A9 |
| NA | MGTAVTTRX_124 | C9 |
| NA | MGTRXN0_124 | A8 |

| | | |
|---|---|---|
| NA | MGTAVCCPLL_124 | C6 |
| NA | MGTRXN1_124 | A7 |
| NA | MGTREFCLKN_124 | C8 |
| NA | MGTRXP1_124 | A6 |
| NA | MGTREFCLKP_124 | D8 |
| NA | MGTTXN1_124 | B6 |
| NA | MGTAVTTTX_124 | C5 |
| NA | MGTTXP1_124 | B5 |
| NA | MGTTXP0_126 | AN5 |
| NA | MGTAVTTTX_126 | AM10 |
| NA | MGTTXN0_126 | AN6 |
| NA | MGTRXP0_126 | AP6 |
| NA | MGTAVTTRX_126 | AM6 |
| NA | MGTRXN0_126 | AP7 |
| NA | MGTAVCCPLL_126 | AM9 |
| NA | MGTRXN1_126 | AP8 |
| NA | MGTREFCLKN_126 | AM7 |
| NA | MGTRXP1_126 | AP9 |
| NA | MGTREFCLKP_126 | AL7 |
| NA | MGTTXN1_126 | AN9 |
| NA | MGTAVTTTX_126 | AM5 |
| NA | MGTTXP1_126 | AN10 |
| NA | GND | B1 |
| NA | GND | AN1 |
| NA | GND | B2 |
| NA | GND | C2 |
| NA | GND | H2 |
| NA | GND | J2 |
| NA | GND | P2 |
| NA | GND | R2 |
| NA | GND | Y2 |
| NA | GND | AA2 |
| NA | GND | AF2 |
| NA | GND | AG2 |
| NA | GND | AM2 |
| NA | GND | AN2 |
| NA | GND | G4 |
| NA | GND | K4 |
| NA | GND | M4 |
| NA | GND | N4 |
| NA | GND | T4 |
| NA | GND | W4 |

| | | |
|---|---|---|
| NA | GND | AB4 |
| NA | GND | AE4 |
| NA | GND | AH4 |
| NA | GND | AK4 |
| NA | GND | E5 |
| NA | GND | K5 |
| NA | GND | R5 |
| NA | GND | T5 |
| NA | GND | W5 |
| NA | GND | Y5 |
| NA | GND | AE5 |
| NA | GND | AJ5 |
| NA | GND | D6 |
| NA | GND | H6 |
| NA | GND | U6 |
| NA | GND | V6 |
| NA | GND | AH6 |
| NA | GND | AL6 |
| NA | GND | B7 |
| NA | GND | F7 |
| NA | GND | L7 |
| NA | GND | AA7 |
| NA | GND | AN7 |
| NA | GND | B8 |
| NA | GND | P8 |
| NA | GND | AD8 |
| NA | GND | AN8 |
| NA | GND | D9 |
| NA | GND | G9 |
| NA | GND | U9 |
| NA | GND | AG9 |
| NA | GND | AL9 |
| NA | GND | K10 |
| NA | GND | R10 |
| NA | GND | Y10 |
| NA | GND | AE10 |
| NA | GND | AK10 |
| NA | GND | A11 |
| NA | GND | B11 |
| NA | GND | C11 |
| NA | GND | N11 |
| NA | GND | U11 |

| | | |
|---|---|---|
| NA | GND | AA11 |
| NA | GND | AC11 |
| NA | GND | AN11 |
| NA | GND | AP11 |
| NA | GND | A12 |
| NA | GND | F12 |
| NA | GND | M12 |
| NA | GND | P12 |
| NA | GND | T12 |
| NA | GND | V12 |
| NA | GND | Y12 |
| NA | GND | AB12 |
| NA | GND | AD12 |
| NA | GND | AF12 |
| NA | GND | J13 |
| NA | GND | L13 |
| NA | GND | N13 |
| NA | GND | R13 |
| NA | GND | U13 |
| NA | GND | W13 |
| NA | GND | AA13 |
| NA | GND | AC13 |
| NA | GND | AJ13 |
| NA | GND | AP13 |
| NA | GND | B14 |
| NA | GND | M14 |
| NA | GND | P14 |
| NA | GND | T14 |
| NA | GND | V14 |
| NA | GND | Y14 |
| NA | GND | AB14 |
| NA | GND | AM14 |
| NA | GND | E15 |
| NA | GND | K15 |
| NA | GND | R15 |
| NA | GND | U15 |
| NA | GND | W15 |
| NA | GND | AA15 |
| NA | GND | AE15 |
| NA | GND | H16 |
| NA | GND | M16 |
| NA | GND | P16 |

| | | |
|---|---|---|
| NA | GND | T16 |
| NA | GND | V16 |
| NA | GND | Y16 |
| NA | GND | AB16 |
| NA | GND | AD16 |
| NA | GND | AH16 |
| NA | GND | A17 |
| NA | GND | L17 |
| NA | GND | N17 |
| NA | GND | R17 |
| NA | GND | AA17 |
| NA | GND | AC17 |
| NA | GND | AF17 |
| NA | GND | AL17 |
| NA | GND | D18 |
| NA | GND | J18 |
| NA | GND | M18 |
| NA | GND | P18 |
| NA | GND | Y18 |
| NA | GND | AB18 |
| NA | GND | AD18 |
| NA | GND | AP18 |
| NA | GND | G19 |
| NA | GND | N19 |
| NA | GND | R19 |
| NA | GND | U19 |
| NA | GND | W19 |
| NA | GND | AA19 |
| NA | GND | AC19 |
| NA | GND | AG19 |
| NA | GND | K20 |
| NA | GND | M20 |
| NA | GND | P20 |
| NA | GND | T20 |
| NA | GND | V20 |
| NA | GND | Y20 |
| NA | GND | AB20 |
| NA | GND | AE20 |
| NA | GND | AK20 |
| NA | GND | C21 |
| NA | GND | H21 |
| NA | GND | N21 |

| | | |
|---|---|---|
| NA | GND | R21 |
| NA | GND | U21 |
| NA | GND | W21 |
| NA | GND | AA21 |
| NA | GND | AC21 |
| NA | GND | AN21 |
| NA | GND | A22 |
| NA | GND | F22 |
| NA | GND | L22 |
| NA | GND | P22 |
| NA | GND | T22 |
| NA | GND | V22 |
| NA | GND | Y22 |
| NA | GND | AB22 |
| NA | GND | AF22 |
| NA | GND | J23 |
| NA | GND | R23 |
| NA | GND | U23 |
| NA | GND | W23 |
| NA | GND | AA23 |
| NA | GND | AJ23 |
| NA | GND | AP23 |
| NA | GND | B24 |
| NA | GND | M24 |
| NA | GND | AB24 |
| NA | GND | AG24 |
| NA | GND | AM24 |
| NA | GND | E25 |
| NA | GND | K25 |
| NA | GND | R25 |
| NA | GND | Y25 |
| NA | GND | AE25 |
| NA | GND | H26 |
| NA | GND | N26 |
| NA | GND | V26 |
| NA | GND | AC26 |
| NA | GND | AH26 |
| NA | GND | A27 |
| NA | GND | L27 |
| NA | GND | AA27 |
| NA | GND | AF27 |
| NA | GND | AL27 |

| | | |
|---|---|---|
| NA | GND | D28 |
| NA | GND | P28 |
| NA | GND | AD28 |
| NA | GND | AP28 |
| NA | GND | B29 |
| NA | GND | G29 |
| NA | GND | U29 |
| NA | GND | AG29 |
| NA | GND | K30 |
| NA | GND | Y30 |
| NA | GND | AK30 |
| NA | GND | C31 |
| NA | GND | N31 |
| NA | GND | AC31 |
| NA | GND | AN31 |
| NA | GND | A32 |
| NA | GND | F32 |
| NA | GND | T32 |
| NA | GND | AF32 |
| NA | GND | D33 |
| NA | GND | J33 |
| NA | GND | W33 |
| NA | GND | AJ33 |
| NA | GND | AP33 |
| NA | GND | B34 |
| NA | GND | G34 |
| NA | GND | M34 |
| NA | GND | U34 |
| NA | GND | AB34 |
| NA | GND | AG34 |
| NA | GND | AM34 |
| NA | VCCAUX | M11 |
| NA | VCCAUX | P11 |
| NA | VCCAUX | V11 |
| NA | VCCAUX | AB11 |
| NA | VCCAUX | L12 |
| NA | VCCAUX | AC12 |
| NA | VCCAUX | M21 |
| NA | VCCAUX | P23 |
| NA | VCCAUX | T23 |
| NA | VCCAUX | V23 |
| NA | VCCAUX | Y23 |

| | | |
|---|---|---|
| NA | VCCAUX | U24 |
| NA | VCCINT | N12 |
| NA | VCCINT | R12 |
| NA | VCCINT | U12 |
| NA | VCCINT | W12 |
| NA | VCCINT | AA12 |
| NA | VCCINT | M13 |
| NA | VCCINT | P13 |
| NA | VCCINT | T13 |
| NA | VCCINT | V13 |
| NA | VCCINT | Y13 |
| NA | VCCINT | AB13 |
| NA | VCCINT | AD13 |
| NA | VCCINT | R14 |
| NA | VCCINT | U14 |
| NA | VCCINT | W14 |
| NA | VCCINT | AA14 |
| NA | VCCINT | T15 |
| NA | VCCINT | V15 |
| NA | VCCINT | Y15 |
| NA | VCCINT | N16 |
| NA | VCCINT | R16 |
| NA | VCCINT | U16 |
| NA | VCCINT | W16 |
| NA | VCCINT | AA16 |
| NA | VCCINT | AC16 |
| NA | VCCINT | M17 |
| NA | VCCINT | P17 |
| NA | VCCINT | Y17 |
| NA | VCCINT | AB17 |
| NA | VCCINT | AD17 |
| NA | VCCINT | N18 |
| NA | VCCINT | R18 |
| NA | VCCINT | AA18 |
| NA | VCCINT | AC18 |
| NA | VCCINT | M19 |
| NA | VCCINT | P19 |
| NA | VCCINT | T19 |
| NA | VCCINT | V19 |
| NA | VCCINT | Y19 |
| NA | VCCINT | AB19 |
| NA | VCCINT | N20 |

| | | |
|---|---|---|
| NA | VCCINT | R20 |
| NA | VCCINT | U20 |
| NA | VCCINT | W20 |
| NA | VCCINT | AA20 |
| NA | VCCINT | AC20 |
| NA | VCCINT | P21 |
| NA | VCCINT | T21 |
| NA | VCCINT | V21 |
| NA | VCCINT | Y21 |
| NA | VCCINT | AB21 |
| NA | VCCINT | R22 |
| NA | VCCINT | U22 |
| NA | VCCINT | W22 |
| 0 | VCCO_0 | AA22 |
| 0 | VCCO_0 | AD23 |
| 1 | VCCO_1 | D13 |
| 1 | VCCO_1 | G14 |
| 2 | VCCO_2 | AM19 |
| 2 | VCCO_2 | AH21 |
| 3 | VCCO_3 | E20 |
| 3 | VCCO_3 | D23 |
| 4 | VCCO_4 | AL12 |
| 4 | VCCO_4 | AG14 |
| 5 | VCCO_5 | C16 |
| 5 | VCCO_5 | F17 |
| 5 | VCCO_5 | B19 |
| 6 | VCCO_6 | AK15 |
| 6 | VCCO_6 | AN16 |
| 6 | VCCO_6 | AJ18 |
| 11 | VCCO_11 | T27 |
| 11 | VCCO_11 | R30 |
| 11 | VCCO_11 | V31 |
| 12 | VCCO_12 | N6 |
| 12 | VCCO_12 | T7 |
| 12 | VCCO_12 | M9 |
| 13 | VCCO_13 | W28 |
| 13 | VCCO_13 | AB29 |
| 13 | VCCO_13 | AA32 |
| 15 | VCCO_15 | M29 |
| 15 | VCCO_15 | L32 |
| 15 | VCCO_15 | P33 |
| 17 | VCCO_17 | AE30 |

| | | |
|---|---|---|
| 17 | VCCO_17 | AH31 |
| 17 | VCCO_17 | AD33 |
| 18 | VCCO_18 | AC6 |
| 18 | VCCO_18 | W8 |
| 18 | VCCO_18 | AB9 |
| 19 | VCCO_19 | J28 |
| 19 | VCCO_19 | E30 |
| 19 | VCCO_19 | H31 |
| 20 | VCCO_20 | J8 |
| 20 | VCCO_20 | E10 |
| 20 | VCCO_20 | H11 |
| 21 | VCCO_21 | AJ28 |
| 21 | VCCO_21 | AM29 |
| 21 | VCCO_21 | AL32 |
| 22 | VCCO_22 | AF7 |
| 22 | VCCO_22 | AJ8 |
| 22 | VCCO_22 | AH11 |
| 23 | VCCO_23 | G24 |
| 23 | VCCO_23 | C26 |
| 23 | VCCO_23 | F27 |
| 25 | VCCO_25 | AL22 |
| 25 | VCCO_25 | AK25 |
| 25 | VCCO_25 | AN26 |
| NA | MGTAVCC_112 | R3 |
| NA | MGTAVCC_112 | R4 |
| NA | MGTAVCC_114 | AA3 |
| NA | MGTAVCC_114 | AA4 |
| NA | MGTAVCC_116 | J3 |
| NA | MGTAVCC_116 | J4 |
| NA | MGTAVCC_118 | AG3 |
| NA | MGTAVCC_118 | AG4 |
| NA | MGTAVCC_120 | D5 |
| NA | MGTAVCC_120 | F4 |
| NA | MGTAVCC_122 | AJ4 |
| NA | MGTAVCC_122 | AK5 |
| NA | MGTAVCC_124 | C7 |
| NA | MGTAVCC_124 | D7 |
| NA | MGTAVCC_126 | AL8 |
| NA | MGTAVCC_126 | AM8 |
| NA | FLOAT | U4 |

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.

2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

As shown in Table 26, the BQ5VSX240T device is available in the CCGA1738 packages.

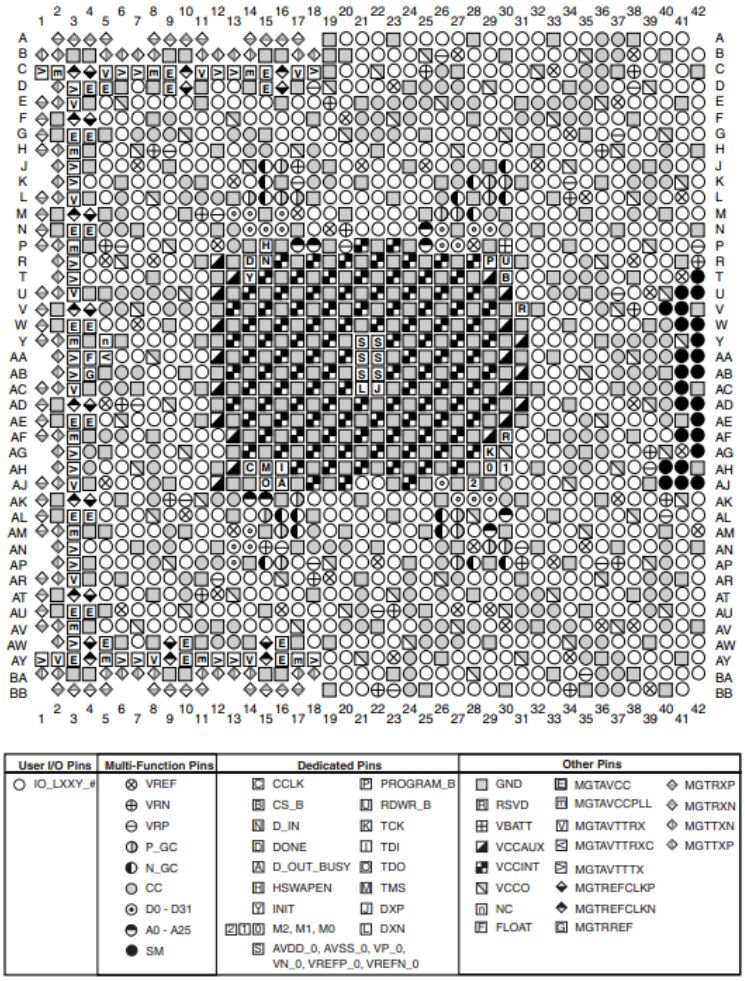



Table 26 BQ5VSX240T packages

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 0 | DXP_0 | AC22 | 20 | IO_L16N_20 | K9 | NA | GND | F2 |
| 0 | DXN_0 | AC21 | 20 | IO_L17P_20 | K7 | NA | GND | G2 |
| 0 | AVDD_0 | Y22 | 20 | IO_L17N_20 | L7 | NA | GND | M2 |
| 0 | AVSS_0 | Y21 | 20 | IO_L18P_20 | M7 | NA | GND | N2 |
| 0 | VP_0 | AA22 | 20 | IO_L18N_20 | M8 | NA | GND | V2 |
| 0 | VN_0 | AB21 | 20 | IO_L19P_20 | M9 | NA | GND | W2 |
| 0 | VREFP_0 | AB22 | 20 | IO_L19N_20 | L9 | NA | GND | AD2 |
| 0 | VREFN_0 | AA21 | 21 | IO_L0P_21 | AB33 | NA | GND | AE2 |
| 0 | VBATT_0 | P30 | 21 | IO_L0N_21 | AB32 | NA | GND | AK2 |
| 0 | PROGRAM_B_ | R29 | 21 | IO_L1P_21 | AC33 | NA | GND | AL2 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| | 0 | | | | | | | |
| 0 | HSWAPEN_0 | P15 | 21 | IO_L1N_21 | AD32 | NA | GND | AT2 |
| 0 | D_IN_0 | R15 | 21 | IO_L2P_21 | AD33 | NA | GND | AU2 |
| 0 | DONE_0 | R14 | 21 | IO_L2N_21 | AE32 | NA | GND | B3 |
| 0 | CCLK_0 | AH14 | 21 | IO_L3P_21 | AE33 | NA | GND | BA3 |
| 0 | INIT_B_0 | T14 | 21 | IO_L3N_21 | AE34 | NA | GND | B4 |
| 0 | CS_B_0 | T30 | 21 | IO_L4P_21 | AV 3 9 | NA | GND | E4 |
| 0 | RDWR_B_0 | R30 | 21 | IO_L4N_VREF_21 | AV 3 8 | NA | GND | H4 |
| 0 | RSVD(3) | V31 | 21 | IO_L5P_21 | AU38 | NA | GND | J4 |
| 0 | RSVD(3) | AF30 | 21 | IO_L5N_21 | AU37 | NA | GND | L4 |
| 0 | TCK_0 | AG29 | 21 | IO_L6P_21 | AT37 | NA | GND | P4 |
| 0 | M0_0 | AH29 | 21 | IO_L6N_21 | AR38 | NA | GND | U4 |
| 0 | M2_0 | AJ28 | 21 | IO_L7P_21 | AR37 | NA | GND | Y4 |
| 0 | M1_0 | AH30 | 21 | IO_L7N_21 | AT36 | NA | GND | AC4 |
| 0 | TMS_0 | AH15 | 21 | IO_L8P_CC_21 | AE35 | NA | GND | AF4 |
| 0 | TDI_0 | AH16 | 21 | IO_L8N_CC_21 | AF34 | NA | GND | AJ4 |
| 0 | D_OUT_BUSY_0 | AJ16 | 21 | IO_L9P_CC_21 | AF35 | NA | GND | AM4 |
| 0 | TDO_0 | AJ15 | 21 | IO_L9N_CC_21 | AF36 | NA | GND | AP4 |
| 1 | IO_L0P_A19_1 | N25 | 21 | IO_L10P_CC_21 | AH34 | NA | GND | AR4 |
| 1 | IO_L0N_A18_1 | P25 | 21 | IO_L10N_CC_21 | AG34 | NA | GND | AV 4 |
| 1 | IO_L1P_A17_1 | P18 | 21 | IO_L11P_CC_21 | AH35 | NA | GND | BA4 |
| 1 | IO_L1N_A16_1 | P17 | 21 | IO_L11N_CC_21 | AG36 | NA | GND | G5 |
| 1 | IO_L2P_A15_D31_1 | P26 | 21 | IO_L12P_VRN_21 | AP37 | NA | GND | M5 |
| 1 | IO_L2N_A14_D30_1 | N26 | 21 | IO_L12N_VRP_21 | AP36 | NA | GND | U5 |
| 1 | IO_L3P_A13_D29_1 | M16 | 21 | IO_L13P_21 | AP35 | NA | GND | AB5 |
| 1 | IO_L3N_A12_D28_1 | N16 | 21 | IO_L13N_21 | AN36 | NA | GND | AG5 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 1 | IO_L4P_A11_D27_1 | P27 | 21 | IO_L14P_21 | AM36 | NA | GND | AM5 |
| 1 | IO_L4N_VREF_A10_D26_1 | P28 | 21 | IO_L14N_VREF_21 | AN35 | NA | GND | AU5 |
| 1 | IO_L5P_A9_D25_1 | N15 | 21 | IO_L15P_21 | AN34 | NA | GND | D6 |
| 1 | IO_L5N_A8_D24_1 | N14 | 21 | IO_L15N_21 | AM34 | NA | GND | K6 |
| 1 | IO_L6P_A7_D23_1 | N28 | 21 | IO_L16P_21 | AH36 | NA | GND | Y6 |
| 1 | IO_L6N_A6_D22_1 | N29 | 21 | IO_L16N_21 | AJ36 | NA | GND | AK6 |
| 1 | IO_L7P_A5_D21_1 | M14 | 21 | IO_L17P_21 | AJ35 | NA | GND | AR6 |
| 1 | IO_L7N_A4_D20_1 | M13 | 21 | IO_L17N_21 | AK35 | NA | GND | AW6 |
| 1 | IO_L8P_CC_A3_D19_1 | N30 | 21 | IO_L18P_21 | AL36 | NA | GND | N7 |
| 1 | IO_L8N_CC_A2_D18_1 | M29 | 21 | IO_L18N_21 | AL35 | NA | GND | AC7 |
| 1 | IO_L9P_CC_A1_D17_1 | N13 | 21 | IO_L19P_21 | AL34 | NA | GND | AN7 |
| 1 | IO_L9N_CC_A0_D16_1 | P13 | 21 | IO_L19N_21 | AK34 | NA | GND | D8 |
| 2 | IO_L0P_CC_RS1_2 | AK12 | 23 | IO_L0P_23 | N33 | NA | GND | F8 |
| 2 | IO_L0N_CC_RS0_2 | AK13 | 23 | IO_L0N_23 | N34 | NA | GND | T8 |
| 2 | IO_L1P_CC_A25_2 | AJ30 | 23 | IO_L1P_23 | M34 | NA | GND | AF8 |
| 2 | IO_L1N_CC_A24_2 | AK30 | 23 | IO_L1N_23 | M33 | NA | GND | AT8 |
| 2 | IO_L2P_A23_2 | AK15 | 23 | IO_L2P_23 | M32 | NA | GND | AW8 |
| 2 | IO_L2N_A22_2 | AK14 | 23 | IO_L2N_23 | M31 | NA | GND | B9 |
| 2 | IO_L3P_A21_2 | AL30 | 23 | IO_L3P_23 | N31 | NA | GND | J9 |
| 2 | IO_L3N_A20 | AM29 | 23 | IO_L3N_23 | P31 | NA | GND | W9 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| | _2 | | | | | | | |
| 2 | IO_L4P_FCS_B_2 | AL14 | 23 | IO_L4P_23 | H34 | NA | GND | AJ9 |
| 2 | IO_L4N_VREF_FOE_B_MOSI_2 | AM13 | 23 | IO_L4N_VREF_23 | G34 | NA | GND | BA9 |
| 2 | IO_L5P_FWE_B_2 | AM28 | 23 | IO_L5P_23 | G33 | NA | GND | B10 |
| 2 | IO_L5N_CSO_B_2 | AL29 | 23 | IO_L5N_23 | H33 | NA | GND | M10 |
| 2 | IO_L6P_D7_2 | AN13 | 23 | IO_L6P_23 | G32 | NA | GND | AB10 |
| 2 | IO_L6N_D6_2 | AP13 | 23 | IO_L6N_23 | G31 | NA | GND | AM10 |
| 2 | IO_L7P_D5_2 | AK28 | 23 | IO_L7P_23 | H31 | NA | GND | BA10 |
| 2 | IO_L7N_D4_2 | AK29 | 23 | IO_L7N_23 | J31 | NA | GND | D11 |
| 2 | IO_L8P_D3_2 | AN14 | 23 | IO_L8P_CC_23 | F35 | NA | GND | E11 |
| 2 | IO_L8N_D2_FS2_2 | AM14 | 23 | IO_L8N_CC_23 | E35 | NA | GND | K11 |
| 2 | IO_L9P_D1_FS1_2 | AK27 | 23 | IO_L9P_CC_23 | E34 | NA | GND | R11 |
| 2 | IO_L9N_D0_FS0_2 | AJ26 | 23 | IO_L9N_CC_23 | F34 | NA | GND | Y11 |
| 3 | IO_L0P_CC_GC_3 | J16 | 23 | IO_L10P_CC_23 | F31 | NA | GND | AC11 |
| 3 | IO_L0N_CC_GC_3 | J15 | 23 | IO_L10N_CC_23 | F32 | NA | GND | AE11 |
| 3 | IO_L1P_CC_GC_3 | M26 | 23 | IO_L11P_CC_23 | E32 | NA | GND | AR11 |
| 3 | IO_L1N_CC_GC_3 | L27 | 23 | IO_L11N_CC_23 | E33 | NA | GND | AW11 |
| 3 | IO_L2P_GC_VRN_3 | J17 | 23 | IO_L12P_VRN_23 | L34 | NA | GND | H12 |
| 3 | IO_L2N_GC_VRP_3 | K17 | 23 | IO_L12N_VRP_23 | K34 | NA | GND | N12 |
| 3 | IO_L3P_GC_3 | M27 | 23 | IO_L13P_23 | K33 | NA | GND | T12 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 3 | IO_L3N_GC_3 | M28 | 23 | IO_L13N_23 | J33 | NA | GND | V12 |
| 3 | IO_L4P_GC_3 | L17 | 23 | IO_L14P_23 | K32 | NA | GND | Y12 |
| 3 | IO_L4N_GC_VREF_3 | M17 | 23 | IO_L14N_VREF_23 | J32 | NA | GND | AB12 |
| 3 | IO_L5P_GC_3 | L29 | 23 | IO_L15P_23 | L32 | NA | GND | AD12 |
| 3 | IO_L5N_GC_3 | K28 | 23 | IO_L15N_23 | L31 | NA | GND | AH12 |
| 3 | IO_L6P_GC_3 | L16 | 23 | IO_L16P_23 | P33 | NA | GND | AN12 |
| 3 | IO_L6N_GC_3 | L15 | 23 | IO_L16N_23 | P32 | NA | GND | AV12 |
| 3 | IO_L7P_GC_3 | K29 | 23 | IO_L17P_23 | R33 | NA | GND | L13 |
| 3 | IO_L7N_GC_3 | J30 | 23 | IO_L17N_23 | R32 | NA | GND | R13 |
| 3 | IO_L8P_GC_3 | L14 | 23 | IO_L18P_23 | T32 | NA | GND | U13 |
| 3 | IO_L8N_GC_3 | K15 | 23 | IO_L18N_23 | U32 | NA | GND | W13 |
| 3 | IO_L9P_GC_3 | K30 | 23 | IO_L19P_23 | U31 | NA | GND | AA13 |
| 3 | IO_L9N_GC_3 | L30 | 23 | IO_L19N_23 | T31 | NA | GND | AC13 |
| 4 | IO_L0P_GC_D15_4 | AN30 | 24 | IO_L0P_24 | J12 | NA | GND | AE13 |
| 4 | IO_L0N_GC_D14_4 | AP30 | 24 | IO_L0N_24 | H11 | NA | GND | AG13 |
| 4 | IO_L1P_GC_D13_4 | AK17 | 24 | IO_L1P_24 | G12 | NA | GND | AJ13 |
| 4 | IO_L1N_GC_D12_4 | AL17 | 24 | IO_L1N_24 | G11 | NA | GND | AL13 |
| 4 | IO_L2P_GC_D11_4 | AN29 | 24 | IO_L2P_24 | F12 | NA | GND | D14 |
| 4 | IO_L2N_GC_D10_4 | AP28 | 24 | IO_L2N_24 | F11 | NA | GND | P14 |
| 4 | IO_L3P_GC_D9_4 | AL15 | 24 | IO_L3P_24 | E10 | NA | GND | V14 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 4 | IO_L3N_GC_D8_4 | AL16 | 24 | IO_L3N_24 | F10 | NA | GND | Y14 |
| 4 | IO_L4P_GC_4 | AP27 | 24 | IO_L4P_24 | K14 | NA | GND | AB14 |
| 4 | IO_L4N_GC_VREF_4 | AN28 | 24 | IO_L4N_VREF_24 | K13 | NA | GND | AD14 |
| 4 | IO_L5P_GC_4 | AM16 | 24 | IO_L5P_24 | K12 | NA | GND | AF14 |
| 4 | IO_L5N_GC_4 | AM17 | 24 | IO_L5N_24 | J11 | NA | GND | AJ14 |
| 4 | IO_L6P_GC_4 | AM27 | 24 | IO_L6P_24 | J13 | NA | GND | AP14 |
| 4 | IO_L6N_GC_4 | AM26 | 24 | IO_L6N_24 | H13 | NA | GND | AW14 |
| 4 | IO_L7P_GC_VRN_4 | AN15 | 24 | IO_L7P_24 | H10 | NA | GND | B15 |
| 4 | IO_L7N_GC_VRP_4 | AN16 | 24 | IO_L7N_24 | J10 | NA | GND | G15 |
| 4 | IO_L8P_CC_GC_4 | AL27 | 24 | IO_L8P_CC_24 | H14 | NA | GND | M15 |
| 4 | IO_L8N_CC_GC_4 | AL26 | 24 | IO_L8N_CC_24 | H15 | NA | GND | U15 |
| 4 | IO_L9P_CC_GC_4 | AP16 | 24 | IO_L9P_CC_24 | K10 | NA | GND | W15 |
| 4 | IO_L9N_CC_GC_4 | AP15 | 24 | IO_L9N_CC_24 | L10 | NA | GND | AA15 |
| 5 | IO_L0P_5 | L24 | 24 | IO_L10P_CC_24 | L12 | NA | GND | AC15 |
| 5 | IO_L0N_5 | M24 | 24 | IO_L10N_CC_24 | L11 | NA | GND | AE15 |
| 5 | IO_L1P_5 | E18 | 24 | IO_L11P_CC_24 | G13 | NA | GND | AG15 |
| 5 | IO_L1N_5 | E17 | 24 | IO_L11N_CC_24 | G14 | NA | GND | AM15 |
| 5 | IO_L2P_5 | K24 | 24 | IO_L12P_VRN_24 | M11 | NA | GND | AU15 |
| 5 | IO_L2N_5 | L25 | 24 | IO_L12N_VRP_24 | M12 | NA | GND | BA15 |
| 5 | IO_L3P_5 | F16 | 24 | IO_L13P_24 | F14 | NA | GND | B16 |
| 5 | IO_L3N_5 | F17 | 24 | IO_L13N_24 | E13 | NA | GND | E16 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 5 | IO_L4P_5 | K25 | 24 | IO_L14P_24 | N11 | NA | GND | K16 |
| 5 | IO_L4N_VREF_5 | J25 | 24 | IO_L14N_VREF_24 | P12 | NA | GND | P16 |
| 5 | IO_L5P_5 | G16 | 24 | IO_L15P_24 | E12 | NA | GND | T16 |
| 5 | IO_L5N_5 | H16 | 24 | IO_L15N_24 | D12 | NA | GND | V16 |
| 5 | IO_L6P_5 | H26 | 24 | IO_L16P_24 | P11 | NA | GND | Y16 |
| 5 | IO_L6N_5 | J26 | 24 | IO_L16N_24 | N10 | NA | GND | AB16 |
| 5 | IO_L7P_5 | G18 | 24 | IO_L17P_24 | D13 | NA | GND | AD16 |
| 5 | IO_L7N_5 | G17 | 24 | IO_L17N_24 | E14 | NA | GND | AF16 |
| 5 | IO_L8P_CC_5 | J28 | 24 | IO_L18P_24 | R10 | NA | GND | AK16 |
| 5 | IO_L8N_CC_5 | J27 | 24 | IO_L18N_24 | P10 | NA | GND | BA16 |
| 5 | IO_L9P_CC_5 | J18 | 24 | IO_L19P_24 | E15 | NA | GND | D17 |
| 5 | IO_L9N_CC_5 | H18 | 24 | IO_L19N_24 | F15 | NA | GND | N17 |
| 5 | IO_L10P_CC_5 | K18 | 25 | IO_L0P_25 | AG31 | NA | GND | R17 |
| 5 | IO_L10N_CC_5 | K19 | 25 | IO_L0N_25 | AF31 | NA | GND | U17 |
| 5 | IO_L11P_CC_5 | K27 | 25 | IO_L1P_25 | AF32 | NA | GND | W17 |
| 5 | IO_L11N_CC_5 | L26 | 25 | IO_L1N_25 | AG33 | NA | GND | AA17 |
| 5 | IO_L12P_VRN_5 | N20 | 25 | IO_L2P_25 | AH33 | NA | GND | AC17 |
| 5 | IO_L12N_VRP_5 | P20 | 25 | IO_L2N_25 | AG32 | NA | GND | AE17 |
| 5 | IO_L13P_5 | G27 | 25 | IO_L3P_25 | AH31 | NA | GND | AG17 |
| 5 | IO_L13N_5 | F27 | 25 | IO_L3N_25 | AJ31 | NA | GND | AJ17 |
| 5 | IO_L14P_5 | M19 | 25 | IO_L4P_25 | AV 3 5 | NA | GND | AN17 |
| 5 | IO_L14N_VREF_5 | N19 | 25 | IO_L4N_VREF_25 | AV 3 6 | NA | GND | AW17 |
| 5 | IO_L15P_5 | G28 | 25 | IO_L5P_25 | AU36 | NA | GND | F18 |
| 5 | IO_L15N_5 | H28 | 25 | IO_L5N_25 | AT35 | NA | GND | L18 |
| 5 | IO_L16P_5 | M18 | 25 | IO_L6P_25 | AU34 | NA | GND | T18 |
| 5 | IO_L16N_5 | N18 | 25 | IO_L6N_25 | AT34 | NA | GND | V18 |
| 5 | IO_L17P_5 | G29 | 25 | IO_L7P_25 | AR35 | NA | GND | Y18 |
| 5 | IO_L17N_5 | F29 | 25 | IO_L7N_25 | AR34 | NA | GND | AB18 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 5 | IO_L18P_5 | L20 | 25 | IO_L8P_CC_25 | AU32 | NA | GND | AD18 |
| 5 | IO_L18N_5 | L19 | 25 | IO_L8N_CC_25 | AU33 | NA | GND | AF18 |
| 5 | IO_L19P_5 | H29 | 25 | IO_L9P_CC_25 | AV 3 3 | NA | GND | AH18 |
| 5 | IO_L19N_5 | H30 | 25 | IO_L9N_CC_25 | AV 3 4 | NA | GND | AL18 |
| 6 | IO_L0P_6 | AR29 | 25 | IO_L10P_CC_25 | AV 3 1 | NA | GND | AT18 |
| 6 | IO_L0N_6 | AR28 | 25 | IO_L10N_CC_25 | AU31 | NA | GND | A19 |
| 6 | IO_L1P_6 | AT14 | 25 | IO_L11P_CC_25 | AT32 | NA | GND | B19 |
| 6 | IO_L1N_6 | AR14 | 25 | IO_L11N_CC_25 | AT31 | NA | GND | C19 |
| 6 | IO_L2P_6 | AR30 | 25 | IO_L12P_VRN_25 | AP31 | NA | GND | J19 |
| 6 | IO_L2N_6 | AT30 | 25 | IO_L12N_VRP_25 | AN31 | NA | GND | P19 |
| 6 | IO_L3P_6 | AT15 | 25 | IO_L13P_25 | AR32 | NA | GND | R19 |
| 6 | IO_L3N_6 | AR15 | 25 | IO_L13N_25 | AP32 | NA | GND | U19 |
| 6 | IO_L4P_6 | AT29 | 25 | IO_L14P_25 | AR33 | NA | GND | W19 |
| 6 | IO_L4N_VREF_6 | AU29 | 25 | IO_L14N_VREF_25 | AP33 | NA | GND | AA19 |
| 6 | IO_L5P_6 | AT17 | 25 | IO_L15P_25 | AN33 | NA | GND | AC19 |
| 6 | IO_L5N_6 | AT16 | 25 | IO_L15N_25 | AM33 | NA | GND | AE19 |
| 6 | IO_L6P_6 | AU28 | 25 | IO_L16P_25 | AK33 | NA | GND | AG19 |
| 6 | IO_L6N_6 | AT27 | 25 | IO_L16N_25 | AJ33 | NA | GND | AJ19 |
| 6 | IO_L7P_6 | AP17 | 25 | IO_L17P_25 | AJ32 | NA | GND | AW19 |
| 6 | IO_L7N_6 | AR17 | 25 | IO_L17N_25 | AK32 | NA | GND | BB19 |
| 6 | IO_L8P_CC_6 | AT26 | 25 | IO_L18P_25 | AL32 | NA | GND | B20 |
| 6 | IO_L8N_CC_6 | AR27 | 25 | IO_L18N_25 | AM32 | NA | GND | M20 |
| 6 | IO_L9P_CC_6 | AN20 | 25 | IO_L19P_25 | AL31 | NA | GND | T20 |
| 6 | IO_L9N_CC_6 | AN19 | 25 | IO_L19N_25 | AM31 | NA | GND | V20 |
| 6 | IO_L10P_CC | AN18 | 26 | IO_L0P_26 | AT7 | NA | GND | Y20 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| | _6 | | | | | | | |
| 6 | IO_L10N_CC_6 | AM18 | 26 | IO_L0N_26 | AR7 | NA | GND | AB20 |
| 6 | IO_L11P_CC_6 | AN26 | 26 | IO_L1P_26 | AG12 | NA | GND | AD20 |
| 6 | IO_L11N_CC_6 | AP26 | 26 | IO_L1N_26 | AG11 | NA | GND | AF20 |
| 6 | IO_L12P_VRN_6 | AR18 | 26 | IO_L2P_26 | AT6 | NA | GND | AH20 |
| 6 | IO_L12N_VRP_6 | AP18 | 26 | IO_L2N_26 | AR5 | NA | GND | AM20 |
| 6 | IO_L13P_6 | AN25 | 26 | IO_L3P_26 | AG9 | NA | GND | E21 |
| 6 | IO_L13N_6 | AP25 | 26 | IO_L3N_26 | AH9 | NA | GND | K21 |
| 6 | IO_L14P_6 | AT19 | 26 | IO_L4P_26 | AT5 | NA | GND | R21 |
| 6 | IO_L14N_VREF_6 | AR19 | 26 | IO_L4N_VREF_26 | AU6 | NA | GND | U21 |
| 6 | IO_L15P_6 | AM24 | 26 | IO_L5P_26 | AH10 | NA | GND | W21 |
| 6 | IO_L15N_6 | AN24 | 26 | IO_L5N_26 | AH11 | NA | GND | AE21 |
| 6 | IO_L16P_6 | AK18 | 26 | IO_L6P_26 | AV 6 | NA | GND | AG21 |
| 6 | IO_L16N_6 | AK19 | 26 | IO_L6N_26 | AV 5 | NA | GND | AK21 |
| 6 | IO_L17P_6 | AK24 | 26 | IO_L7P_26 | AJ11 | NA | GND | AR21 |
| 6 | IO_L17N_6 | AK25 | 26 | IO_L7N_26 | AJ10 | NA | GND | H22 |
| 6 | IO_L18P_6 | AM19 | 26 | IO_L8P_CC_26 | AM9 | NA | GND | P22 |
| 6 | IO_L18N_6 | AL19 | 26 | IO_L8N_CC_26 | AN9 | NA | GND | T22 |
| 6 | IO_L19P_6 | AL25 | 26 | IO_L9P_CC_26 | AG8 | NA | GND | V22 |
| 6 | IO_L19N_6 | AL24 | 26 | IO_L9N_CC_26 | AH8 | NA | GND | AD22 |
| 7 | IO_L0P_7 | M23 | 26 | IO_L10P_CC_26 | AK8 | NA | GND | AF22 |
| 7 | IO_L0N_7 | M22 | 26 | IO_L10N_CC_26 | AJ8 | NA | GND | AH22 |
| 7 | IO_L1P_7 | M21 | 26 | IO_L11P_CC_26 | AN8 | NA | GND | AN22 |
| 7 | IO_L1N_7 | L21 | 26 | IO_L11N_CC_26 | AP8 | NA | GND | AV22 |
| 7 | IO_L2P_7 | N24 | 26 | IO_L12P_VRN_26 | AK9 | NA | GND | A23 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 7 | IO_L2N_7 | N23 | 26 | IO_L12N_VRP_26 | AK10 | NA | GND | L23 |
| 7 | IO_L3P_7 | N22 | 26 | IO_L13P_26 | AP7 | NA | GND | R23 |
| 7 | IO_L3N_7 | N21 | 26 | IO_L13N_26 | AR8 | NA | GND | U23 |
| 7 | IO_L4P_7 | H21 | 26 | IO_L14P_26 | AL9 | NA | GND | W23 |
| 7 | IO_L4N_VREF_7 | J21 | 26 | IO_L14N_VREF_26 | AL10 | NA | GND | AA23 |
| 7 | IO_L5P_7 | J20 | 26 | IO_L15P_26 | AP6 | NA | GND | AC23 |
| 7 | IO_L5N_7 | K20 | 26 | IO_L15N_26 | AP5 | NA | GND | AE23 |
| 7 | IO_L6P_7 | L22 | 26 | IO_L16P_26 | AL6 | NA | GND | AG23 |
| 7 | IO_L6N_7 | K23 | 26 | IO_L16N_26 | AL7 | NA | GND | AJ23 |
| 7 | IO_L7P_7 | K22 | 26 | IO_L17P_26 | AN4 | NA | GND | AL23 |
| 7 | IO_L7N_7 | J22 | 26 | IO_L17N_26 | AN5 | NA | GND | BA23 |
| 7 | IO_L8P_CC_7 | F22 | 26 | IO_L18P_26 | AN6 | NA | GND | D24 |
| 7 | IO_L8N_CC_7 | G22 | 26 | IO_L18N_26 | AM6 | NA | GND | J24 |
| 7 | IO_L9P_CC_7 | G21 | 26 | IO_L19P_26 | AM7 | NA | GND | P24 |
| 7 | IO_L9N_CC_7 | F21 | 26 | IO_L19N_26 | AM8 | NA | GND | T24 |
| 7 | IO_L10P_CC_7 | E22 | 27 | IO_L0P_27 | D31 | NA | GND | V24 |
| 7 | IO_L10N_CC_7 | E23 | 27 | IO_L0N_27 | C31 | NA | GND | Y24 |
| 7 | IO_L11P_CC_7 | F24 | 27 | IO_L1P_27 | C30 | NA | GND | AB24 |
| 7 | IO_L11N_CC_7 | G23 | 27 | IO_L1N_27 | B31 | NA | GND | AD24 |
| 7 | IO_L12P_VRN_7 | E19 | 27 | IO_L2P_27 | A30 | NA | GND | AF24 |
| 7 | IO_L12N_VRP_7 | D18 | 27 | IO_L2N_27 | A31 | NA | GND | AH24 |
| 7 | IO_L13P_7 | J23 | 27 | IO_L3P_27 | A32 | NA | GND | AP24 |
| 7 | IO_L13N_7 | H23 | 27 | IO_L3N_27 | B32 | NA | GND | G25 |
| 7 | IO_L14P_7 | E20 | 27 | IO_L4P_27 | B33 | NA | GND | M25 |
| 7 | IO_L14N_VREF_7 | F20 | 27 | IO_L4N_VREF_27 | C33 | NA | GND | R25 |
| 7 | IO_L15P_7 | G24 | 27 | IO_L5P_27 | D32 | NA | GND | U25 |
| 7 | IO_L15N_7 | H24 | 27 | IO_L5N_27 | D33 | NA | GND | W25 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 7 | IO_L16P_7 | F19 | 27 | IO_L6P_27 | C34 | NA | GND | AA25 |
| 7 | IO_L16N_7 | G19 | 27 | IO_L6N_27 | B34 | NA | GND | AC25 |
| 7 | IO_L17P_7 | F26 | 27 | IO_L7P_27 | A34 | NA | GND | AE25 |
| 7 | IO_L17N_7 | F25 | 27 | IO_L7N_27 | A35 | NA | GND | AG25 |
| 7 | IO_L18P_7 | H19 | 27 | IO_L8P_CC_27 | D35 | NA | GND | AJ25 |
| 7 | IO_L18N_7 | H20 | 27 | IO_L8N_CC_27 | D36 | NA | GND | AM25 |
| 7 | IO_L19P_7 | H25 | 27 | IO_L9P_CC_27 | C36 | NA | GND | AU25 |
| 7 | IO_L19N_7 | G26 | 27 | IO_L9N_CC_27 | C35 | NA | GND | BB25 |
| 8 | IO_L0P_8 | AL21 | 27 | IO_L10P_CC_27 | A37 | NA | GND | K26 |
| 8 | IO_L0N_8 | AL22 | 27 | IO_L10N_CC_27 | A36 | NA | GND | T26 |
| 8 | IO_L1P_8 | AK23 | 27 | IO_L11P_CC_27 | B37 | NA | GND | V26 |
| 8 | IO_L1N_8 | AK22 | 27 | IO_L11N_CC_27 | B36 | NA | GND | Y26 |
| 8 | IO_L2P_8 | AJ22 | 27 | IO_L12P_VRN_27 | C38 | NA | GND | AB26 |
| 8 | IO_L2N_8 | AJ21 | 27 | IO_L12N_VRP_27 | D38 | NA | GND | AD26 |
| 8 | IO_L3P_8 | AK20 | 27 | IO_L13P_27 | C39 | NA | GND | AF26 |
| 8 | IO_L3N_8 | AL20 | 27 | IO_L13N_27 | C40 | NA | GND | AH26 |
| 8 | IO_L4P_8 | AU26 | 27 | IO_L14P_27 | B39 | NA | GND | AK26 |
| 8 | IO_L4N_VREF_8 | AU27 | 27 | IO_L14N_VREF_27 | B38 | NA | GND | AY26 |
| 8 | IO_L5P_8 | AU19 | 27 | IO_L15P_27 | A39 | NA | GND | C27 |
| 8 | IO_L5N_8 | AU18 | 27 | IO_L15N_27 | A40 | NA | GND | N27 |
| 8 | IO_L6P_8 | AR25 | 27 | IO_L16P_27 | A41 | NA | GND | R27 |
| 8 | IO_L6N_8 | AT25 | 27 | IO_L16N_27 | B41 | NA | GND | U27 |
| 8 | IO_L7P_8 | AR20 | 27 | IO_L17P_27 | B42 | NA | GND | W27 |
| 8 | IO_L7N_8 | AT20 | 27 | IO_L17N_27 | C41 | NA | GND | AA27 |
| 8 | IO_L8P_CC_8 | AT24 | 27 | IO_L18P_27 | D40 | NA | GND | AC27 |
| 8 | IO_L8N_CC_8 | AR24 | 27 | IO_L18N_27 | D41 | NA | GND | AE27 |
| 8 | IO_L9P_CC_ | AU21 | 27 | IO_L19P_27 | E42 | NA | GND | AG27 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| | 8 | | | | | | | |
| 8 | IO_L9N_CC_8 | AT21 | 27 | IO_L19N_27 | D42 | NA | GND | AJ27 |
| 8 | IO_L10P_CC_8 | AV21 | 29 | IO_L0P_29 | AY 4 2 | NA | GND | AN27 |
| 8 | IO_L10N_CC_8 | AV20 | 29 | IO_L0N_29 | AW42 | NA | GND | A28 |
| 8 | IO_L11P_CC_8 | AU24 | 29 | IO_L1P_29 | AW41 | NA | GND | F28 |
| 8 | IO_L11N_CC_8 | AV25 | 29 | IO_L1N_29 | AW40 | NA | GND | L28 |
| 8 | IO_L12P_VRN_8 | AU23 | 29 | IO_L2P_29 | AY 4 0 | NA | GND | T28 |
| 8 | IO_L12N_VRP_8 | AU22 | 29 | IO_L2N_29 | BA41 | NA | GND | V28 |
| 8 | IO_L13P_8 | AV23 | 29 | IO_L3P_29 | BA42 | NA | GND | Y28 |
| 8 | IO_L13N_8 | AV24 | 29 | IO_L3N_29 | BB41 | NA | GND | AB28 |
| 8 | IO_L14P_8 | AR23 | 29 | IO_L4P_29 | BA40 | NA | GND | AD28 |
| 8 | IO_L14N_VREF_8 | AP22 | 29 | IO_L4N_VREF_29 | BB39 | NA | GND | AF28 |
| 8 | IO_L15P_8 | AR22 | 29 | IO_L5P_29 | BB38 | NA | GND | AH28 |
| 8 | IO_L15N_8 | AT22 | 29 | IO_L5N_29 | BA39 | NA | GND | AT28 |
| 8 | IO_L16P_8 | AM22 | 29 | IO_L6P_29 | AY 3 8 | NA | GND | J29 |
| 8 | IO_L16N_8 | AM23 | 29 | IO_L6N_29 | AW37 | NA | GND | P29 |
| 8 | IO_L17P_8 | AN23 | 29 | IO_L7P_29 | AW38 | NA | GND | U29 |
| 8 | IO_L17N_8 | AP23 | 29 | IO_L7N_29 | AY 3 9 | NA | GND | W29 |
| 8 | IO_L18P_8 | AP20 | 29 | IO_L8P_CC_29 | BB37 | NA | GND | AA29 |
| 8 | IO_L18N_8 | AP21 | 29 | IO_L8N_CC_29 | BA37 | NA | GND | AC29 |
| 8 | IO_L19P_8 | AN21 | 29 | IO_L9P_CC_29 | AY 3 7 | NA | GND | AE29 |
| 8 | IO_L19N_8 | AM21 | 29 | IO_L9N_CC_29 | AW36 | NA | GND | AJ29 |
| 11 | IO_L0P_11 | F42 | 29 | IO_L10P_CC_29 | BB36 | NA | GND | AP29 |
| 11 | IO_L0N_11 | G42 | 29 | IO_L10N_CC_29 | BA36 | NA | GND | AW29 |
| 11 | IO_L1P_11 | F41 | 29 | IO_L11P_CC_29 | AY 3 5 | NA | GND | B30 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 11 | IO_L1N_11 | G41 | 29 | IO_L11N_CC_29 | AW35 | NA | GND | M30 |
| 11 | IO_L2P_11 | H41 | 29 | IO_L12P_VRN_29 | BB34 | NA | GND | V30 |
| 11 | IO_L2N_11 | J41 | 29 | IO_L12N_VRP_29 | BA35 | NA | GND | Y30 |
| 11 | IO_L3P_11 | J42 | 29 | IO_L13P_29 | BB33 | NA | GND | AB30 |
| 11 | IO_L3N_11 | K42 | 29 | IO_L13N_29 | BA34 | NA | GND | AD30 |
| 11 | IO_L4P_11 | L40 | 29 | IO_L14P_29 | AY 3 3 | NA | GND | AM30 |
| 11 | IO_L4N_VREF_11 | L41 | 29 | IO_L14N_VREF_29 | AY 3 4 | NA | GND | BB30 |
| 11 | IO_L5P_11 | L42 | 29 | IO_L15P_29 | AW33 | NA | GND | E31 |
| 11 | IO_L5N_11 | M41 | 29 | IO_L15N_29 | AW32 | NA | GND | K31 |
| 11 | IO_L6P_11 | M42 | 29 | IO_L16P_29 | AY 3 2 | NA | GND | R31 |
| 11 | IO_L6N_11 | N41 | 29 | IO_L16N_29 | BA32 | NA | GND | W31 |
| 11 | IO_L7P_11 | N40 | 29 | IO_L17P_29 | BB32 | NA | GND | AA31 |
| 11 | IO_L7N_11 | P40 | 29 | IO_L17N_29 | BB31 | NA | GND | AC31 |
| 11 | IO_L8P_CC_11 | W40 | 29 | IO_L18P_29 | BA30 | NA | GND | AE31 |
| 11 | IO_L8N_CC_11 | Y40 | 29 | IO_L18N_29 | BA31 | NA | GND | AK31 |
| 11 | IO_L9P_CC_11 | AA40 | 29 | IO_L19P_29 | AY 3 0 | NA | GND | AR31 |
| 11 | IO_L9N_CC_11 | AA39 | 29 | IO_L19N_29 | AW31 | NA | GND | H32 |
| 11 | IO_L10P_CC_SM15P_11 | Y39 | 31 | IO_L0P_31 | D20 | NA | GND | N32 |
| 11 | IO_L10N_CC_SM15N_11 | Y38 | 31 | IO_L0N_31 | D21 | NA | GND | V32 |
| 11 | IO_L11P_CC_SM14P_11 | Y37 | 31 | IO_L1P_31 | C21 | NA | GND | AC32 |
| 11 | IO_L11N_CC_SM14N_11 | AA37 | 31 | IO_L1N_31 | C20 | NA | GND | AH32 |
| 11 | IO_L12P_VRN_11 | R42 | 31 | IO_L2P_31 | A20 | NA | GND | AN32 |
| 11 | IO_L12N_VRP_11 | P42 | 31 | IO_L2N_31 | A21 | NA | GND | AV32 |
| 11 | IO_L13P_11 | P41 | 31 | IO_L3P_31 | A22 | NA | GND | A33 |
| 11 | IO_L13N_11 | R40 | 31 | IO_L3N_31 | B21 | NA | GND | L33 |
| 11 | IO_L14P_11 | T40 | 31 | IO_L4P_31 | D22 | NA | GND | T33 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 11 | IO_L14N_VREF_11 | T41 | 31 | IO_L4N_VREF_31 | D23 | NA | GND | AA33 |
| 11 | IO_L15P_SM13P_11 | T42 | 31 | IO_L5P_31 | C23 | NA | GND | AF33 |
| 11 | IO_L15N_SM13N_11 | U41 | 31 | IO_L5N_31 | B22 | NA | GND | AL33 |
| 11 | IO_L16P_SM12P_11 | U42 | 31 | IO_L6P_31 | B23 | NA | GND | BA33 |
| 11 | IO_L16N_SM12N_11 | V41 | 31 | IO_L6N_31 | A24 | NA | GND | D34 |
| 11 | IO_L17P_SM11P_11 | V40 | 31 | IO_L7P_31 | B24 | NA | GND | P34 |
| 11 | IO_L17N_SM11N_11 | W41 | 31 | IO_L7N_31 | C24 | NA | GND | W34 |
| 11 | IO_L18P_SM10P_11 | W42 | 31 | IO_L8P_CC_31 | E24 | NA | GND | AD34 |
| 11 | IO_L18N_SM10N_11 | Y42 | 31 | IO_L8N_CC_31 | E25 | NA | GND | AP34 |
| 11 | IO_L19P_SM9P_11 | AA42 | 31 | IO_L9P_CC_31 | D25 | NA | GND | G35 |
| 11 | IO_L19N_SM9N_11 | AA41 | 31 | IO_L9N_CC_31 | D26 | NA | GND | M35 |
| 12 | IO_L0P_12 | AA7 | 31 | IO_L10P_CC_31 | E28 | NA | GND | U35 |
| 12 | IO_L0N_12 | AA6 | 31 | IO_L10N_CC_31 | E27 | NA | GND | AG35 |
| 12 | IO_L1P_12 | G6 | 31 | IO_L11P_CC_31 | D27 | NA | GND | AU35 |
| 12 | IO_L1N_12 | H5 | 31 | IO_L11N_CC_31 | C26 | NA | GND | BB35 |
| 12 | IO_L2P_12 | W5 | 31 | IO_L12P_VRN_31 | C25 | NA | GND | K36 |
| 12 | IO_L2N_12 | W6 | 31 | IO_L12N_VRP_31 | B26 | NA | GND | Y36 |
| 12 | IO_L3P_12 | H6 | 31 | IO_L13P_31 | A26 | NA | GND | AK36 |
| 12 | IO_L3N_12 | J5 | 31 | IO_L13N_31 | A25 | NA | GND | AY36 |
| 12 | IO_L4P_12 | Y7 | 31 | IO_L14P_31 | A27 | NA | GND | C37 |
| 12 | IO_L4N_VREF_12 | W7 | 31 | IO_L14N_VREF_31 | B27 | NA | GND | N37 |
| 12 | IO_L5P_12 | J6 | 31 | IO_L15P_31 | B28 | NA | GND | AC37 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 12 | IO_L5N_12 | K5 | 31 | IO_L15N_31 | A29 | NA | GND | AN37 |
| 12 | IO_L6P_12 | W8 | 31 | IO_L16P_31 | F30 | NA | GND | A38 |
| 12 | IO_L6N_12 | V8 | 31 | IO_L16N_31 | E30 | NA | GND | F38 |
| 12 | IO_L7P_12 | K4 | 31 | IO_L17P_31 | E29 | NA | GND | T38 |
| 12 | IO_L7N_12 | L5 | 31 | IO_L17N_31 | D30 | NA | GND | AF38 |
| 12 | IO_L8P_CC_12 | V5 | 31 | IO_L18P_31 | C29 | NA | GND | AT38 |
| 12 | IO_L8N_CC_12 | V6 | 31 | IO_L18N_31 | B29 | NA | GND | BA38 |
| 12 | IO_L9P_CC_12 | L6 | 31 | IO_L19P_31 | C28 | NA | GND | J39 |
| 12 | IO_L9N_CC_12 | M6 | 31 | IO_L19N_31 | D28 | NA | GND | W39 |
| 12 | IO_L10P_CC_12 | N5 | 33 | IO_L0P_33 | BB29 | NA | GND | AJ39 |
| 12 | IO_L10N_CC_12 | N6 | 33 | IO_L0N_33 | BB28 | NA | GND | AW39 |
| 12 | IO_L11P_CC_12 | U7 | 33 | IO_L1P_33 | BB27 | NA | GND | B40 |
| 12 | IO_L11N_CC_12 | U6 | 33 | IO_L1N_33 | BA27 | NA | GND | M40 |
| 12 | IO_L12P_VRN_12 | P5 | 33 | IO_L2P_33 | BB26 | NA | GND | AB40 |
| 12 | IO_L12N_VRP_12 | P6 | 33 | IO_L2N_33 | BA26 | NA | GND | AM40 |
| 12 | IO_L13P_12 | T7 | 33 | IO_L3P_33 | BA25 | NA | GND | BB40 |
| 12 | IO_L13N_12 | T6 | 33 | IO_L3N_33 | AY 2 5 | NA | GND | E41 |
| 12 | IO_L14P_12 | R4 | 33 | IO_L4P_33 | AW30 | NA | GND | R41 |
| 12 | IO_L14N_VREF_12 | R5 | 33 | IO_L4N_VREF_33 | AV 3 0 | NA | GND | AE41 |
| 12 | IO_L15P_12 | T5 | 33 | IO_L5P_33 | AV 2 9 | NA | GND | AR41 |
| 12 | IO_L15N_12 | T4 | 33 | IO_L5N_33 | AW28 | NA | GND | AY41 |
| 12 | IO_L16P_12 | AA11 | 33 | IO_L6P_33 | AY 2 7 | NA | GND | C42 |
| 12 | IO_L16N_12 | AA10 | 33 | IO_L6N_33 | AY 2 8 | NA | GND | H42 |
| 12 | IO_L17P_12 | AA9 | 33 | IO_L7P_33 | AY 2 9 | NA | GND | N42 |
| 12 | IO_L17N_12 | Y10 | 33 | IO_L7N_33 | BA29 | NA | GND | V42 |
| 12 | IO_L18P_12 | W11 | 33 | IO_L8P_CC_33 | BB24 | NA | GND | AC42 |
| 12 | IO_L18N_12 | W10 | 33 | IO_L8N_CC_33 | BA24 | NA | GND | AH42 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 12 | IO_L19P_12 | Y9 | 33 | IO_L9P_CC_33 | AY 2 4 | NA | GND | AN42 |
| 12 | IO_L19N_12 | Y8 | 33 | IO_L9N_CC_33 | AW25 | NA | GND | AV42 |
| 13 | IO_L0P_SM8P_13 | AB41 | 33 | IO_L10P_CC_33 | AV 2 8 | NA | VCCAUX | R12 |
| 13 | IO_L0N_SM8N_13 | AB42 | 33 | IO_L10N_CC_33 | AW27 | NA | VCCAUX | U12 |
| 13 | IO_L1P_SM7P_13 | AC41 | 33 | IO_L11P_CC_33 | AV 2 6 | NA | VCCAUX | W12 |
| 13 | IO_L1N_SM7N_13 | AD42 | 33 | IO_L11N_CC_33 | AW26 | NA | VCCAUX | AA12 |
| 13 | IO_L2P_SM6P_13 | AE42 | 33 | IO_L12P_VRN_33 | BB22 | NA | VCCAUX | AC12 |
| 13 | IO_L2N_SM6N_13 | AD41 | 33 | IO_L12N_VRP_33 | BB23 | NA | VCCAUX | AE12 |
| 13 | IO_L3P_SM5P_13 | AF41 | 33 | IO_L13P_33 | BB21 | NA | VCCAUX | AJ12 |
| 13 | IO_L3N_SM5N_13 | AF42 | 33 | IO_L13N_33 | BA22 | NA | VCCAUX | T13 |
| 13 | IO_L4P_13 | AF40 | 33 | IO_L14P_33 | AY 2 2 | NA | VCCAUX | AF13 |
| 13 | IO_L4N_VREF_13 | AG41 | 33 | IO_L14N_VREF_33 | AY 2 3 | NA | VCCAUX | AH13 |
| 13 | IO_L5P_SM4P_13 | AG42 | 33 | IO_L15P_33 | AW23 | NA | VCCAUX | T29 |
| 13 | IO_L5N_SM4N_13 | AH41 | 33 | IO_L15N_33 | AW22 | NA | VCCAUX | AF29 |
| 13 | IO_L6P_SM3P_13 | AJ42 | 33 | IO_L16P_33 | BB20 | NA | VCCAUX | U30 |
| 13 | IO_L6N_SM3N_13 | AJ41 | 33 | IO_L16N_33 | BA21 | NA | VCCAUX | W30 |
| 13 | IO_L7P_SM2P_13 | AH40 | 33 | IO_L17P_33 | BA20 | NA | VCCAUX | AA30 |
| 13 | IO_L7N_SM2N_13 | AJ40 | 33 | IO_L17N_33 | BA19 | NA | VCCAUX | AC30 |
| 13 | IO_L8P_CC_SM1P_13 | AB37 | 33 | IO_L18P_33 | AY 1 9 | NA | VCCAUX | AE30 |
| 13 | IO_L8N_CC_SM1N_13 | AB38 | 33 | IO_L18N_33 | AY 2 0 | NA | VCCAUX | Y31 |
| 13 | IO_L9P_CC_ | AB39 | 33 | IO_L19P_33 | AW21 | NA | VCCAUX | AB31 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| | SM0P_13 | | | | | | | |
| 13 | IO_L9N_CC_SM0N_13 | AC38 | 33 | IO_L19N_33 | AW20 | NA | VCCAUX | AD31 |
| 13 | IO_L10P_CC_13 | AE40 | 34 | IO_L0P_34 | AW18 | NA | VCCINT | V13 |
| 13 | IO_L10N_CC_13 | AD40 | 34 | IO_L0N_34 | AV 1 9 | NA | VCCINT | Y13 |
| 13 | IO_L11P_CC_13 | AC40 | 34 | IO_L1P_34 | AL11 | NA | VCCINT | AB13 |
| 13 | IO_L11N_CC_13 | AC39 | 34 | IO_L1N_34 | AL12 | NA | VCCINT | AD13 |
| 13 | IO_L12P_VRN_13 | AK40 | 34 | IO_L2P_34 | AV 1 8 | NA | VCCINT | U14 |
| 13 | IO_L12N_VRP_13 | AL40 | 34 | IO_L2N_34 | AU17 | NA | VCCINT | W14 |
| 13 | IO_L13P_13 | AL41 | 34 | IO_L3P_34 | AM11 | NA | VCCINT | AA14 |
| 13 | IO_L13N_13 | AK42 | 34 | IO_L3N_34 | AM12 | NA | VCCINT | AC14 |
| 13 | IO_L14P_13 | AL42 | 34 | IO_L4P_34 | AV 1 6 | NA | VCCINT | AE14 |
| 13 | IO_L14N_VREF_13 | AM42 | 34 | IO_L4N_VREF_34 | AU16 | NA | VCCINT | AG14 |
| 13 | IO_L15P_13 | AM41 | 34 | IO_L5P_34 | AN11 | NA | VCCINT | T15 |
| 13 | IO_L15N_13 | AN41 | 34 | IO_L5N_34 | AN10 | NA | VCCINT | V15 |
| 13 | IO_L16P_13 | AP42 | 34 | IO_L6P_34 | AV 1 5 | NA | VCCINT | Y15 |
| 13 | IO_L16N_13 | AP41 | 34 | IO_L6N_34 | AV 1 4 | NA | VCCINT | AB15 |
| 13 | IO_L17P_13 | AR42 | 34 | IO_L7P_34 | AP10 | NA | VCCINT | AD15 |
| 13 | IO_L17N_13 | AT42 | 34 | IO_L7N_34 | AR9 | NA | VCCINT | AF15 |
| 13 | IO_L18P_13 | AT41 | 34 | IO_L8P_CC_34 | AW13 | NA | VCCINT | R16 |
| 13 | IO_L18N_13 | AU41 | 34 | IO_L8N_CC_34 | AV 1 3 | NA | VCCINT | U16 |
| 13 | IO_L19P_13 | AU42 | 34 | IO_L9P_CC_34 | AP11 | NA | VCCINT | W16 |
| 13 | IO_L19N_13 | AV 4 1 | 34 | IO_L9N_CC_34 | AP12 | NA | VCCINT | AA16 |
| 15 | IO_L0P_15 | H38 | 34 | IO_L10P_CC_34 | AR10 | NA | VCCINT | AC16 |
| 15 | IO_L0N_15 | H39 | 34 | IO_L10N_CC_34 | AT10 | NA | VCCINT | AE16 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 15 | IO_L1P_15 | G38 | 34 | IO_L11P_CC_34 | AW12 | NA | VCCINT | AG16 |
| 15 | IO_L1N_15 | G39 | 34 | IO_L11N_CC_34 | AV 11 | NA | VCCINT | T17 |
| 15 | IO_L2P_15 | F39 | 34 | IO_L12P_VRN_34 | AT11 | NA | VCCINT | V17 |
| 15 | IO_L2N_15 | F40 | 34 | IO_L12N_VRP_34 | AR12 | NA | VCCINT | Y17 |
| 15 | IO_L3P_15 | E39 | 34 | IO_L13P_34 | AU11 | NA | VCCINT | AB17 |
| 15 | IO_L3N_15 | E40 | 34 | IO_L13N_34 | AU12 | NA | VCCINT | AD17 |
| 15 | IO_L4P_15 | R39 | 34 | IO_L14P_34 | AR13 | NA | VCCINT | AF17 |
| 15 | IO_L4N_VREF_15 | R38 | 34 | IO_L14N_VREF_34 | AT12 | NA | VCCINT | AH17 |
| 15 | IO_L5P_15 | R37 | 34 | IO_L15P_34 | AU14 | NA | VCCINT | R18 |
| 15 | IO_L5N_15 | P37 | 34 | IO_L15N_34 | AU13 | NA | VCCINT | U18 |
| 15 | IO_L6P_15 | P38 | 34 | IO_L16P_34 | AW7 | NA | VCCINT | W18 |
| 15 | IO_L6N_15 | N38 | 34 | IO_L16N_34 | AV 8 | NA | VCCINT | AA18 |
| 15 | IO_L7P_15 | N39 | 34 | IO_L17P_34 | AV 1 0 | NA | VCCINT | AC18 |
| 15 | IO_L7N_15 | M39 | 34 | IO_L17N_34 | AV 9 | NA | VCCINT | AE18 |
| 15 | IO_L8P_CC_15 | M38 | 34 | IO_L18P_34 | AU9 | NA | VCCINT | AG18 |
| 15 | IO_L8N_CC_15 | L39 | 34 | IO_L18N_34 | AT9 | NA | VCCINT | AJ18 |
| 15 | IO_L9P_CC_15 | K38 | 34 | IO_L19P_34 | AU8 | NA | VCCINT | T19 |
| 15 | IO_L9N_CC_15 | J38 | 34 | IO_L19N_34 | AU7 | NA | VCCINT | V19 |
| 15 | IO_L10P_CC_15 | H40 | NA | MGTTXP0_112 | T2 | NA | VCCINT | Y19 |
| 15 | IO_L10N_CC_15 | J40 | NA | MGTAVTTTX_112 | AA3 | NA | VCCINT | AB19 |
| 15 | IO_L11P_CC_15 | K40 | NA | MGTTXN0_112 | U2 | NA | VCCINT | AD19 |
| 15 | IO_L11N_CC_15 | K39 | NA | MGTRXP0_112 | U1 | NA | VCCINT | AF19 |
| 15 | IO_L12P_VRN_15 | V38 | NA | MGTAVTTRX_112 | U3 | NA | VCCINT | AH19 |
| 15 | IO_L12N_VRP_15 | U37 | NA | MGTRXN0_112 | V1 | NA | VCCINT | R20 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 15 | IO_L13P_15 | T37 | NA | MGTAVCCPLL_112 | Y3 | NA | VCCINT | U20 |
| 15 | IO_L13N_15 | U38 | NA | MGTRXN1_112 | W1 | NA | VCCINT | W20 |
| 15 | IO_L14P_15 | T39 | NA | MGTREFCLKN_112 | V3 | NA | VCCINT | AA20 |
| 15 | IO_L14N_VREF_15 | U39 | NA | MGTRXP1_112 | Y1 | NA | VCCINT | AC20 |
| 15 | IO_L15P_15 | V39 | NA | MGTREFCLKP_112 | V4 | NA | VCCINT | AE20 |
| 15 | IO_L15N_15 | W38 | NA | MGTTXN1_112 | Y2 | NA | VCCINT | AG20 |
| 15 | IO_L16P_15 | AA35 | NA | MGTAVTTTX_112 | T3 | NA | VCCINT | AJ20 |
| 15 | IO_L16N_15 | AA36 | NA | MGTTXP1_112 | AA2 | NA | VCCINT | P21 |
| 15 | IO_L17P_15 | AA34 | NA | MGTAVTTRXC | AA5 | NA | VCCINT | T21 |
| 15 | IO_L17N_15 | Y34 | NA | MGTRREF_112 | AB4 | NA | VCCINT | V21 |
| 15 | IO_L18P_15 | Y35 | NC | NC | Y5 | NA | VCCINT | AD21 |
| 15 | IO_L18N_15 | W35 | NA | MGTTXP0_114 | AB2 | NA | VCCINT | AF21 |
| 15 | IO_L19P_15 | W36 | NA | MGTAVTTTX_114 | AB3 | NA | VCCINT | AH21 |
| 15 | IO_L19N_15 | W37 | NA | MGTTXN0_114 | AC2 | NA | VCCINT | R22 |
| 17 | IO_L0P_17 | AB34 | NA | MGTRXP0_114 | AC1 | NA | VCCINT | U22 |
| 17 | IO_L0N_17 | AC34 | NA | MGTAVTTRX_114 | AC3 | NA | VCCINT | W22 |
| 17 | IO_L1P_17 | AC35 | NA | MGTRXN0_114 | AD1 | NA | VCCINT | AE22 |
| 17 | IO_L1N_17 | AB36 | NA | MGTAVCCPLL_114 | AF3 | NA | VCCINT | AG22 |
| 17 | IO_L2P_17 | AC36 | NA | MGTRXN1_114 | AE1 | NA | VCCINT | P23 |
| 17 | IO_L2N_17 | AD35 | NA | MGTREFCLKN_114 | AD3 | NA | VCCINT | T23 |
| 17 | IO_L3P_17 | AD36 | NA | MGTRXP1_114 | AF1 | NA | VCCINT | V23 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 17 | IO_L3N_17 | AD37 | NA | MGTREFCLKP_114 | AD4 | NA | VCCINT | Y23 |
| 17 | IO_L4P_17 | AE37 | NA | MGTTXN1_114 | AF2 | NA | VCCINT | AB23 |
| 17 | IO_L4N_VREF_17 | AD38 | NA | MGTAVTTTX_114 | AG3 | NA | VCCINT | AD23 |
| 17 | IO_L5P_17 | AE39 | NA | MGTTXP1_114 | AG2 | NA | VCCINT | AF23 |
| 17 | IO_L5N_17 | AE38 | NA | MGTTXP0_116 | K2 | NA | VCCINT | AH23 |
| 17 | IO_L6P_17 | AF39 | NA | MGTAVTTTX_116 | K3 | NA | VCCINT | R24 |
| 17 | IO_L6N_17 | AG38 | NA | MGTTXN0_116 | L2 | NA | VCCINT | U24 |
| 17 | IO_L7P_17 | AG37 | NA | MGTRXP0_116 | L1 | NA | VCCINT | W24 |
| 17 | IO_L7N_17 | AF37 | NA | MGTAVTTRX_116 | L3 | NA | VCCINT | AA24 |
| 17 | IO_L8P_CC_17 | AN40 | NA | MGTRXN0_116 | M1 | NA | VCCINT | AC24 |
| 17 | IO_L8N_CC_17 | AP40 | NA | MGTAVCCPLL_116 | P3 | NA | VCCINT | AE24 |
| 17 | IO_L9P_CC_17 | AR40 | NA | MGTRXN1_116 | N1 | NA | VCCINT | AG24 |
| 17 | IO_L9N_CC_17 | AT40 | NA | MGTREFCLKN_116 | M3 | NA | VCCINT | AJ24 |
| 17 | IO_L10P_CC_17 | AV 4 0 | NA | MGTRXP1_116 | P1 | NA | VCCINT | T25 |
| 17 | IO_L10N_CC_17 | AU39 | NA | MGTREFCLKP_116 | M4 | NA | VCCINT | V25 |
| 17 | IO_L11P_CC_17 | AT39 | NA | MGTTXN1_116 | P2 | NA | VCCINT | Y25 |
| 17 | IO_L11N_CC_17 | AR39 | NA | MGTAVTTTX_116 | R3 | NA | VCCINT | AB25 |
| 17 | IO_L12P_VRN_17 | AG39 | NA | MGTTXP1_116 | R2 | NA | VCCINT | AD25 |
| 17 | IO_L12N_VRP_17 | AH39 | NA | MGTTXP0_118 | AH2 | NA | VCCINT | AF25 |
| 17 | IO_L13P_17 | AJ38 | NA | MGTAVTTTX_118 | AH3 | NA | VCCINT | AH25 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 17 | IO_L13N_17 | AK39 | NA | MGTTXN0_118 | AJ2 | NA | VCCINT | R26 |
| 17 | IO_L14P_17 | AK38 | NA | MGTRXP0_118 | AJ1 | NA | VCCINT | U26 |
| 17 | IO_L14N_VREF_17 | AK37 | NA | MGTAVTTRX_118 | AJ3 | NA | VCCINT | W26 |
| 17 | IO_L15P_17 | AJ37 | NA | MGTRXN0_118 | AK1 | NA | VCCINT | AA26 |
| 17 | IO_L15N_17 | AH38 | NA | MGTAVCCPLL_118 | AM3 | NA | VCCINT | AC26 |
| 17 | IO_L16P_17 | AL39 | NA | MGTRXN1_118 | AL1 | NA | VCCINT | AE26 |
| 17 | IO_L16N_17 | AM39 | NA | MGTREFCLKN_118 | AK3 | NA | VCCINT | AG26 |
| 17 | IO_L17P_17 | AN39 | NA | MGTRXP1_118 | AM1 | NA | VCCINT | T27 |
| 17 | IO_L17N_17 | AP38 | NA | MGTREFCLKP_118 | AK4 | NA | VCCINT | V27 |
| 17 | IO_L18P_17 | AN38 | NA | MGTTXN1_118 | AM2 | NA | VCCINT | Y27 |
| 17 | IO_L18N_17 | AM38 | NA | MGTAVTTTX_118 | AN3 | NA | VCCINT | AB27 |
| 17 | IO_L19P_17 | AM37 | NA | MGTTXP1_118 | AN2 | NA | VCCINT | AD27 |
| 17 | IO_L19N_17 | AL37 | NA | MGTTXP0_120 | D2 | NA | VCCINT | AF27 |
| 18 | IO_L0P_18 | AJ7 | NA | MGTAVTTTX_120 | D3 | NA | VCCINT | AH27 |
| 18 | IO_L0N_18 | AK7 | NA | MGTTXN0_120 | E2 | NA | VCCINT | R28 |
| 18 | IO_L1P_18 | AB11 | NA | MGTRXP0_120 | E1 | NA | VCCINT | U28 |
| 18 | IO_L1N_18 | AC10 | NA | MGTAVTTRX_120 | E3 | NA | VCCINT | W28 |
| 18 | IO_L2P_18 | AL5 | NA | MGTRXN0_120 | F1 | NA | VCCINT | AA28 |
| 18 | IO_L2N_18 | AK5 | NA | MGTAVCCPLL_120 | H3 | NA | VCCINT | AC28 |
| 18 | IO_L3P_18 | AB9 | NA | MGTRXN1_120 | G1 | NA | VCCINT | AE28 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 18 | IO_L3N_18 | AB8 | NA | MGTREFCLKN_120 | F3 | NA | VCCINT | AG28 |
| 18 | IO_L4P_18 | AJ6 | NA | MGTRXP1_120 | H1 | NA | VCCINT | V29 |
| 18 | IO_L4N_VREF_18 | AJ5 | NA | MGTREFCLKP_120 | F4 | NA | VCCINT | Y29 |
| 18 | IO_L5P_18 | AC8 | NA | MGTTXN1_120 | H2 | NA | VCCINT | AB29 |
| 18 | IO_L5N_18 | AC9 | NA | MGTAVTTTX_120 | J3 | NA | VCCINT | AD29 |
| 18 | IO_L6P_18 | AH6 | NA | MGTTXP1_120 | J2 | 0 | VCCO_0 | AL28 |
| 18 | IO_L6N_18 | AH5 | NA | MGTTXP0_122 | AP2 | 0 | VCCO_0 | AG30 |
| 18 | IO_L7P_18 | AD10 | NA | MGTAVTTTX_122 | AP3 | 1 | VCCO_1 | F13 |
| 18 | IO_L7N_18 | AD11 | NA | MGTTXN0_122 | AR2 | 1 | VCCO_1 | J14 |
| 18 | IO_L8P_CC_18 | AG4 | NA | MGTRXP0_122 | AR1 | 2 | VCCO_2 | AR26 |
| 18 | IO_L8N_CC_18 | AH4 | NA | MGTAVTTRX_122 | AR3 | 2 | VCCO_2 | AV27 |
| 18 | IO_L9P_CC_18 | AB7 | NA | MGTRXN0_122 | AT1 | 3 | VCCO_3 | E26 |
| 18 | IO_L9N_CC_18 | AB6 | NA | MGTAVCCPLL_122 | AV 3 | 3 | VCCO_3 | H27 |
| 18 | IO_L10P_CC_18 | AC5 | NA | MGTRXN1_122 | AU1 | 4 | VCCO_4 | AT13 |
| 18 | IO_L10N_CC_18 | AC6 | NA | MGTREFCLKN_122 | AT3 | 4 | VCCO_4 | AR16 |
| 18 | IO_L11P_CC_18 | AF5 | NA | MGTRXP1_122 | AV 1 | 5 | VCCO_5 | C22 |
| 18 | IO_L11N_CC_18 | AF6 | NA | MGTREFCLKP_122 | AT4 | 5 | VCCO_5 | F23 |
| 18 | IO_L12P_VRN_18 | AD6 | NA | MGTTXN1_122 | AV 2 | 5 | VCCO_5 | B25 |
| 18 | IO_L12N_VRP_18 | AD7 | NA | MGTAVTTTX_122 | AW3 | 6 | VCCO_6 | AY21 |
| 18 | IO_L13P_18 | AG6 | NA | MGTTXP1_122 | AW2 | 6 | VCCO_6 | AT23 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 18 | IO_L13N_18 | AG7 | NA | MGTTXP0_124 | B6 | 6 | VCCO_6 | AW24 |
| 18 | IO_L14P_18 | AE5 | NA | MGTAVTTTX_124 | C1 | 7 | VCCO_7 | H17 |
| 18 | IO_L14N_VREF_18 | AD5 | NA | MGTTXN0_124 | B5 | 7 | VCCO_7 | D19 |
| 18 | IO_L15P_18 | AF7 | NA | MGTRXP0_124 | A5 | 7 | VCCO_7 | G20 |
| 18 | IO_L15N_18 | AE7 | NA | MGTAVTTRX_124 | C5 | 8 | VCCO_8 | AV17 |
| 18 | IO_L16P_18 | AD8 | NA | MGTRXN0_124 | A4 | 8 | VCCO_8 | AP19 |
| 18 | IO_L16N_18 | AE8 | NA | MGTAVCCPLL_124 | C2 | 8 | VCCO_8 | AU20 |
| 18 | IO_L17P_18 | AF9 | NA | MGTRXN1_124 | A3 | 11 | VCCO_11 | V37 |
| 18 | IO_L17N_18 | AF10 | NA | MGTREFCLKN_124 | C3 | 11 | VCCO_11 | AA38 |
| 18 | IO_L18P_18 | AE9 | NA | MGTRXP1_124 | A2 | 11 | VCCO_11 | Y41 |
| 18 | IO_L18N_18 | AE10 | NA | MGTREFCLKP_124 | C4 | 12 | VCCO_12 | V7 |
| 18 | IO_L19P_18 | AF11 | NA | MGTTXN1_124 | B2 | 12 | VCCO_12 | AA8 |
| 18 | IO_L19N_18 | AF12 | NA | MGTAVTTTX_124 | C6 | 12 | VCCO_12 | U10 |
| 19 | IO_L0P_19 | R34 | NA | MGTTXP1_124 | B1 | 13 | VCCO_13 | AB35 |
| 19 | IO_L0N_19 | P35 | NA | MGTTXP0_126 | BA1 | 13 | VCCO_13 | AE36 |
| 19 | IO_L1P_19 | N35 | NA | MGTAVTTTX_126 | AY 1 | 13 | VCCO_13 | AD39 |
| 19 | IO_L1N_19 | M36 | NA | MGTTXN0_126 | BA2 | 15 | VCCO_15 | R36 |
| 19 | IO_L2P_19 | L37 | NA | MGTRXP0_126 | BB2 | 15 | VCCO_15 | P39 |
| 19 | IO_L2N_19 | M37 | NA | MGTAVTTRX_126 | AY 2 | 15 | VCCO_15 | U40 |
| 19 | IO_L3P_19 | N36 | NA | MGTRXN0_126 | BB3 | 17 | VCCO_17 | AH37 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 19 | IO_L3N_19 | P36 | NA | MGTAVCCPLL_126 | AY 5 | 17 | VCCO_17 | AG40 |
| 19 | IO_L4P_19 | L36 | NA | MGTRXN1_126 | BB4 | 17 | VCCO_17 | AK41 |
| 19 | IO_L4N_VREF_19 | L35 | NA | MGTREFCLKN_126 | AY 4 | 18 | VCCO_18 | AE6 |
| 19 | IO_L5P_19 | K35 | NA | MGTRXP1_126 | BB5 | 18 | VCCO_18 | AD9 |
| 19 | IO_L5N_19 | J35 | NA | MGTREFCLKP_126 | AW4 | 18 | VCCO_18 | AG10 |
| 19 | IO_L6P_19 | H35 | NA | MGTTXN1_126 | BA5 | 19 | VCCO_19 | L38 |
| 19 | IO_L6N_19 | J36 | NA | MGTAVTTTX_126 | AY 6 | 19 | VCCO_19 | G40 |
| 19 | IO_L7P_19 | K37 | NA | MGTTXP1_126 | BA6 | 19 | VCCO_19 | K41 |
| 19 | IO_L7N_19 | J37 | NA | MGTTXP0_128 | B12 | 20 | VCCO_20 | R6 |
| 19 | IO_L8P_CC_19 | U34 | NA | MGTAVTTTX_128 | C12 | 20 | VCCO_20 | L8 |
| 19 | IO_L8N_CC_19 | T35 | NA | MGTTXN0_128 | B11 | 20 | VCCO_20 | P9 |
| 19 | IO_L9P_CC_19 | T34 | NA | MGTRXP0_128 | A11 | 21 | VCCO_21 | AJ34 |
| 19 | IO_L9N_CC_19 | U33 | NA | MGTAVTTRX_128 | C11 | 21 | VCCO_21 | AM35 |
| 19 | IO_L10P_CC_19 | R35 | NA | MGTRXN0_128 | A10 | 21 | VCCO_21 | AL38 |
| 19 | IO_L10N_CC_19 | T36 | NA | MGTAVCCPLL_128 | C8 | 23 | VCCO_23 | E36 |
| 19 | IO_L11P_CC_19 | U36 | NA | MGTRXN1_128 | A9 | 23 | VCCO_23 | H37 |
| 19 | IO_L11N_CC_19 | V36 | NA | MGTREFCLKN_128 | C10 | 23 | VCCO_23 | D39 |
| 19 | IO_L12P_VRN_19 | H36 | NA | MGTRXP1_128 | A8 | 24 | VCCO_24 | E6 |
| 19 | IO_L12N_VRP_19 | G37 | NA | MGTREFCLKP_128 | D10 | 24 | VCCO_24 | H7 |
| 19 | IO_L13P_19 | F36 | NA | MGTTXN1_128 | B8 | 24 | VCCO_24 | G10 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 19 | IO_L13N_19 | G36 | NA | MGTAVTTTX_128 | C7 | 25 | VCCO_25 | AR36 |
| 19 | IO_L14P_19 | F37 | NA | MGTTXP1_128 | B7 | 25 | VCCO_25 | AP39 |
| 19 | IO_L14N_VREF_19 | E37 | NA | MGTTXP0_130 | BA7 | 25 | VCCO_25 | AU40 |
| 19 | IO_L15P_19 | E38 | NA | MGTAVTTTX_130 | AY 1 2 | 26 | VCCO_26 | AH7 |
| 19 | IO_L15N_19 | D37 | NA | MGTTXN0_130 | BA8 | 26 | VCCO_26 | AL8 |
| 19 | IO_L16P_19 | V35 | NA | MGTRXP0_130 | BB8 | 26 | VCCO_26 | AK11 |
| 19 | IO_L16N_19 | V34 | NA | MGTAVTTRX_130 | AY 8 | 27 | VCCO_27 | F33 |
| 19 | IO_L17P_19 | V33 | NA | MGTRXN0_130 | BB9 | 27 | VCCO_27 | J34 |
| 19 | IO_L17N_19 | W33 | NA | MGTAVCCPLL_130 | AY 11 | 27 | VCCO_27 | B35 |
| 19 | IO_L18P_19 | Y33 | NA | MGTRXN1_130 | BB10 | 29 | VCCO_29 | AT33 |
| 19 | IO_L18N_19 | W32 | NA | MGTREFCLKN_130 | AY 9 | 29 | VCCO_29 | AW34 |
| 19 | IO_L19P_19 | Y32 | NA | MGTRXP1_130 | BB11 | 29 | VCCO_29 | AV37 |
| 19 | IO_L19N_19 | AA32 | NA | MGTREFCLKP_130 | AW9 | 31 | VCCO_31 | D29 |
| 20 | IO_L0P_20 | N9 | NA | MGTTXN1_130 | BA11 | 31 | VCCO_31 | G30 |
| 20 | IO_L0N_20 | N8 | NA | MGTAVTTTX_130 | AY 7 | 31 | VCCO_31 | C32 |
| 20 | IO_L1P_20 | E9 | NA | MGTTXP1_130 | BA12 | 33 | VCCO_33 | BA28 |
| 20 | IO_L1N_20 | E8 | NA | MGTTXP0_132 | B18 | 33 | VCCO_33 | AU30 |
| 20 | IO_L2P_20 | P7 | NA | MGTAVTTTX_132 | C13 | 33 | VCCO_33 | AY31 |
| 20 | IO_L2N_20 | P8 | NA | MGTTXN0_132 | B17 | 34 | VCCO_34 | AV7 |
| 20 | IO_L3P_20 | D7 | NA | MGTRXP0_132 | A17 | 34 | VCCO_34 | AP9 |

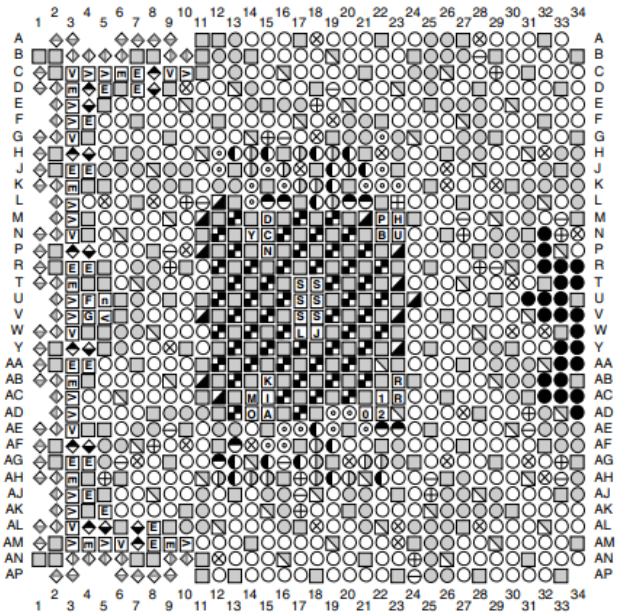
| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 20 | IO_L3N_20 | E7 | NA | MGTAVTTRX_132 | C17 | 34 | VCCO_34 | AU10 |
| 20 | IO_L4P_20 | R7 | NA | MGTRXN0_132 | A16 | NA | MGTAVCC_112 | W3 |
| 20 | IO_L4N_VREF_20 | R8 | NA | MGTAVCCPLL_132 | C14 | NA | MGTAVCC_112 | W4 |
| 20 | IO_L5P_20 | F7 | NA | MGTRXN1_132 | A15 | NA | MGTAVCC_114 | AE3 |
| 20 | IO_L5N_20 | F6 | NA | MGTREFCLKN_132 | C16 | NA | MGTAVCC_114 | AE4 |
| 20 | IO_L6P_20 | R9 | NA | MGTRXP1_132 | A14 | NA | MGTAVCC_116 | N3 |
| 20 | IO_L6N_20 | T9 | NA | MGTREFCLKP_132 | D16 | NA | MGTAVCC_116 | N4 |
| 20 | IO_L7P_20 | E5 | NA | MGTTXN1_132 | B14 | NA | MGTAVCC_118 | AL3 |
| 20 | IO_L7N_20 | F5 | NA | MGTAVTTTX_132 | C18 | NA | MGTAVCC_118 | AL4 |
| 20 | IO_L8P_CC_20 | V9 | NA | MGTTXP1_132 | B13 | NA | MGTAVCC_120 | G3 |
| 20 | IO_L8N_CC_20 | V10 | NA | MGTTXP0_134 | BA13 | NA | MGTAVCC_120 | G4 |
| 20 | IO_L9P_CC_20 | F9 | NA | MGTAVTTTX_134 | AY 1 3 | NA | MGTAVCC_122 | AU3 |
| 20 | IO_L9N_CC_20 | G9 | NA | MGTTXN0_134 | BA14 | NA | MGTAVCC_122 | AU4 |
| 20 | IO_L10P_CC_20 | G7 | NA | MGTRXP0_134 | BB14 | NA | MGTAVCC_124 | D4 |
| 20 | IO_L10N_CC_20 | G8 | NA | MGTAVTTRX_134 | AY 1 4 | NA | MGTAVCC_124 | D5 |
| 20 | IO_L11P_CC_20 | U8 | NA | MGTRXN0_134 | BB15 | NA | MGTAVCC_126 | AW5 |
| 20 | IO_L11N_CC_20 | U9 | NA | MGTAVCCPLL_134 | AY 1 7 | NA | MGTAVCC_126 | AY3 |
| 20 | IO_L12P_VRN_20 | H8 | NA | MGTRXN1_134 | BB16 | NA | MGTAVCC_128 | C9 |
| 20 | IO_L12N_VRP_20 | H9 | NA | MGTREFCLKN_134 | AY 1 5 | NA | MGTAVCC_128 | D9 |
| 20 | IO_L13P_20 | T10 | NA | MGTRXP1_134 | BB17 | NA | MGTAVCC_130 | AW10 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 20 | IO_L13N_20 | T11 | NA | MGTREFCLKP_134 | AW15 | NA | MGTAVCC_130 | AY10 |
| 20 | IO_L14P_20 | J8 | NA | MGTTXN1_134 | BA17 | NA | MGTAVCC_132 | C15 |
| 20 | IO_L14N_VREF_20 | J7 | NA | MGTAVTTTX_134 | AY 1 8 | NA | MGTAVCC_132 | D15 |
| 20 | IO_L15P_20 | U11 | NA | MGTTXP1_134 | BA18 | NA | MGTAVCC_134 | AW16 |
| 20 | IO_L15N_20 | V11 | | | | NA | MGTAVCC_134 | AY16 |
| 20 | IO_L16P_20 | K8 | | | | NA | FLOAT | AA4 |

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

As shown in Table 27, the BQ5VLX155T device is available in the CCGA1136 packages.



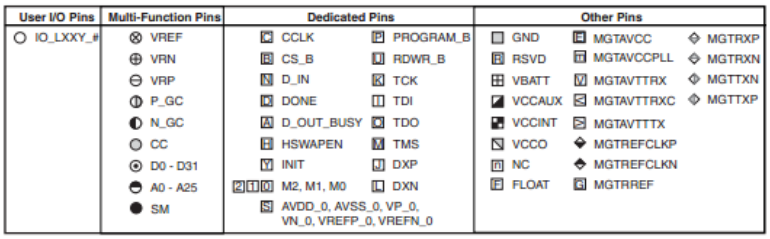


Table 27 BQ5VLX155T packages

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 0 | DXP_0 | W18 | 17 | IO_L16P_17 | AJ31 | NA | MGTRXP0_124 | A9 |
| 0 | DXN_0 | W17 | 17 | IO_L16N_17 | AK31 | NA | MGTAVTTRX_124 | C9 |
| 0 | AVDD_0 | T18 | 17 | IO_L17P_17 | AF29 | NA | MGTRXN0_124 | A8 |
| 0 | AVSS_0 | T17 | 17 | IO_L17N_17 | AF30 | NA | MGTAVCCPLL_124 | C6 |
| 0 | VP_0 | U18 | 17 | IO_L18P_17 | AJ30 | NA | MGTRXN1_124 | A7 |
| 0 | VN_0 | V17 | 17 | IO_L18N_17 | AH30 | NA | MGTREFCLKN_124 | C8 |
| 0 | VREFP_0 | V18 | 17 | IO_L19P_17 | AH29 | NA | MGTRXP1_124 | A6 |
| 0 | VREFN_0 | U17 | 17 | IO_L19N_17 | AG30 | NA | MGTREFCLKP_124 | D8 |
| 0 | VBATT_0 | L23 | 18 | IO_L0P_18 | AC4 | NA | MGTTXN1_124 | B6 |
| 0 | PROGRAM_B_0 | M22 | 18 | IO_L0N_18 | AC5 | NA | MGTAVTTTX_124 | C5 |
| 0 | HSWAPEN_0 | M23 | 18 | IO_L1P_18 | AB6 | NA | MGTTXP1_124 | B5 |
| 0 | D_IN_0 | P15 | 18 | IO_L1N_18 | AB7 | NA | MGTTXP0_126 | AN5 |
| 0 | DONE_0 | M15 | 18 | IO_L2P_18 | AA5 | NA | MGTAVTTTX_126 | AM10 |
| 0 | CCLK_0 | N15 | 18 | IO_L2N_18 | AB5 | NA | MGTTXN0_126 | AN6 |
| 0 | INIT_B_0 | N14 | 18 | IO_L3P_18 | AC7 | NA | MGTRXP0_126 | AP6 |
| 0 | CS_B_0 | N22 | 18 | IO_L3N_18 | AD7 | NA | MGTAVTTRX_126 | AM6 |
| 0 | RDWR_B_0 | N23 | 18 | IO_L4P_18 | Y8 | NA | MGTRXN0_126 | AP7 |
| 0 | RSVD(3) | AB23 | 18 | IO_L4N_VREF_18 | Y9 | NA | MGTAVCCPLL_126 | AM9 |
| 0 | RSVD(3) | AC23 | 18 | IO_L5P_18 | AD4 | NA | MGTRXN1_126 | AP8 |
| 0 | TCK_0 | AB15 | 18 | IO_L5N_18 | AD5 | NA | MGTREFCLKN_126 | AM7 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 0 | M0_0 | AD21 | 18 | IO_L6P_18 | AA6 | NA | MGTRXP1_126 | AP9 |
| 0 | M2_0 | AD22 | 18 | IO_L6N_18 | Y7 | NA | MGTREFCLKP_126 | AL7 |
| 0 | M1_0 | AC22 | 18 | IO_L7P_18 | AD6 | NA | MGTTXN1_126 | AN9 |
| 0 | TMS_0 | AC14 | 18 | IO_L7N_18 | AE6 | NA | MGTAVTTTX_126 | AM5 |
| 0 | TDI_0 | AC15 | 18 | IO_L8P_CC_18 | W6 | NA | MGTTXP1_126 | AN10 |
| 0 | D_OUT_BUSY_0 | AD15 | 18 | IO_L8N_CC_18 | Y6 | NA | GND | B1 |
| 0 | TDO_0 | AD14 | 18 | IO_L9P_CC_18 | AE7 | NA | GND | AN1 |
| 1 | IO_L0P_A19_1 | L21 | 18 | IO_L9N_CC_18 | AF6 | NA | GND | B2 |
| 1 | IO_L0N_A18_1 | L20 | 18 | IO_L10P_CC_18 | AG5 | NA | GND | C2 |
| 1 | IO_L1P_A17_1 | L15 | 18 | IO_L10N_CC_18 | AF5 | NA | GND | H2 |
| 1 | IO_L1N_A16_1 | L16 | 18 | IO_L11P_CC_18 | W7 | NA | GND | J2 |
| 1 | IO_L2P_A15_D31_1 | J22 | 18 | IO_L11N_CC_18 | V7 | NA | GND | P2 |
| 1 | IO_L2N_A14_D30_1 | K21 | 18 | IO_L12P_VRN_18 | AH5 | NA | GND | R2 |
| 1 | IO_L3P_A13_D29_1 | K16 | 18 | IO_L12N_VRP_18 | AG6 | NA | GND | Y2 |
| 1 | IO_L3N_A12_D28_1 | J15 | 18 | IO_L13P_18 | Y11 | NA | GND | AA2 |
| 1 | IO_L4P_A11_D27_1 | G22 | 18 | IO_L13N_18 | W11 | NA | GND | AF2 |
| 1 | IO_L4N_VREF_A10_D26_1 | H22 | 18 | IO_L14P_18 | AH7 | NA | GND | AG2 |
| 1 | IO_L5P_A9_D25_1 | L14 | 18 | IO_L14N_VREF_18 | AG7 | NA | GND | AM2 |
| 1 | IO_L5N_A8_D24_1 | K14 | 18 | IO_L15P_18 | W10 | NA | GND | AN2 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 1 | IO_L6P_A7_D23_1 | K23 | 18 | IO_L15N_18 | W9 | NA | GND | G4 |
| 1 | IO_L6N_A6_D22_1 | K22 | 18 | IO_L16P_18 | AJ7 | NA | GND | K4 |
| 1 | IO_L7P_A5_D21_1 | J12 | 18 | IO_L16N_18 | AJ6 | NA | GND | M4 |
| 1 | IO_L7N_A4_D20_1 | H12 | 18 | IO_L17P_18 | V8 | NA | GND | N4 |
| 1 | IO_L8P_CC_A3_D19_1 | G23 | 18 | IO_L17N_18 | U8 | NA | GND | T4 |
| 1 | IO_L8N_CC_A2_D18_1 | H23 | 18 | IO_L18P_18 | AK7 | NA | GND | W4 |
| 1 | IO_L9P_CC_A1_D17_1 | K13 | 18 | IO_L18N_18 | AK6 | NA | GND | AB4 |
| 1 | IO_L9N_CC_A0_D16_1 | K12 | 18 | IO_L19P_18 | V10 | NA | GND | AE4 |
| 2 | IO_L0P_CC_RS1_2 | AE13 | 18 | IO_L19N_18 | V9 | NA | GND | AH4 |
| 2 | IO_L0N_CC_RS0_2 | AE12 | 19 | IO_L0P_19 | K24 | NA | GND | AK4 |
| 2 | IO_L1P_CC_A25_2 | AF23 | 19 | IO_L0N_19 | L24 | NA | GND | E5 |
| 2 | IO_L1N_CC_A24_2 | AG23 | 19 | IO_L1P_19 | L25 | NA | GND | K5 |
| 2 | IO_L2P_A23_2 | AF13 | 19 | IO_L1N_19 | L26 | NA | GND | R5 |
| 2 | IO_L2N_A22_2 | AG12 | 19 | IO_L2P_19 | J24 | NA | GND | T5 |
| 2 | IO_L3P_A21_2 | AE22 | 19 | IO_L2N_19 | J25 | NA | GND | W5 |
| 2 | IO_L3N_A20_2 | AE23 | 19 | IO_L3P_19 | M25 | NA | GND | Y5 |
| 2 | IO_L4P_FCS_B_2 | AE14 | 19 | IO_L3N_19 | M26 | NA | GND | AE5 |
| 2 | IO_L4N_VREF_FOE_B_MOSI_2 | AF14 | 19 | IO_L4P_19 | J27 | NA | GND | AJ5 |
| 2 | IO_L5P_FWE_B_2 | AF20 | 19 | IO_L4N_VREF_19 | J26 | NA | GND | D6 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 2 | IO_L5N_CSO_B_2 | AF21 | 19 | IO_L5P_19 | G25 | NA | GND | H6 |
| 2 | IO_L6P_D7_2 | AF15 | 19 | IO_L5N_19 | G26 | NA | GND | U6 |
| 2 | IO_L6N_D6_2 | AE16 | 19 | IO_L6P_19 | H25 | NA | GND | V6 |
| 2 | IO_L7P_D5_2 | AE21 | 19 | IO_L6N_19 | H24 | NA | GND | AH6 |
| 2 | IO_L7N_D4_2 | AD20 | 19 | IO_L7P_19 | F25 | NA | GND | AL6 |
| 2 | IO_L8P_D3_2 | AF16 | 19 | IO_L7N_19 | F26 | NA | GND | B7 |
| 2 | IO_L8N_D2_FS2_2 | AE17 | 19 | IO_L8P_CC_19 | G27 | NA | GND | F7 |
| 2 | IO_L9P_D1_FS1_2 | AE19 | 19 | IO_L8N_CC_19 | H27 | NA | GND | L7 |
| 2 | IO_L9N_D0_FS0_2 | AD19 | 19 | IO_L9P_CC_19 | H28 | NA | GND | AA7 |
| 3 | IO_L0P_CC_GC_3 | H17 | 19 | IO_L9N_CC_19 | G28 | NA | GND | AN7 |
| 3 | IO_L0N_CC_GC_3 | H18 | 19 | IO_L10P_CC_19 | E28 | NA | GND | B8 |
| 3 | IO_L1P_CC_GC_3 | K17 | 19 | IO_L10N_CC_19 | F28 | NA | GND | P8 |
| 3 | IO_L1N_CC_GC_3 | L18 | 19 | IO_L11P_CC_19 | E26 | NA | GND | AD8 |
| 3 | IO_L2P_GC_VRN_3 | G15 | 19 | IO_L11N_CC_19 | E27 | NA | GND | AN8 |
| 3 | IO_L2N_GC_VRP_3 | G16 | 19 | IO_L12P_VRN_19 | N27 | NA | GND | D9 |
| 3 | IO_L3P_GC_3 | K18 | 19 | IO_L12N_VRP_19 | M27 | NA | GND | G9 |
| 3 | IO_L3N_GC_3 | J19 | 19 | IO_L13P_19 | K28 | NA | GND | U9 |
| 3 | IO_L4P_GC_3 | J16 | 19 | IO_L13N_19 | L28 | NA | GND | AG9 |
| 3 | IO_L4N_GC_VREF_3 | J17 | 19 | IO_L14P_19 | K27 | NA | GND | AL9 |
| 3 | IO_L5P_GC_3 | L19 | 19 | IO_L14N_VREF_19 | K26 | NA | GND | K10 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 3 | IO_L5N_GC_3 | K19 | 19 | IO_L15P_19 | M28 | NA | GND | R10 |
| 3 | IO_L6P_GC_3 | H14 | 19 | IO_L15N_19 | N28 | NA | GND | Y10 |
| 3 | IO_L6N_GC_3 | H15 | 19 | IO_L16P_19 | P26 | NA | GND | AE10 |
| 3 | IO_L7P_GC_3 | J20 | 19 | IO_L16N_19 | P27 | NA | GND | AK10 |
| 3 | IO_L7N_GC_3 | J21 | 19 | IO_L17P_19 | N24 | NA | GND | A11 |
| 3 | IO_L8P_GC_3 | J14 | 19 | IO_L17N_19 | P24 | NA | GND | B11 |
| 3 | IO_L8N_GC_3 | H13 | 19 | IO_L18P_19 | P25 | NA | GND | C11 |
| 3 | IO_L9P_GC_3 | H19 | 19 | IO_L18N_19 | N25 | NA | GND | N11 |
| 3 | IO_L9N_GC_3 | H20 | 19 | IO_L19P_19 | R24 | NA | GND | U11 |
| 4 | IO_L0P_GC_D15_4 | AG22 | 19 | IO_L19N_19 | T24 | NA | GND | AA11 |
| 4 | IO_L0N_GC_D14_4 | AH22 | 20 | IO_L0P_20 | E9 | NA | GND | AC11 |
| 4 | IO_L1P_GC_D13_4 | AH12 | 20 | IO_L0N_20 | E8 | NA | GND | AN11 |
| 4 | IO_L1N_GC_D12_4 | AG13 | 20 | IO_L1P_20 | F9 | NA | GND | AP11 |
| 4 | IO_L2P_GC_D11_4 | AH20 | 20 | IO_L1N_20 | F8 | NA | GND | A12 |
| 4 | IO_L2N_GC_D10_4 | AH19 | 20 | IO_L2P_20 | F10 | NA | GND | F12 |
| 4 | IO_L3P_GC_D9_4 | AH14 | 20 | IO_L2N_20 | G10 | NA | GND | M12 |
| 4 | IO_L3N_GC_D8_4 | AH13 | 20 | IO_L3P_20 | G8 | NA | GND | P12 |
| 4 | IO_L4P_GC_4 | AG21 | 20 | IO_L3N_20 | H8 | NA | GND | T12 |
| 4 | IO_L4N_GC_VREF_4 | AG20 | 20 | IO_L4P_20 | D11 | NA | GND | V12 |
| 4 | IO_L5P_GC_4 | AH15 | 20 | IO_L4N_VREF_20 | D10 | NA | GND | Y12 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 4 | IO_L5N_GC_4 | AG15 | 20 | IO_L5P_20 | K11 | NA | GND | AB12 |
| 4 | IO_L6P_GC_4 | AG18 | 20 | IO_L5N_20 | J11 | NA | GND | AD12 |
| 4 | IO_L6N_GC_4 | AF19 | 20 | IO_L6P_20 | D12 | NA | GND | AF12 |
| 4 | IO_L7P_GC_VRN_4 | AH17 | 20 | IO_L6N_20 | C12 | NA | GND | J13 |
| 4 | IO_L7N_GC_VRP_4 | AG16 | 20 | IO_L7P_20 | H10 | NA | GND | L13 |
| 4 | IO_L8P_CC_GC_4 | AF18 | 20 | IO_L7N_20 | H9 | NA | GND | N13 |
| 4 | IO_L8N_CC_GC_4 | AE18 | 20 | IO_L8P_CC_20 | A13 | NA | GND | R13 |
| 4 | IO_L9P_CC_GC_4 | AH18 | 20 | IO_L8N_CC_20 | B12 | NA | GND | U13 |
| 4 | IO_L9N_CC_GC_4 | AG17 | 20 | IO_L9P_CC_20 | J10 | NA | GND | W13 |
| 5 | IO_L0P_5 | B16 | 20 | IO_L9N_CC_20 | J9 | NA | GND | AA13 |
| 5 | IO_L0N_5 | B15 | 20 | IO_L10P_CC_20 | K8 | NA | GND | AC13 |
| 5 | IO_L1P_5 | A15 | 20 | IO_L10N_CC_20(2 | K9 | NA | GND | AJ13 |
| 5 | IO_L1N_5 | A14 | 20 | IO_L11P_CC_20 | B13 | NA | GND | AP13 |
| 5 | IO_L2P_5 | B17 | 20 | IO_L11N_CC_20(2 | C13 | NA | GND | B14 |
| 5 | IO_L2N_5 | A16 | 20 | IO_L12P_VRN_20 | L10 | NA | GND | M14 |
| 5 | IO_L3P_5 | C14 | 20 | IO_L12N_VRP_20 | L11 | NA | GND | P14 |
| 5 | IO_L3N_5 | C15 | 20 | IO_L13P_20 | G11 | NA | GND | T14 |
| 5 | IO_L4P_5 | E19 | 20 | IO_L13N_20 | G12 | NA | GND | V14 |
| 5 | IO_L4N_VREF_5 | F19 | 20 | IO_L14P_20 | M8 | NA | GND | Y14 |
| 5 | IO_L5P_5 | C17 | 20 | IO_L14N_VREF_20 | L8 | NA | GND | AB14 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 5 | IO_L5N_5 | D17 | 20 | IO_L15P_20 | F11 | NA | GND | AM14 |
| 5 | IO_L6P_5 | E21 | 20 | IO_L15N_20 | E11 | NA | GND | E15 |
| 5 | IO_L6N_5 | D20 | 20 | IO_L16P_20 | M10 | NA | GND | K15 |
| 5 | IO_L7P_5 | D16 | 20 | IO_L16N_20 | L9 | NA | GND | R15 |
| 5 | IO_L7N_5 | D15 | 20 | IO_L17P_20 | E12 | NA | GND | U15 |
| 5 | IO_L8P_CC_5 | G20 | 20 | IO_L17N_20 | E13 | NA | GND | W15 |
| 5 | IO_L8N_CC_5 | F20 | 20 | IO_L18P_20 | N10 | NA | GND | AA15 |
| 5 | IO_L9P_CC_5 | D14 | 20 | IO_L18N_20 | N9 | NA | GND | AE15 |
| 5 | IO_L9N_CC_5 | E14 | 20 | IO_L19P_20 | F13 | NA | GND | H16 |
| 5 | IO_L10P_CC_5 | E17 | 20 | IO_L19N_20 | G13 | NA | GND | M16 |
| 5 | IO_L10N_CC_5 | E16 | 21 | IO_L0P_21 | AA25 | NA | GND | P16 |
| 5 | IO_L11P_CC_5 | F21 | 21 | IO_L0N_21 | AA26 | NA | GND | T16 |
| 5 | IO_L11N_CC_5 | G21 | 21 | IO_L1P_21 | AB27 | NA | GND | V16 |
| 5 | IO_L12P_VRN_5 | E18 | 21 | IO_L1N_21 | AC27 | NA | GND | Y16 |
| 5 | IO_L12N_VRP_5 | D19 | 21 | IO_L2P_21 | Y24 | NA | GND | AB16 |
| 5 | IO_L13P_5 | D21 | 21 | IO_L2N_21 | AA24 | NA | GND | AD16 |
| 5 | IO_L13N_5 | D22 | 21 | IO_L3P_21 | AB25 | NA | GND | AH16 |
| 5 | IO_L14P_5 | F18 | 21 | IO_L3N_21 | AB26 | NA | GND | A17 |
| 5 | IO_L14N_VREF_5 | G18 | 21 | IO_L4P_21 | AC28 | NA | GND | L17 |
| 5 | IO_L15P_5 | E22 | 21 | IO_L4N_VREF_21 | AD27 | NA | GND | N17 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 5 | IO_L15N_5 | F23 | 21 | IO_L5P_21 | AB28 | NA | GND | R17 |
| 5 | IO_L16P_5 | G17 | 21 | IO_L5N_21 | AA28 | NA | GND | AA17 |
| 5 | IO_L16N_5 | F16 | 21 | IO_L6P_21 | AG28 | NA | GND | AC17 |
| 5 | IO_L17P_5 | D24 | 21 | IO_L6N_21 | AH28 | NA | GND | AF17 |
| 5 | IO_L17N_5 | E23 | 21 | IO_L7P_21 | AE28 | NA | GND | AL17 |
| 5 | IO_L18P_5 | F14 | 21 | IO_L7N_21 | AF28 | NA | GND | D18 |
| 5 | IO_L18N_5 | F15 | 21 | IO_L8P_CC_21 | AK26 | NA | GND | J18 |
| 5 | IO_L19P_5 | F24 | 21 | IO_L8N_CC_21 | AJ27 | NA | GND | M18 |
| 5 | IO_L19N_5 | E24 | 21 | IO_L9P_CC_21 | AK29 | NA | GND | P18 |
| 6 | IO_L0P_6 | AH24 | 21 | IO_L9N_CC_21 | AJ29 | NA | GND | Y18 |
| 6 | IO_L0N_6 | AJ24 | 21 | IO_L10P_CC_21 | AK28 | NA | GND | AB18 |
| 6 | IO_L1P_6 | AK12 | 21 | IO_L10N_CC_21 | AK27 | NA | GND | AD18 |
| 6 | IO_L1N_6 | AJ12 | 21 | IO_L11P_CC_21 | AH27 | NA | GND | AP18 |
| 6 | IO_L2P_6 | AH23 | 21 | IO_L11N_CC_21 | AJ26 | NA | GND | G19 |
| 6 | IO_L2N_6 | AJ22 | 21 | IO_L12P_VRN_21 | AJ25 | NA | GND | N19 |
| 6 | IO_L3P_6 | AL13 | 21 | IO_L12N_VRP_21 | AH25 | NA | GND | R19 |
| 6 | IO_L3N_6 | AK13 | 21 | IO_L13P_21 | AF24 | NA | GND | U19 |
| 6 | IO_L4P_6 | AK24 | 21 | IO_L13N_21 | AG25 | NA | GND | W19 |
| 6 | IO_L4N_VREF_6 | AL23 | 21 | IO_L14P_21 | AG27 | NA | GND | AA19 |
| 6 | IO_L5P_6 | AJ14 | 21 | IO_L14N_VREF_21 | AG26 | NA | GND | AC19 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 6 | IO_L5N_6 | AK14 | 21 | IO_L15P_21 | AF25 | NA | GND | AG19 |
| 6 | IO_L6P_6 | AK23 | 21 | IO_L15N_21 | AF26 | NA | GND | K20 |
| 6 | IO_L6N_6 | AK22 | 21 | IO_L16P_21 | AE27 | NA | GND | M20 |
| 6 | IO_L7P_6 | AL15 | 21 | IO_L16N_21 | AE26 | NA | GND | P20 |
| 6 | IO_L7N_6 | AL14 | 21 | IO_L17P_21 | AC25 | NA | GND | T20 |
| 6 | IO_L8P_CC_6 | AJ21 | 21 | IO_L17N_21 | AC24 | NA | GND | V20 |
| 6 | IO_L8N_CC_6 | AJ20 | 21 | IO_L18P_21 | AD26 | NA | GND | Y20 |
| 6 | IO_L9P_CC_6 | AJ16 | 21 | IO_L18N_21 | AD25 | NA | GND | AB20 |
| 6 | IO_L9N_CC_6 | AJ15 | 21 | IO_L19P_21 | AD24 | NA | GND | AE20 |
| 6 | IO_L10P_CC_6 | AK16 | 21 | IO_L19N_21 | AE24 | NA | GND | AK20 |
| 6 | IO_L10N_CC_6 | AL16 | 22 | IO_L0P_22 | AN14 | NA | GND | C21 |
| 6 | IO_L11P_CC_6 | AL21 | 22 | IO_L0N_22 | AP14 | NA | GND | H21 |
| 6 | IO_L11N_CC_6 | AK21 | 22 | IO_L1P_22 | AB10 | NA | GND | N21 |
| 6 | IO_L12P_VRN_6 | AK17 | 22 | IO_L1N_22 | AA10 | NA | GND | R21 |
| 6 | IO_L12N_VRP_6 | AJ17 | 22 | IO_L2P_22 | AN13 | NA | GND | U21 |
| 6 | IO_L13P_6 | AL19 | 22 | IO_L2N_22 | AM13 | NA | GND | W21 |
| 6 | IO_L13N_6 | AL20 | 22 | IO_L3P_22 | AA8 | NA | GND | AA21 |
| 6 | IO_L14P_6 | AK18 | 22 | IO_L3N_22 | AA9 | NA | GND | AC21 |
| 6 | IO_L14N_VREF_6 | AL18 | 22 | IO_L4P_22 | AP12 | NA | GND | AN21 |
| 6 | IO_L15P_6 | AJ19 | 22 | IO_L4N_VREF_22 | AN12 | NA | GND | A22 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 6 | IO_L15N_6 | AK19 | 22 | IO_L5P_22 | AC8 | NA | GND | F22 |
| 6 | IO_L16P_6 | AM15 | 22 | IO_L5N_22 | AB8 | NA | GND | L22 |
| 6 | IO_L16N_6 | AM16 | 22 | IO_L6P_22 | AM12 | NA | GND | P22 |
| 6 | IO_L17P_6 | AP16 | 22 | IO_L6N_22 | AM11 | NA | GND | T22 |
| 6 | IO_L17N_6 | AP17 | 22 | IO_L7P_22 | AC10 | NA | GND | V22 |
| 6 | IO_L18P_6 | AN15 | 22 | IO_L7N_22 | AC9 | NA | GND | Y22 |
| 6 | IO_L18N_6 | AP15 | 22 | IO_L8P_CC_22 | AL11 | NA | GND | AB22 |
| 6 | IO_L19P_6 | AM17 | 22 | IO_L8N_CC_22 | AL10 | NA | GND | AF22 |
| 6 | IO_L19N_6 | AN17 | 22 | IO_L9P_CC_22 | AE8 | NA | GND | J23 |
| 11 | IO_L0P_11 | B32 | 22 | IO_L9N_CC_22 | AD9 | NA | GND | R23 |
| 11 | IO_L0N_11 | A33 | 22 | IO_L10P_CC_22 | AD10 | NA | GND | U23 |
| 11 | IO_L1P_11 | B33 | 22 | IO_L10N_CC_22 | AD11 | NA | GND | W23 |
| 11 | IO_L1N_11 | C33 | 22 | IO_L11P_CC_22 | AK11 | NA | GND | AA23 |
| 11 | IO_L2P_11 | C32 | 22 | IO_L11N_CC_22 | AJ11 | NA | GND | AJ23 |
| 11 | IO_L2N_11 | D32 | 22 | IO_L12P_VRN_22 | AF8 | NA | GND | AP23 |
| 11 | IO_L3P_11 | C34 | 22 | IO_L12N_VRP_22 | AE9 | NA | GND | B24 |
| 11 | IO_L3N_11 | D34 | 22 | IO_L13P_22 | AK8 | NA | GND | M24 |
| 11 | IO_L4P_11 | G32 | 22 | IO_L13N_22 | AK9 | NA | GND | AB24 |
| 11 | IO_L4N_VREF_11 | H32 | 22 | IO_L14P_22 | AF9 | NA | GND | AG24 |
| 11 | IO_L5P_11 | F33 | 22 | IO_L14N_VREF_22 | AF10 | NA | GND | AM24 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 11 | IO_L5N_11 | E34 | 22 | IO_L15P_22 | AJ9 | NA | GND | E25 |
| 11 | IO_L6P_11 | E32 | 22 | IO_L15N_22 | AJ10 | NA | GND | K25 |
| 11 | IO_L6N_11 | E33 | 22 | IO_L16P_22 | AF11 | NA | GND | R25 |
| 11 | IO_L7P_11 | G33 | 22 | IO_L16N_22 | AE11 | NA | GND | Y25 |
| 11 | IO_L7N_11 | F34 | 22 | IO_L17P_22 | AH9 | NA | GND | AE25 |
| 11 | IO_L8P_CC_11 | J32 | 22 | IO_L17N_22 | AH10 | NA | GND | H26 |
| 11 | IO_L8N_CC_11 | H33 | 22 | IO_L18P_22 | AG8 | NA | GND | N26 |
| 11 | IO_L9P_CC_11 | H34 | 22 | IO_L18N_22 | AH8 | NA | GND | V26 |
| 11 | IO_L9N_CC_11 | J34 | 22 | IO_L19P_22 | AG10 | NA | GND | AC26 |
| 11 | IO_L10P_CC_SM15P_11 | L34 | 22 | IO_L19N_22 | AG11 | NA | GND | AH26 |
| 11 | IO_L10N_CC_SM15N_11 | K34 | 23 | IO_L0P_23 | C20 | NA | GND | A27 |
| 11 | IO_L11P_CC_SM14P_11 | K33 | 23 | IO_L0N_23 | B20 | NA | GND | L27 |
| 11 | IO_L11N_CC_SM14N_11 | K32 | 23 | IO_L1P_23 | B21 | NA | GND | AA27 |
| 11 | IO_L12P_VRN_11 | N33 | 23 | IO_L1N_23 | A21 | NA | GND | AF27 |
| 11 | IO_L12N_VRP_11 | M33 | 23 | IO_L2P_23 | C19 | NA | GND | AL27 |
| 11 | IO_L13P_11 | L33 | 23 | IO_L2N_23 | C18 | NA | GND | D28 |
| 11 | IO_L13N_11 | M32 | 23 | IO_L3P_23 | C22 | NA | GND | P28 |
| 11 | IO_L14P_11 | P34 | 23 | IO_L3N_23 | B22 | NA | GND | AD28 |
| 11 | IO_L14N_VREF_11 | N34 | 23 | IO_L4P_23 | B18 | NA | GND | AP28 |
| 11 | IO_L15P_SM13P_11 | P32 | 23 | IO_L4N_VREF_23 | A18 | NA | GND | B29 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 11 | IO_L15N_SM13N_11 | N32 | 23 | IO_L5P_23 | C23 | NA | GND | G29 |
| 11 | IO_L16P_SM12P_11 | T33 | 23 | IO_L5N_23 | B23 | NA | GND | U29 |
| 11 | IO_L16N_SM12N_11 | R34 | 23 | IO_L6P_23 | A19 | NA | GND | AG29 |
| 11 | IO_L17P_SM11P_11 | R33 | 23 | IO_L6N_23 | A20 | NA | GND | K30 |
| 11 | IO_L17N_SM11N_11 | R32 | 23 | IO_L7P_23 | A23 | NA | GND | Y30 |
| 11 | IO_L18P_SM10P_11 | U33 | 23 | IO_L7N_23 | A24 | NA | GND | AK30 |
| 11 | IO_L18N_SM10N_11 | T34 | 23 | IO_L8P_CC_23 | C24 | NA | GND | C31 |
| 11 | IO_L19P_SM9P_11 | U32 | 23 | IO_L8N_CC_23 | D25 | NA | GND | N31 |
| 11 | IO_L19N_SM9N_11 | U31 | 23 | IO_L9P_CC_23 | B26 | NA | GND | AC31 |
| 12 | IO_L0P_12 | M6 | 23 | IO_L9N_CC_23 | A25 | NA | GND | AN31 |
| 12 | IO_L0N_12 | M5 | 23 | IO_L10P_CC_23 | B27 | NA | GND | A32 |
| 12 | IO_L1P_12 | N8 | 23 | IO_L10N_CC_23 | A26 | NA | GND | F32 |
| 12 | IO_L1N_12 | N7 | 23 | IO_L11P_CC_23 | B25 | NA | GND | T32 |
| 12 | IO_L2P_12 | M7 | 23 | IO_L11N_CC_23 | C25 | NA | GND | AF32 |
| 12 | IO_L2N_12 | L6 | 23 | IO_L12P_VRN_23 | C29 | NA | GND | D33 |
| 12 | IO_L3P_12 | N5 | 23 | IO_L12N_VRP_23 | B28 | NA | GND | J33 |
| 12 | IO_L3N_12 | P5 | 23 | IO_L13P_23 | D26 | NA | GND | W33 |
| 12 | IO_L4P_12 | L4 | 23 | IO_L13N_23 | C27 | NA | GND | AJ33 |
| 12 | IO_L4N_VREF_12 | L5 | 23 | IO_L14P_23 | A29 | NA | GND | AP33 |
| 12 | IO_L5P_12 | P7 | 23 | IO_L14N_VREF_23 | A28 | NA | GND | B34 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 12 | IO_L5N_12 | P6 | 23 | IO_L15P_23 | C28 | NA | GND | G34 |
| 12 | IO_L6P_12 | K7 | 23 | IO_L15N_23 | D27 | NA | GND | M34 |
| 12 | IO_L6N_12 | K6 | 23 | IO_L16P_23 | B31 | NA | GND | U34 |
| 12 | IO_L7P_12 | R6 | 23 | IO_L16N_23 | A31 | NA | GND | AB34 |
| 12 | IO_L7N_12 | T6 | 23 | IO_L17P_23 | C30 | NA | GND | AG34 |
| 12 | IO_L8P_CC_12 | J6 | 23 | IO_L17N_23 | D29 | NA | GND | AM34 |
| 12 | IO_L8N_CC_12 | J5 | 23 | IO_L18P_23 | D31 | NA | VCCAUX | M11 |
| 12 | IO_L9P_CC_12 | R7 | 23 | IO_L18N_23 | D30 | NA | VCCAUX | P11 |
| 12 | IO_L9N_CC_12 | R8 | 23 | IO_L19P_23 | A30 | NA | VCCAUX | V11 |
| 12 | IO_L10P_CC_12 | T8 | 23 | IO_L19N_23 | B30 | NA | VCCAUX | AB11 |
| 12 | IO_L10N_CC_12 | U7 | 25 | IO_L0P_25 | AL29 | NA | VCCAUX | L12 |
| 12 | IO_L11P_CC_12 | H7 | 25 | IO_L0N_25 | AL30 | NA | VCCAUX | AC12 |
| 12 | IO_L11N_CC_12 | J7 | 25 | IO_L1P_25 | AM31 | NA | VCCAUX | M21 |
| 12 | IO_L12P_VRN_12 | R9 | 25 | IO_L1N_25 | AL31 | NA | VCCAUX | P23 |
| 12 | IO_L12N_VRP_12 | P9 | 25 | IO_L2P_25 | AN30 | NA | VCCAUX | T23 |
| 12 | IO_L13P_12 | H5 | 25 | IO_L2N_25 | AM30 | NA | VCCAUX | V23 |
| 12 | IO_L13N_12 | G5 | 25 | IO_L3P_25 | AP30 | NA | VCCAUX | Y23 |
| 12 | IO_L14P_12 | R11 | 25 | IO_L3N_25 | AP31 | NA | VCCAUX | U24 |
| 12 | IO_L14N_VREF_12 | P10 | 25 | IO_L4P_25 | AM27 | NA | VCCINT | N12 |
| 12 | IO_L15P_12 | F5 | 25 | IO_L4N_VREF_25 | AL28 | NA | VCCINT | R12 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 12 | IO_L15N_12 | F6 | 25 | IO_L5P_25 | AP29 | NA | VCCINT | U12 |
| 12 | IO_L16P_12 | T10 | 25 | IO_L5N_25 | AN29 | NA | VCCINT | W12 |
| 12 | IO_L16N_12 | T11 | 25 | IO_L6P_25 | AP27 | NA | VCCINT | AA12 |
| 12 | IO_L17P_12 | G6 | 25 | IO_L6N_25 | AN27 | NA | VCCINT | M13 |
| 12 | IO_L17N_12 | G7 | 25 | IO_L7P_25 | AN28 | NA | VCCINT | P13 |
| 12 | IO_L18P_12 | T9 | 25 | IO_L7N_25 | AM28 | NA | VCCINT | T13 |
| 12 | IO_L18N_12 | U10 | 25 | IO_L8P_CC_25 | AN25 | NA | VCCINT | V13 |
| 12 | IO_L19P_12 | E6 | 25 | IO_L8N_CC_25 | AM25 | NA | VCCINT | Y13 |
| 12 | IO_L19N_12 | E7 | 25 | IO_L9P_CC_25 | AM26 | NA | VCCINT | AB13 |
| 13 | IO_L0P_SM8P_13 | V32 | 25 | IO_L9N_CC_25 | AL26 | NA | VCCINT | AD13 |
| 13 | IO_L0N_SM8N_13 | V33 | 25 | IO_L10P_CC_25 | AP26 | NA | VCCINT | R14 |
| 13 | IO_L1P_SM7P_13 | W34 | 25 | IO_L10N_CC_25 | AP25 | NA | VCCINT | U14 |
| 13 | IO_L1N_SM7N_13 | V34 | 25 | IO_L11P_CC_25 | AL25 | NA | VCCINT | W14 |
| 13 | IO_L2P_SM6P_13 | Y33 | 25 | IO_L11N_CC_25 | AL24 | NA | VCCINT | AA14 |
| 13 | IO_L2N_SM6N_13 | AA33 | 25 | IO_L12P_VRN_25 | AN24 | NA | VCCINT | T15 |
| 13 | IO_L3P_SM5P_13 | AA34 | 25 | IO_L12N_VRP_25 | AP24 | NA | VCCINT | V15 |
| 13 | IO_L3N_SM5N_13 | Y34 | 25 | IO_L13P_25 | AM21 | NA | VCCINT | Y15 |
| 13 | IO_L4P_13 | Y32 | 25 | IO_L13N_25 | AM20 | NA | VCCINT | N16 |
| 13 | IO_L4N_VREF_13 | W32 | 25 | IO_L14P_25 | AN23 | NA | VCCINT | R16 |
| 13 | IO_L5P_SM4P_13 | AC34 | 25 | IO_L14N_VREF_25 | AM23 | NA | VCCINT | U16 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 13 | IO_L5N_SM4N_13 | AD34 | 25 | IO_L15P_25 | AN20 | NA | VCCINT | W16 |
| 13 | IO_L6P_SM3P_13 | AC32 | 25 | IO_L15N_25 | AP20 | NA | VCCINT | AA16 |
| 13 | IO_L6N_SM3N_13 | AB32 | 25 | IO_L16P_25 | AN22 | NA | VCCINT | AC16 |
| 13 | IO_L7P_SM2P_13 | AC33 | 25 | IO_L16N_25 | AM22 | NA | VCCINT | M17 |
| 13 | IO_L7N_SM2N_13 | AB33 | 25 | IO_L17P_25 | AN18 | NA | VCCINT | P17 |
| 13 | IO_L8P_CC_SM1P_13 | AF33 | 25 | IO_L17N_25 | AM18 | NA | VCCINT | Y17 |
| 13 | IO_L8N_CC_SM1N_13 | AE33 | 25 | IO_L18P_25 | AP22 | NA | VCCINT | AB17 |
| 13 | IO_L9P_CC_SM0P_13 | AF34 | 25 | IO_L18N_25 | AP21 | NA | VCCINT | AD17 |
| 13 | IO_L9N_CC_SM0N_13 | AE34 | 25 | IO_L19P_25 | AN19 | NA | VCCINT | N18 |
| 13 | IO_L10P_CC_13 | AH34 | 25 | IO_L19N_25 | AP19 | NA | VCCINT | R18 |
| 13 | IO_L10N_CC_13 | AJ34 | NA | MGTTXP0_112 | M2 | NA | VCCINT | AA18 |
| 13 | IO_L11P_CC_13 | AD32 | NA | MGTAVTTTX_112 | M3 | NA | VCCINT | AC18 |
| 13 | IO_L11N_CC_13 | AE32 | NA | MGTTXN0_112 | N2 | NA | VCCINT | M19 |
| 13 | IO_L12P_VRN_13 | AG33 | NA | MGTRXP0_112 | N1 | NA | VCCINT | P19 |
| 13 | IO_L12N_VRP_13 | AH33 | NA | MGTAVTTRX_112 | N3 | NA | VCCINT | T19 |
| 13 | IO_L13P_13 | AK34 | NA | MGTRXN0_112 | P1 | NA | VCCINT | V19 |
| 13 | IO_L13N_13 | AK33 | NA | MGTAVCCPLL_112 | T3 | NA | VCCINT | Y19 |
| 13 | IO_L14P_13 | AG32 | NA | MGTRXN1_112 | R1 | NA | VCCINT | AB19 |
| 13 | IO_L14N_VREF_13 | AH32 | NA | MGTREFCLKN_112 | P3 | NA | VCCINT | N20 |
| 13 | IO_L15P_13 | AJ32 | NA | MGTRXP1_112 | T1 | NA | VCCINT | R20 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 13 | IO_L15N_13 | AK32 | NA | MGTREFCLKP_112 | P4 | NA | VCCINT | U20 |
| 13 | IO_L16P_13 | AL34 | NA | MGTTXN1_112 | T2 | NA | VCCINT | W20 |
| 13 | IO_L16N_13 | AL33 | NA | MGTAVTTTX_112 | U3 | NA | VCCINT | AA20 |
| 13 | IO_L17P_13 | AM33 | NA | MGTTXP1_112 | U2 | NA | VCCINT | AC20 |
| 13 | IO_L17N_13 | AM32 | NA | MGTAVTTRXC | V5 | NA | VCCINT | P21 |
| 13 | IO_L18P_13 | AN34 | NA | MGTRREF_112 | V4 | NA | VCCINT | T21 |
| 13 | IO_L18N_13 | AN33 | NC | NC | U5 | NA | VCCINT | V21 |
| 13 | IO_L19P_13 | AN32 | NA | MGTTXP0_114 | V2 | NA | VCCINT | Y21 |
| 13 | IO_L19N_13 | AP32 | NA | MGTAVTTTX_114 | AC3 | NA | VCCINT | AB21 |
| 15 | IO_L0P_15 | E29 | NA | MGTTXN0_114 | W2 | NA | VCCINT | R22 |
| 15 | IO_L0N_15 | F29 | NA | MGTRXP0_114 | W1 | NA | VCCINT | U22 |
| 15 | IO_L1P_15 | G30 | NA | MGTAVTTRX_114 | W3 | NA | VCCINT | W22 |
| 15 | IO_L1N_15 | F30 | NA | MGTRXN0_114 | Y1 | 0 | VCCO_0 | AA22 |
| 15 | IO_L2P_15 | H29 | NA | MGTAVCCPLL_114 | AB3 | 0 | VCCO_0 | AD23 |
| 15 | IO_L2N_15 | J29 | NA | MGTRXN1_114 | AA1 | 1 | VCCO_1 | D13 |
| 15 | IO_L3P_15 | F31 | NA | MGTREFCLKN_114 | Y3 | 1 | VCCO_1 | G14 |
| 15 | IO_L3N_15 | E31 | NA | MGTRXP1_114 | AB1 | 2 | VCCO_2 | AM19 |
| 15 | IO_L4P_15 | L29 | NA | MGTREFCLKP_114 | Y4 | 2 | VCCO_2 | AH21 |
| 15 | IO_L4N_VREF_15 | K29 | NA | MGTTXN1_114 | AB2 | 3 | VCCO_3 | E20 |
| 15 | IO_L5P_15 | H30 | NA | MGTAVTTTX_114 | V3 | 3 | VCCO_3 | D23 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 15 | IO_L5N_15 | G31 | NA | MGTTXP1_114 | AC2 | 4 | VCCO_4 | AL12 |
| 15 | IO_L6P_15 | J30 | NA | MGTTXP0_116 | F2 | 4 | VCCO_4 | AG14 |
| 15 | IO_L6N_15 | J31 | NA | MGTAVTTTX_116 | F3 | 5 | VCCO_5 | C16 |
| 15 | IO_L7P_15 | L30 | NA | MGTTXN0_116 | G2 | 5 | VCCO_5 | F17 |
| 15 | IO_L7N_15 | M30 | NA | MGTRXP0_116 | G1 | 5 | VCCO_5 | B19 |
| 15 | IO_L8P_CC_15 | N29 | NA | MGTAVTTRX_116 | G3 | 6 | VCCO_6 | AK15 |
| 15 | IO_L8N_CC_15 | P29 | NA | MGTRXN0_116 | H1 | 6 | VCCO_6 | AN16 |
| 15 | IO_L9P_CC_15 | K31 | NA | MGTAVCCPLL_116 | K3 | 6 | VCCO_6 | AJ18 |
| 15 | IO_L9N_CC_15 | L31 | NA | MGTRXN1_116 | J1 | 11 | VCCO_11 | T27 |
| 15 | IO_L10P_CC_15 | P31 | NA | MGTREFCLKN_116 | H3 | 11 | VCCO_11 | R30 |
| 15 | IO_L10N_CC_15 | P30 | NA | MGTRXP1_116 | K1 | 11 | VCCO_11 | V31 |
| 15 | IO_L11P_CC_15 | M31 | NA | MGTREFCLKP_116 | H4 | 12 | VCCO_12 | N6 |
| 15 | IO_L11N_CC_15 | N30 | NA | MGTTXN1_116 | K2 | 12 | VCCO_12 | T7 |
| 15 | IO_L12P_VRN_15 | R28 | NA | MGTAVTTTX_116 | L3 | 12 | VCCO_12 | M9 |
| 15 | IO_L12N_VRP_15 | R29 | NA | MGTTXP1_116 | L2 | 13 | VCCO_13 | W28 |
| 15 | IO_L13P_15 | T31 | NA | MGTTXP0_118 | AD2 | 13 | VCCO_13 | AB29 |
| 15 | IO_L13N_15 | R31 | NA | MGTAVTTTX_118 | AD3 | 13 | VCCO_13 | AA32 |
| 15 | IO_L14P_15 | U30 | NA | MGTTXN0_118 | AE2 | 15 | VCCO_15 | M29 |
| 15 | IO_L14N_VREF_15 | T30 | NA | MGTRXP0_118 | AE1 | 15 | VCCO_15 | L32 |
| 15 | IO_L15P_15 | T28 | NA | MGTAVTTRX_118 | AE3 | 15 | VCCO_15 | P33 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 15 | IO_L15N_15 | T29 | NA | MGTRXN0_118 | AF1 | 17 | VCCO_17 | AE30 |
| 15 | IO_L16P_15 | U27 | NA | MGTAVCCPLL_118 | AH3 | 17 | VCCO_17 | AH31 |
| 15 | IO_L16N_15 | U28 | NA | MGTRXN1_118 | AG1 | 17 | VCCO_17 | AD33 |
| 15 | IO_L17P_15 | R26 | NA | MGTREFCLKN_118 | AF3 | 18 | VCCO_18 | AC6 |
| 15 | IO_L17N_15 | R27 | NA | MGTRXP1_118 | AH1 | 18 | VCCO_18 | W8 |
| 15 | IO_L18P_15 | U26 | NA | MGTREFCLKP_118 | AF4 | 18 | VCCO_18 | AB9 |
| 15 | IO_L18N_15 | T26 | NA | MGTTXN1_118 | AH2 | 19 | VCCO_19 | J28 |
| 15 | IO_L19P_15 | U25 | NA | MGTAVTTTX_118 | AJ3 | 19 | VCCO_19 | E30 |
| 15 | IO_L19N_15 | T25 | NA | MGTTXP1_118 | AJ2 | 19 | VCCO_19 | H31 |
| 17 | IO_L0P_17 | W24 | NA | MGTTXP0_120 | B4 | 20 | VCCO_20 | J8 |
| 17 | IO_L0N_17 | V24 | NA | MGTAVTTTX_120 | C4 | 20 | VCCO_20 | E10 |
| 17 | IO_L1P_17 | Y26 | NA | MGTTXN0_120 | B3 | 20 | VCCO_20 | H11 |
| 17 | IO_L1N_17 | W26 | NA | MGTRXP0_120 | A3 | 21 | VCCO_21 | AJ28 |
| 17 | IO_L2P_17 | V25 | NA | MGTAVTTRX_120 | C3 | 21 | VCCO_21 | AM29 |
| 17 | IO_L2N_17 | W25 | NA | MGTRXN0_120 | A2 | 21 | VCCO_21 | AL32 |
| 17 | IO_L3P_17 | Y27 | NA | MGTAVCCPLL_120 | D3 | 22 | VCCO_22 | AF7 |
| 17 | IO_L3N_17 | W27 | NA | MGTRXN1_120 | C1 | 22 | VCCO_22 | AJ8 |
| 17 | IO_L4P_17 | V30 | NA | MGTREFCLKN_120 | D4 | 22 | VCCO_22 | AH11 |
| 17 | IO_L4N_VREF_17 | W30 | NA | MGTRXP1_120 | D1 | 23 | VCCO_23 | G24 |
| 17 | IO_L5P_17 | V28 | NA | MGTREFCLKP_120 | E4 | 23 | VCCO_23 | C26 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 17 | IO_L5N_17 | V27 | NA | MGTTXN1_120 | D2 | 23 | VCCO_23 | F27 |
| 17 | IO_L6P_17 | W31 | NA | MGTAVTTTX_120 | E3 | 25 | VCCO_25 | AL22 |
| 17 | IO_L6N_17 | Y31 | NA | MGTTXP1_120 | E2 | 25 | VCCO_25 | AK25 |
| 17 | IO_L7P_17 | W29 | NA | MGTTXP0_122 | AK2 | 25 | VCCO_25 | AN26 |
| 17 | IO_L7N_17 | V29 | NA | MGTAVTTTX_122 | AK3 | NA | MGTAVCC_112 | R3 |
| 17 | IO_L8P_CC_17 | Y28 | NA | MGTTXN0_122 | AL2 | NA | MGTAVCC_112 | R4 |
| 17 | IO_L8N_CC_17 | Y29 | NA | MGTRXP0_122 | AL1 | NA | MGTAVCC_114 | AA3 |
| 17 | IO_L9P_CC_17 | AB31 | NA | MGTAVTTRX_122 | AL3 | NA | MGTAVCC_114 | AA4 |
| 17 | IO_L9N_CC_17 | AA31 | NA | MGTRXN0_122 | AM1 | NA | MGTAVCC_116 | J3 |
| 17 | IO_L10P_CC_17 | AB30 | NA | MGTAVCCPLL_122 | AM4 | NA | MGTAVCC_116 | J4 |
| 17 | IO_L10N_CC_17 | AC30 | NA | MGTRXN1_122 | AP2 | NA | MGTAVCC_118 | AG3 |
| 17 | IO_L11P_CC_17 | AA29 | NA | MGTREFCLKN_122 | AL4 | NA | MGTAVCC_118 | AG4 |
| 17 | IO_L11N_CC_17 | AA30 | NA | MGTRXP1_122 | AP3 | NA | MGTAVCC_120 | D5 |
| 17 | IO_L12P_VRN_17 | AD31 | NA | MGTREFCLKP_122 | AL5 | NA | MGTAVCC_120 | F4 |
| 17 | IO_L12N_VRP_17 | AE31 | NA | MGTTXN1_122 | AN3 | NA | MGTAVCC_122 | AJ4 |
| 17 | IO_L13P_17 | AD30 | NA | MGTAVTTTX_122 | AM3 | NA | MGTAVCC_122 | AK5 |
| 17 | IO_L13N_17 | AC29 | NA | MGTTXP1_122 | AN4 | NA | MGTAVCC_124 | C7 |
| 17 | IO_L14P_17 | AF31 | NA | MGTTXP0_124 | B10 | NA | MGTAVCC_124 | D7 |
| 17 | IO_L14N_VREF_17 | AG31 | NA | MGTAVTTTX_124 | C10 | NA | MGTAVCC_126 | AL8 |
| 17 | IO_L15P_17 | AE29 | NA | MGTTXN0_124 | B9 | NA | MGTAVCC_126 | AM8 |

| Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number | Bank | Pin Description | Pin Number |
|---|---|---|---|---|---|---|---|---|
| 17 | IO_L15N_17 | AD29 | | | | NA | FLOAT | U4 |

Notes:

1. Do not connect a single-ended clock to the N-side of the differential clock pair of pins, for example, IO_L3N_GC_3.
2. Do not connect a single-ended clock to the N-side of clock capable pins, for example, IO_L8N_CC_11.
3. RSVD pins must be tied to GND (logic 0).

# Revision History

The following table shows the revision history for this document

| Date | Version | Revision |
|---|---|---|
| 10/09/2018 | V1.1 | Initial release |
| | | |
| | | |
| | | |

## Service & Supply

ADDRESS: No.2. Siyingmen N.Rd. Donggaodi Fengtai District,BeiJing,PRC
DEPARTMENT: International Cooperation Department
TELEPHONE: 86-010-67968115
FAX: 86-010-68757706
POST CODE: 100076