BQ79712B-Q1 Functional Safety-Compliant Automotive Battery Monitors

1 Features

- AEC-Q100 qualified with –40°C to +125°C ambient temperature range
- Functional Safety Compliant
  - Documentation to aid ISO 26262 system design
  - Systematic capability up to ASIL D
  - Hardware capability up to ASIL D
- Measure from 9 to 12 cells in series per device, stackable up to 64 devices
- Dedicated ADC per cell
- Cell voltage and battery pack current measurement synchronized to 64us
- Support limp home mode with full redundancy
- Integrated post-ADC configurable digital low-pass filters
- Supports bus bar without affecting measurement accuracy
- 7 GPIOs for temp sensor/analog/digital/I^2C controller/SPI controller
- Internal cell balancing
  - Balancing at 200mA (BQ79712SB); 400mA (BQ79712PB)
  - User controlled PWM adjusted balancing current
  - Built-in balancing thermal management with automatic pause and resume control
- Robust daisy chain communication and support for ring architecture
- Hardware reset by host simulates POR-like event without battery removal
- Support transformer and capacitive isolation
- On chip memory for one time custom programming
- Shutdown current 6uA
- Compatible with BQ79600-Q1 with SPI/UART interface

2 Applications

- Battery Management System (BMS) in hybrid and electric powertrain systems
- Energy storage battery packs with Battery Management Systems

3 Description

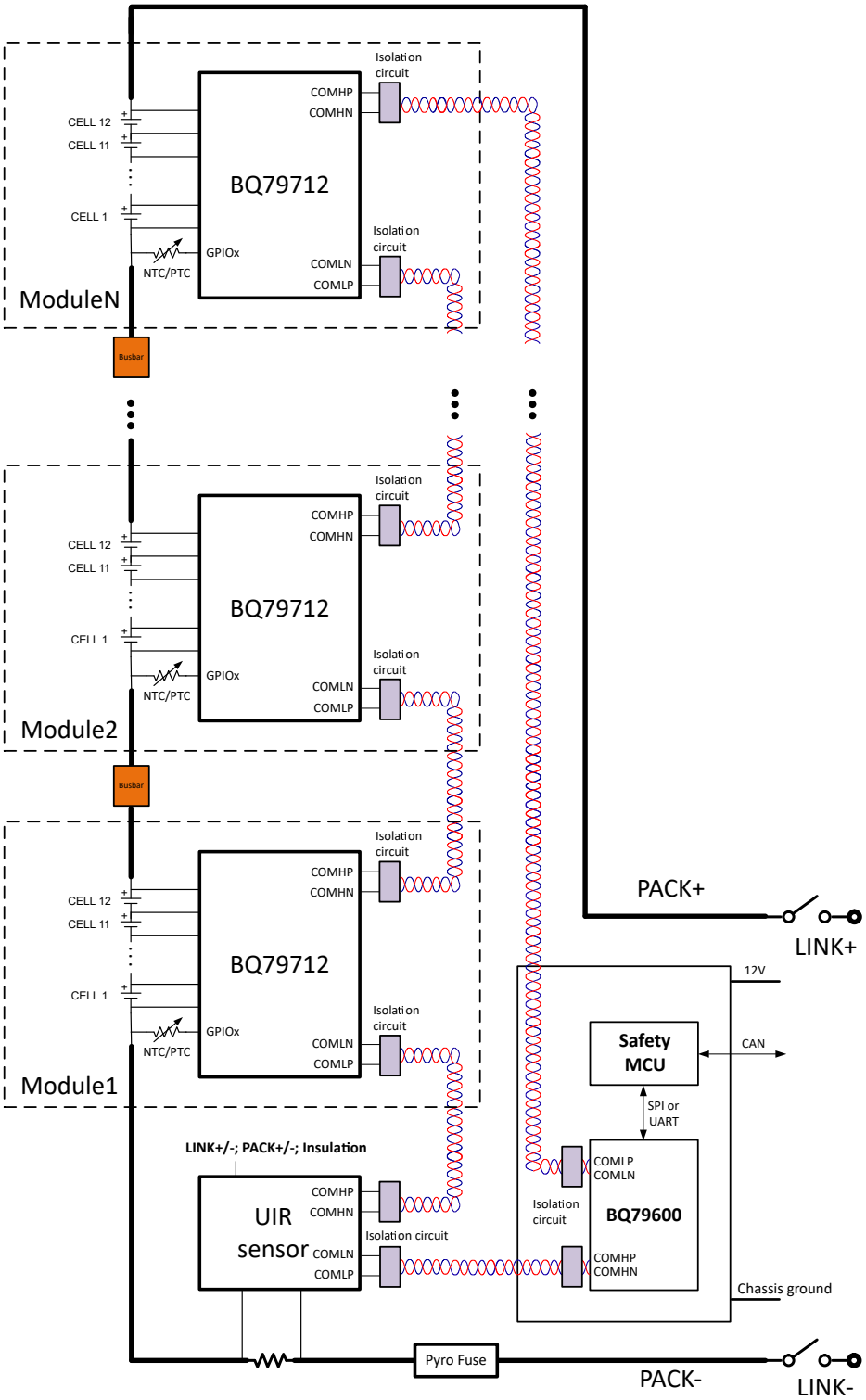
The BQ79712SB-Q1 and BQ79712PB-Q1 provide high-accuracy cell voltage measurements for 12S battery modules in high-voltage battery management systems in xEV/EV. The BQ797xx-Q1 family of monitors offers different channel options and supports high reuse of the established software and hardware across any platform. This device has advanced ADC architecture and measurement systems, meeting stringent automotive standards and safety requirements. With the daisy chain isolated by transformer (or capacitor), the device is designed for centralized or distributed architectures in xEV powertrain.

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
BQ79712PB-Q1	HTQFP (48)	7.00mm × 7.00mm
BQ79712SB-Q1		

(1) Any mention of BQ79712, BQ79712P and BQ79712S in diagrams in this data sheet refer to BQ79712B, BQ79712PB and BQ79712SB respectively.
(2) For all available packages, see the orderable addendum at the end of the data sheet.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.



Simplified System Diagram

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4 Device Comparison Table

DEVICE	STATUS	DESCRIPTION
BQ79712PB-Q1	Active	12S, 7 GPIOs, integrated DCDC
BQ79712SB-Q1	Active	12S, 7 GPIOs, integrated LDO FET

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5 Device and Documentation Support

5.1 Device Support

5.1.1 Third-Party Products Disclaimer

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5.2 Documentation Support

5.2.1 Related Documentation

5.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.5 Trademarks

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5.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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6.1 Package Option Addendum

Packaging Information

Orderable Device(1)	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(5)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4)
BQ79712PBQPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NiPdAu	MSL-3-260C-168 HR	-40 to 125C	BQ79712PBQ
BQ79712SBQPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NiPdAu	MSL-3-260C-168 HR	-40 to 125C	BQ79712SBQ

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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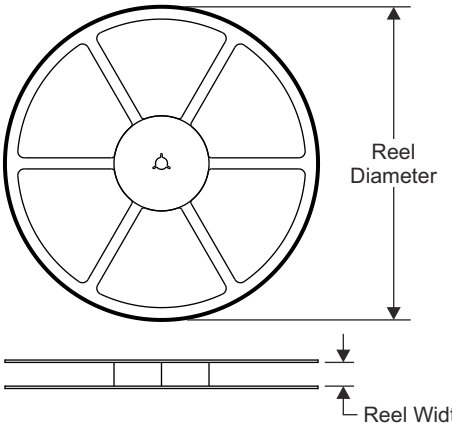
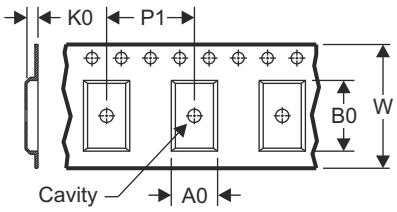
6.2 Tape and Reel Information

REEL DIMENSIONS

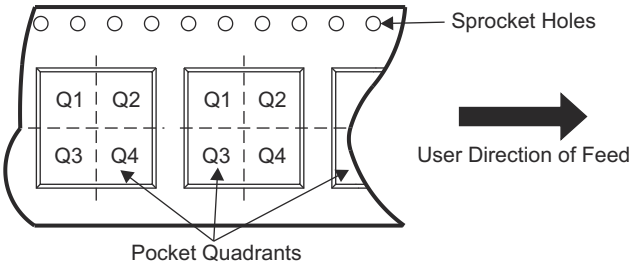


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ79712PBQPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
BQ79712SBQPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

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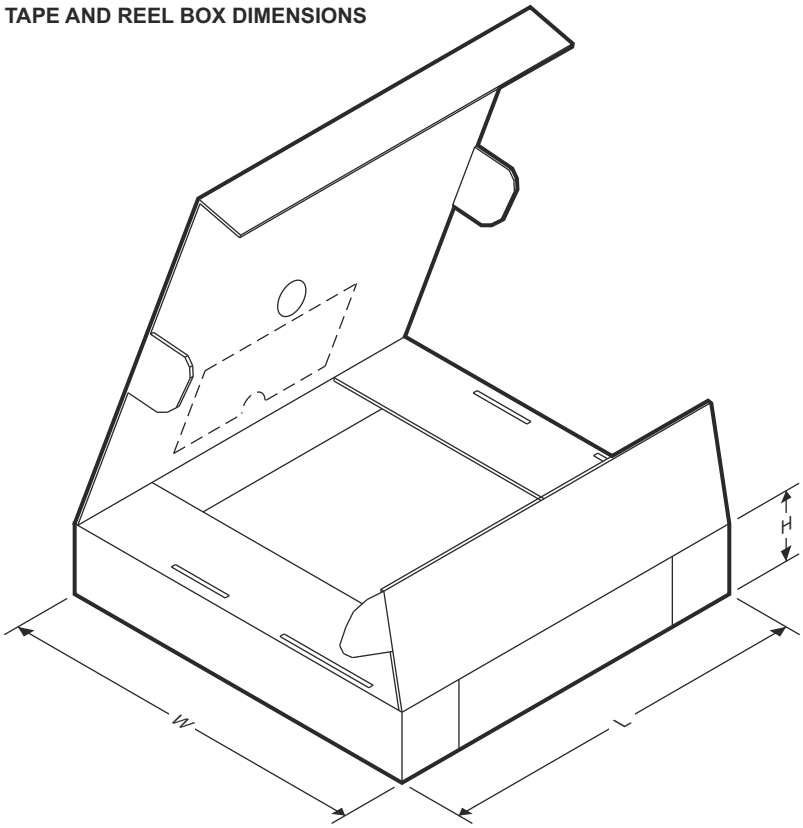
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ79712PBQPHPRQ1	HTQFP	PHP	48	1000	336.6	336.6	31.8
BQ79712SBQPHPRQ1	HTQFP	PHP	48	1000	336.6	336.6	31.8

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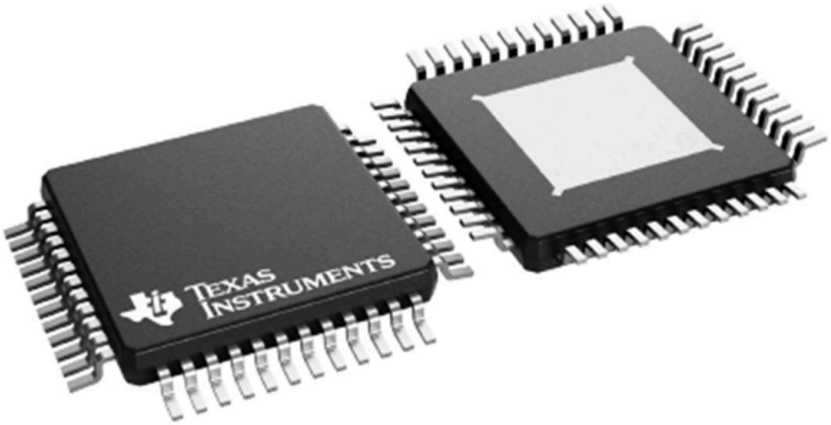
6.3 Mechanical Data

PHP 48 **TQFP - 1.2 mm max height**

7 x 7, 0.5 mm pitch QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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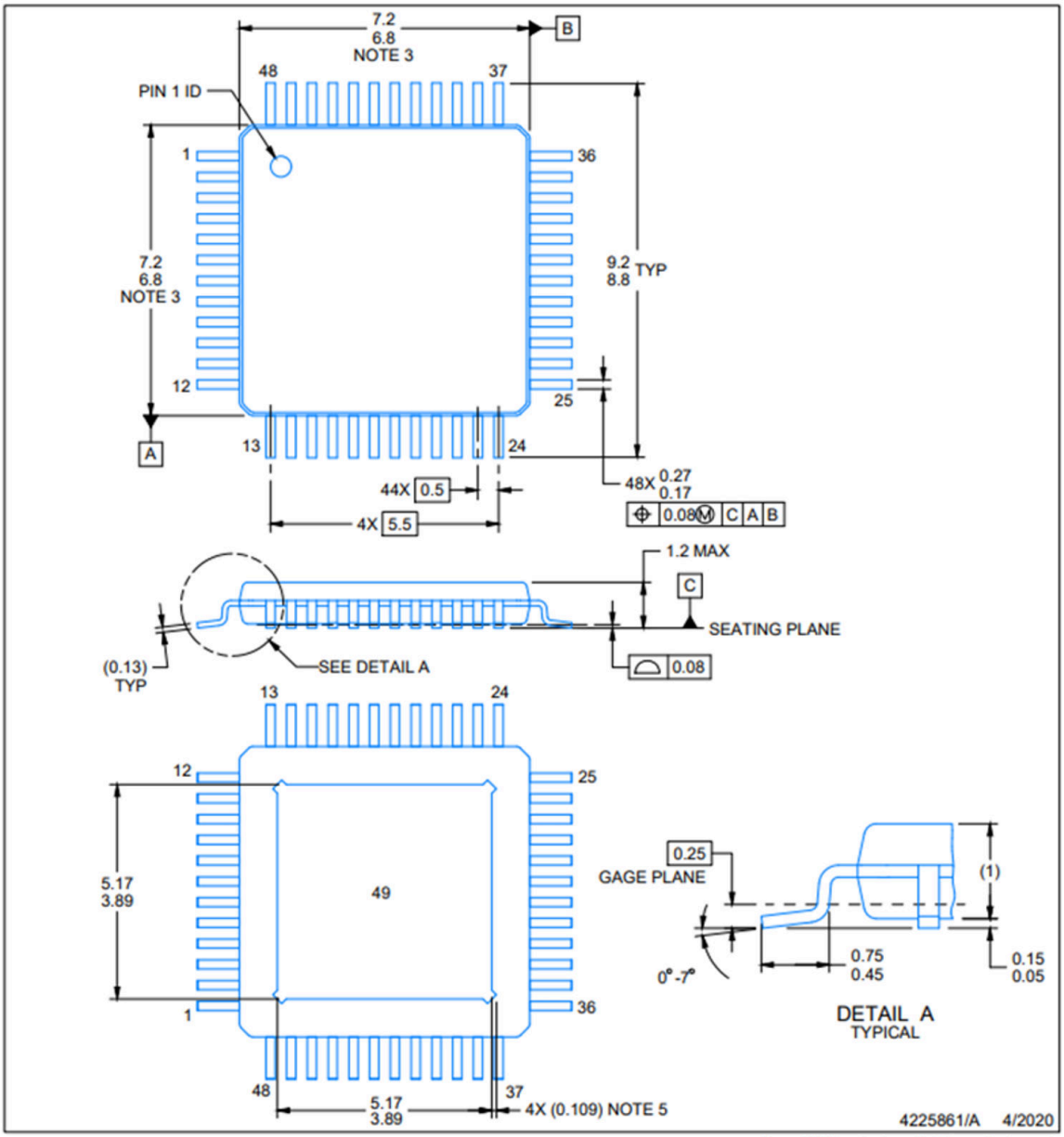
PACKAGE OUTLINE

PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

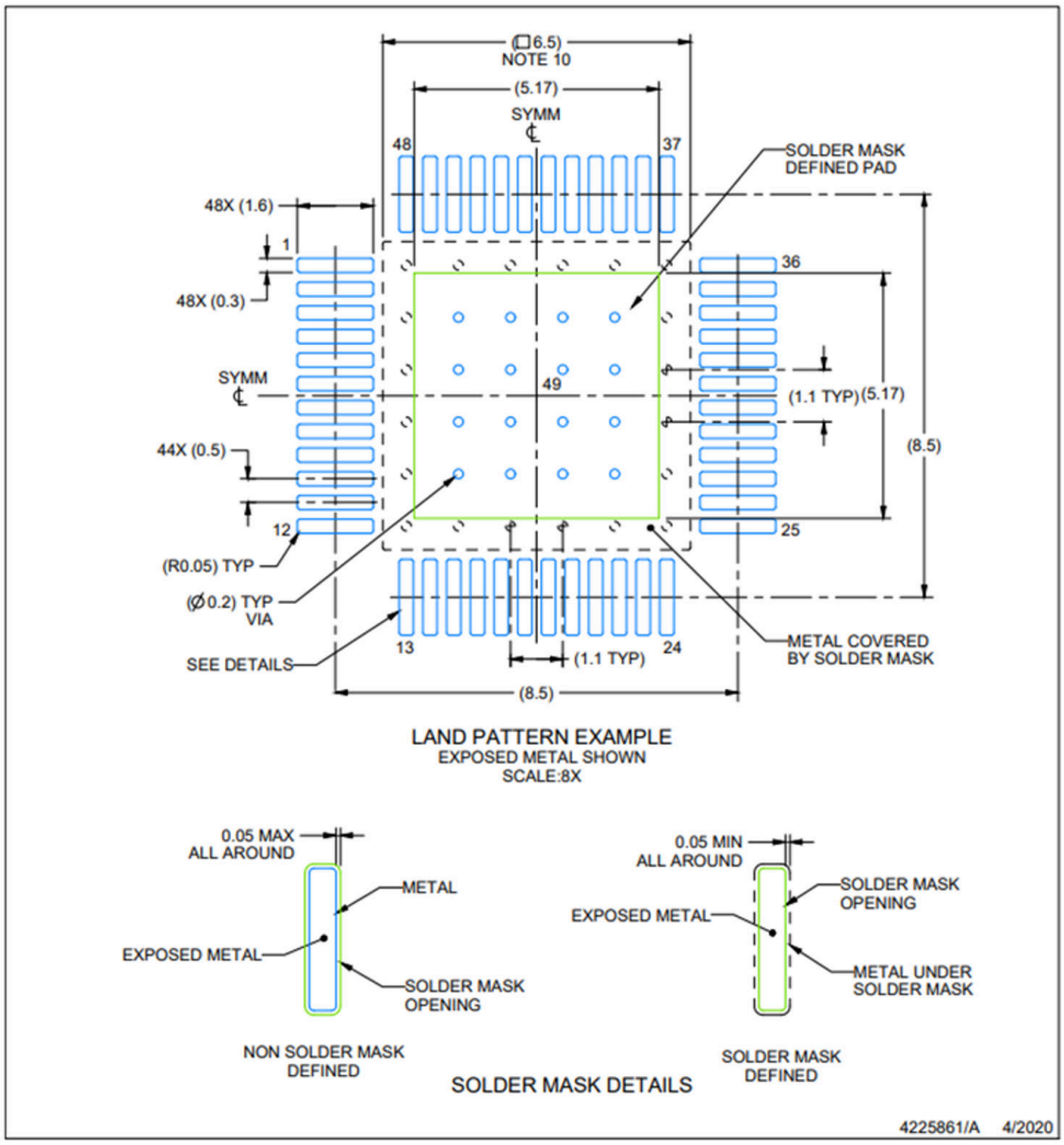
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

EXAMPLE BOARD LAYOUT

PHP0048G — **PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

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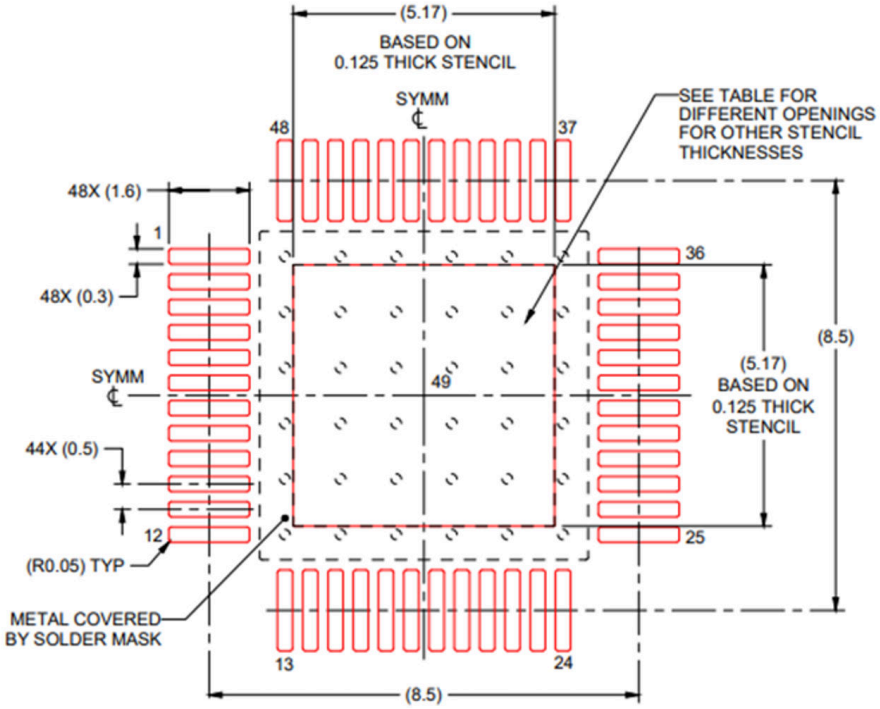
EXAMPLE STENCIL DESIGN

PHP0048G **PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

4225861/A 4/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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