Ver 1.1

BQR2V Series FPGA

Datasheet

Part Number：BQR2V3000

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Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2017.1		Initial release.	
1.1	2018.3		Update format	

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1. Features

- 0.13 µm 8-layer epitaxial process
- Certified to CAST C
- Guaranteed over the full military temperature range(–55℃ to +125℃)
- Radiation hardened FPGAs for space and satellite Applications
- Guaranteed total ionizing dose to 100K Rad(si)
- Latch-up immune to LET = 75 MeV cm^2/mg
- IP-Immersion Architecture
  - Densities 3M system gates
  - 300+ MHz internal clock speed (Advance Data)
  - 622+ Mb/s I/O(Advance Data)
- SelectRAMTM Memory Hierarchy
  - 1.728Mb of dual-port RAM in 18 Kbit block SelectRAM resources
  - 0.448 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
  - SRAM interfaces
    - SDR/DDR SRAM
    - QDR SRAM
  - CAM interfaces
- Arithmetic Functions
  - Dedicated 18-bit×18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 28672 internal registers/latches with Clock Enable
  - Up to 28672 look-up tables (LUTs) or cascadable 16-bit shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and sum-of-products support
  - Internal 3-state busing
- High-Performance Clock Management Circuitry
  - Up to 12 DCM (Digital Clock Manager) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers
- Active Interconnect Technology
  - Fourth generation segmented routing structure
  - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
  - Up to 516 user I/Os

- ✧ 19 single-ended and six differential standards
- ✧ Programmable sink current (2 mA to 24 mA) per I/O
- ✧ Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
- ✧ Differential Signaling
  - 622 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
  - Bus LVDS I/O
  - Lightning Data Transport (LDT) I/O with current driver buffers
  - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
  - Built-in DDR input and output registers
- ✧ Proprietary high-performance SelectLink Technology
  - High-bandwidth data path
  - Double Data Rate (DDR) link
  - Web-based HDL generation methodology
- Supported by Xilinx ISE Development Systems
- SRAM-Based In-System Configuration
  - ✧ Fast SelectMAP configuration
  - ✧ IEEE 1532 support
  - ✧ Partial reconfiguration
  - ✧ Unlimited reprogrammability
  - ✧ Readback capability
- 1.5V (V_{CCINT}) Core Power Supply, Dedicated 3.3V V_{CCAUX} Auxiliary and V_{CCO} I/O Power Supplies IEEE 1149.1 Compatible Boundary-Scan Logic Support

2. General Description

The BQR2V3000 is developed for high performance, high-density, aerospace designs that are based on IP cores and customized modules. The device delivers complete solutions for telecommunication, networking, video, and DSP applications, including PCI, LVDS, and DDR interfaces.

The 0.13 μm CMOS 8-layer metal process and the BQR2V3000 architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a high densities of 1 million system gates, the BQR2V3000 enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays and other one-time-programmable device. As shown in 错误！未找到引用源。, the BQR2V3000 comprises CLB，Multiplier Blocks，SelectRAM Blocks，DCMs and IOBs.

Table 1: BQR2V3000-CCGA717 Field-Programmable Gate Array

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads
		Array Row xCol.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)		
BQR2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	516

3. Architecture

3.1 Overview

BQR2V3000 device are user-programmable gate arrays with various configurable elements.The BQR2V3000 architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

The internal configurable logic includes four major elements organized in a regular array:

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit×18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

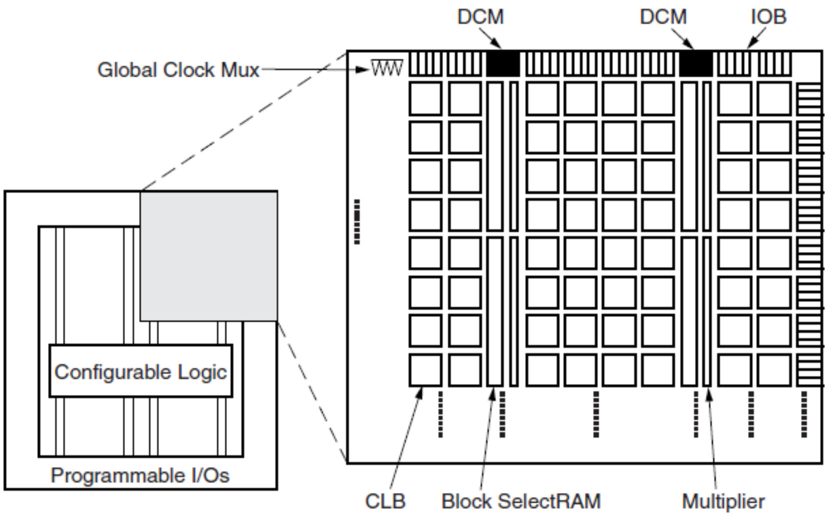


Figure 1 BQR2V3000 Architecture Overview

3.2 Features

This section briefly describes BQR2V3000 features.

3.2.1 Input/Output Blocks (IOBs)

BQR2V3000 I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as an input and/or an output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in Figure 2.

Note: Differential I/Os must use the same clock.

IOB blocks are designed for high-performance I/Os,supporting 19 single-ended standards, as well as differential signaling with LVDS, LDT, Bus LVDS, and LVPECL.

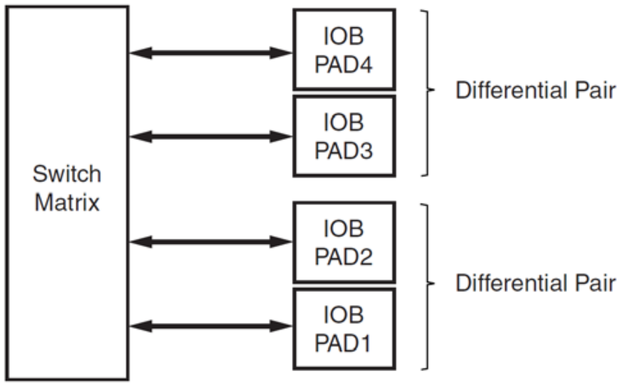


Figure 2 BQR2V3000 Input/Output Tile

Supported I/O Standards

BQR2V3000 IOB blocks feature SelectI/O-Ultra inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage (VCCINT = 1.5V), output driver supply voltage (VCCO) is dependent on the I/O standard (see Table 1). An auxiliary supply voltage (VCCAUX = 3.3 V) is required, regardless of the I/O standard used.

Table 1 Supported Single-Ended I/O Standards

I/O Satndard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage(V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS33	3.3	3.3	N/A	N/A
LVCMOS25	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
LVCMOS15	1.5	1.5	N/A	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
PCI-X	3.3	3.3	N/A	N/A
GTL	Note 1	Note 1	0.8	1.2
GTLP	Note 1	Note 1	1.0	1.5
HSTL_I	1.5	N/A	0.75	0.75
HSTL_II	1.5	N/A	0.75	0.75
HSTL_III	1.5	N/A	0.9	1.5
HSTL_IV	1.5	N/A	0.9	1.5
HSTL_I_18	1.8	N/A	0.9	0.9

I/O Satndard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage(V_{TT})
HSTL_II_18	1.8	N/A	0.9	0.9
HSTL_III_18	1.8	N/A	1.1	1.8
HSTL_IV_18	1.8	N/A	1.1	1.8
SSTL2_I	2.5	N/A	1.25	1.25
SSTL2_II	2.5	N/A	1.25	1.25
SSTL3_I	3.3	N/A	1.5	1.5
SSTL3_II	3.3	N/A	1.5	1.5
AGP-2X/AGP	3.3	N/A	1.32	N/A

Notes:

1.V_{CCO} of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad.

Table 2 Supported Differential Signal I/O Standards

I/O Satndard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Output V_{OD}
LVPECL_33	3.3	N/A	N/A	490mV to 1.22V
LDT_25	2.5	N/A	N/A	0.430-0.670
LVDS_33	3.3	N/A	N/A	0.250-0.400
LVDS_25	2.5	N/A	N/A	0.250-0.400
LVDSEXT_33	3.3	N/A	N/A	0.330-0.700
LVDSEXT_25	2.5	N/A	N/A	0.330-0.700
BLVDS_25	2.5	N/A	N/A	0.250-0.450
ULVDS_25	2.5	N/A	N/A	0.430-0.670

All of the user IOBs have fixed-clamp diodes to VCCO and to ground. These IOBs are not 5V tolerant.

Logic Resources

IOB blocks include six storage elements, as shown in Figure 3.Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch.On the input, output, and 3-state path, one or two DDR registers can be used.

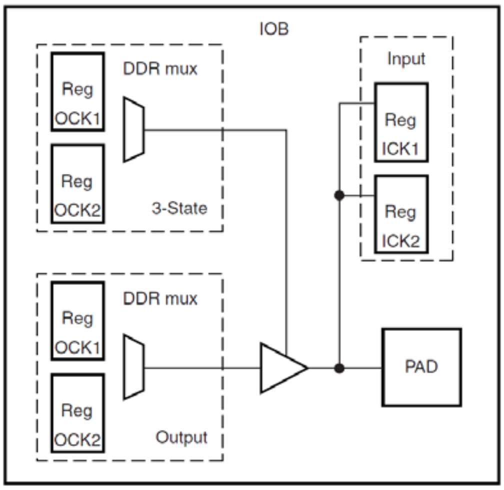


Figure 3 BQR2V3000 IOB Block

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 4. There are two input, output, and 3-state data signals, each being alternately clocked out.

The DDR mechanism shown in Figure 4 can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay.It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. BQR2V3000 can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic“1”. SRLOW forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0,and INIT1 attributes are independent. Synchronous or asynchronous set/reset is consistent in an IOB block.All the control signals have independent polarities. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers orlatches) (see Figure 5) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

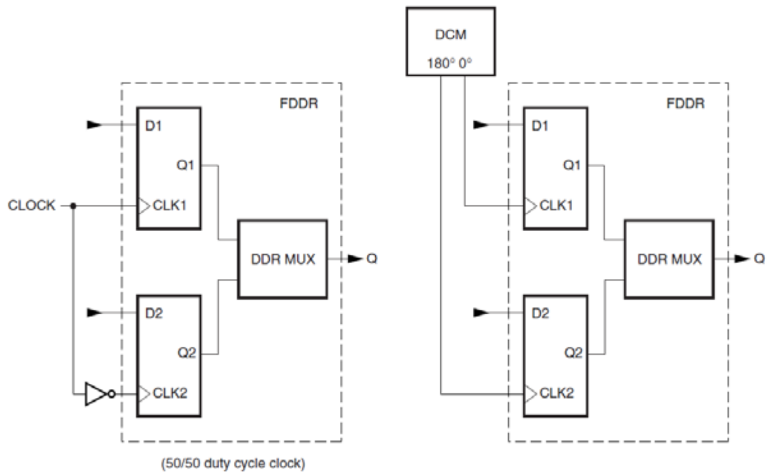


Figure 4 Double Data Rate Registers

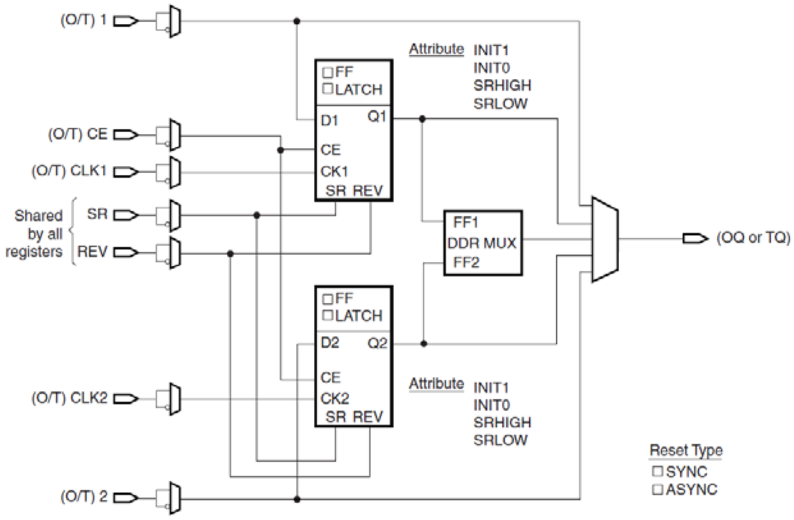


Figure 5 Register/Latch Configuration in an IOB Block

Input Path

The BQR2V3000 IOB input path routes input signals directly to internal logic and/or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the BQR2V3000 and when used, ensures that the pad-to-pad hold time is zero.Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, VREF. The need to supply VREF imposes constraints on which standards can be used in the same bank.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and/or the 3-state signal can be routed to the buffer directly from the internal logic or through an output/3-state flip-flop or latch, or through the DDR output/3-state registers.Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied VCCO voltage. The need to supply VCCO imposes constraints on which standards can be used in the same bank.

I/O Banking

Some of the I/O standards described above require VCCO and VREF voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks.Consequently, restrictions exist about which I/O standards can be combined within a given bank. Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 6. Each bank has multiple VCCO pins, all of which must be connected to the same voltage.This voltage is determined by the output standards in use.

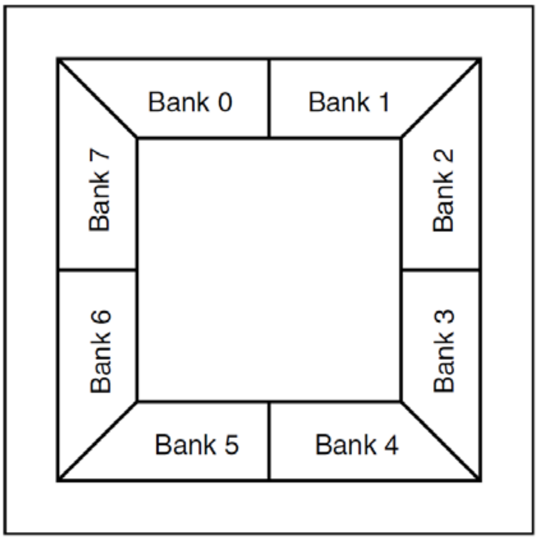


Figure 6 BQR2V3000 I/O Banks:Top View for Wire-Bond Package

Some input standards require a user-supplied threshold voltage (VREF), and certain user-I/O pins are automatically configured as VREF inputs. Approximately one in six of the I/O pins in the bank assume this role.

VREF pins within a bank are interconnected internally, and consequently only one VREF voltage can be used within each bank. However, for correct operation, all VREF pins in the bank must be connected to the external reference voltage source.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bidirectional standards in the same bank:

1. Combining output standards only.

Output standards with the same output VCCO requirement can be combined in the same bank.

Compatible example:

SSTL2_I and LVDS_25_DCI outputs

Incompatible example:

SSTL2_I (output VCCO = 2.5V) and LVCMOS33 (output VCCO = 3.3V) outputs

2. Combining input standards only.

Input standards with the same input VCCO and input VREF requirements can be combined in the same bank.

Compatible example:

LVCMOS15 and HSTL_IV inputs

Incompatible example:

LVCMOS15 (input VCCO = 1.5V) and

LVCMOS18 (input VCCO = 1.8V) inputs

Incompatible example:

HSTL_I_DCI_18 (VREF = 0.9V) and

HSTL_IV_DCI_18 (VREF = 1.1V) inputs

3. Combining input standards and output standards.

Input standards and output standards with the same input VCCO and output VCCO requirement can be combined in the same bank.

Compatible example:

LVDS_25 output and HSTL_I input

Incompatible example:

LVDS_25 output (output VCCO = 2.5V) and

HSTL_I_DCI_18 input (input VCCO = 1.8V)

4. Combining bidirectional standards with input or output standards.

When combining bidirectional I/O with other standards, make sure the bidirectional standard can meet rules 1 through 3 above.

5. Additional rules for combining DCI I/O standards.

a. No more than one Single Termination type (input or output) is allowed in the same bank.

Incompatible example:

HSTL_IV_DCI input and HSTL_III_DCI input

b. No more than one Split Termination type (input or output) is allowed in the same bank.

Incompatible example:

HSTL_I_DCI input and HSTL_II_DCI input

Table 3 summarizes all standards and voltage supplies.

Table 3 Summary of Voltage Supply Requirements to All Input and Output Standards

I/O Standard	V_{CCO}	V_{REF}	Termination Type

	Output	Input	Input	Output	Input
LVDS_33	3.3	N/R	N/R[1]	N/R	N/R
LVDSEXT_33			N/R	N/R	N/R
LVPECL_33			N/R	N/R	N/R
SSTL3_I			1.5	N/R	N/R
SSTL3_II			1.5	N/R	N/R
AGP			1.32	N/R	N/R
LVTTL		3.3	N/R	N/R	N/R
LVCMOS33			N/R	N/R	N/R
LVDCI_33			N/R	Series	N/R
LVDCI_DV2_33			N/R	Series	N/R
PCI33_3			N/R	N/R	N/R
PCI66_3			N/R	N/R	N/R
PCIX			N/R	N/R	N/R
LVDS_33_DCI			N/R	N/R	Split
LVDSEXT_33_DCI			N/R	N/R	Split
SSTL3_I_DCI			1.5	N/R	Split
SSTL3_II_DCI			1.5	Split	Split
LVDS_25	2.5	N/R	N/R	N/R	N/R
LVDSEXT_25			N/R	N/R	N/R
LDT_25			N/R	N/R	N/R
ULVDS_25			N/R	N/R	N/R
BLVDS_25			N/R	N/R	N/R
SSTL2_I			1.25	N/R	N/R
SSTL2_II			1.25	N/R	N/R
LVCMOS25		2.5	N/R	N/R	N/R
LVDCI_25			N/R	Series	N/R
LVDCI_DV2_25			N/R	Series	N/R
LVDS_25_DCI			N/R	N/R	Split
LVDSEXT_25_DCI			N/R	N/R	Split
SSTL2_I_DCI			1.25	N/R	Split
SSTL2_II_DCI			1.25	Split	Split
HSTL_III_18	1.8	N/R	1.1	N/R	N/R
HSTL_IV_18			1.1	N/R	N/R

<table>
<tr><th rowspan="2">I/O Standard</th><th colspan="2">V_{CCO}</th><th>V_{REF}</th><th colspan="2">Termination Type</th></tr>
<tr><th>Output</th><th>Input</th><th>Input</th><th>Output</th><th>Input</th></tr>
<tr><td>HSTL_I_18</td><td rowspan="13"></td><td rowspan="4"></td><td>0.9</td><td>N/R</td><td>N/R</td></tr>
<tr><td>HSTL_II_18</td><td>0.9</td><td>N/R</td><td>N/R</td></tr>
<tr><td>SSTL18_I</td><td>0.9</td><td>N/R</td><td>N/R</td></tr>
<tr><td>SSTL18_II</td><td>0.9</td><td>N/R</td><td>N/R</td></tr>
<tr><td>LVCMOS18</td><td rowspan="9">1.8</td><td>N/R</td><td>N/R</td><td>N/R</td></tr>
<tr><td>LVDCI_18</td><td>N/R</td><td>Series</td><td>N/R</td></tr>
<tr><td>LVDCI_DV2_18</td><td>N/R</td><td>Series</td><td>N/R</td></tr>
<tr><td>HSTL_III_DCI_18</td><td>1.1</td><td>N/R</td><td>Single</td></tr>
<tr><td>HSTL_IV_DCI_18</td><td>1.1</td><td>Single</td><td>Single</td></tr>
<tr><td>HSTL_I_DCI_18</td><td>0.9</td><td>N/R</td><td>Split</td></tr>
<tr><td>HSTL_II_DCI_18</td><td>0.9</td><td>Split</td><td>Split</td></tr>
<tr><td>SSTL18_I_DCI</td><td>0.9</td><td>N/R</td><td>Split</td></tr>
<tr><td>SSTL18_II_DCI</td><td>0.9</td><td>Split</td><td>Split</td></tr>
<tr><td>HSTL_III</td><td rowspan="12">1.5</td><td rowspan="4">N/R</td><td>0.9</td><td>N/R</td><td>N/R</td></tr>
<tr><td>HSTL_IV</td><td>0.9</td><td>N/R</td><td>N/R</td></tr>
<tr><td>HSTL_I</td><td>0.75</td><td>N/R</td><td>N/R</td></tr>
<tr><td>HSTL_II</td><td>0.75</td><td>N/R</td><td>N/R</td></tr>
<tr><td>LVCMOS15</td><td rowspan="8">1.5</td><td>N/R</td><td>N/R</td><td>N/R</td></tr>
<tr><td>LVDCI_15</td><td>N/R</td><td>Series</td><td>N/R</td></tr>
<tr><td>LVDCI_DV2_15</td><td>N/R</td><td>Series</td><td>N/R</td></tr>
<tr><td>GTLP_DCI</td><td>1</td><td>Single</td><td>Single</td></tr>
<tr><td>HSTL_III_DCI</td><td>0.9</td><td>N/R</td><td>Single</td></tr>
<tr><td>HSTL_IV_DCI</td><td>0.9</td><td>Single</td><td>Single</td></tr>
<tr><td>HSTL_I_DCI</td><td>0.75</td><td>N/R</td><td>Split</td></tr>
<tr><td>HSTL_II_DCI</td><td>0.75</td><td>Split</td><td>Split</td></tr>
<tr><td>GTL_DCI</td><td>1.2</td><td>1.2</td><td>0.8</td><td>Single</td><td>Single</td></tr>
<tr><td>GTLP</td><td rowspan="2">N/R</td><td rowspan="2">N/R</td><td>1</td><td>N/R</td><td>N/R</td></tr>
<tr><td>GTL</td><td>0.8</td><td>N/R</td><td>N/R</td></tr>
</table>

Notes:1. N/R = no requirement.

Digitally Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball gridarrays) can not accommodate external termination resistors.

DCI provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os. This eliminates the need for external resistors, and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, the voltage reference of the N transistor (VRN), and the voltage reference of the P transistor (VRP) are shown in Figure 7.

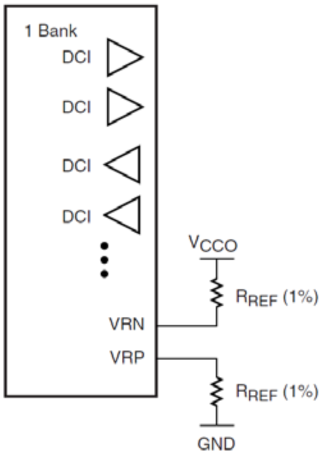


Figure 7 DCI in a BQR2V3000 Bank

When used with a terminated I/O standard, the value of resistors are specified by the standard (typically 50 Ω).When used with a controlled impedance driver, the resistors set the output impedance of the driver within the specified range (25 Ω to 100 Ω). For all series and parallel terminations listed in Table 4 and Table 5, the reference resistors must have the same value for any given bank. One percent resistors are recommended.The DCI system adjusts the I/O impedance to match the two external reference resistors or half of the reference resistors, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

Table 4 SelectI/O-Ultra Controlled Impedance Buffers

V_{CCO}	DCI	DCI Half Impedance
3.3V	LVDCI_33	LVDCI_DV2_33
2.5V	LVDCI_25	LVDCI_DV2_25

1.8V	LVDCI_18	LVDCI_DV2_18
1.5V	LVDCI_15	LVDCI_DV2_15

Controlled Impedance Drives(Series Termination)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance (Z). BQR2V3000 input buffers also support LVDCI and LVDCI_DV2 I/O standards.

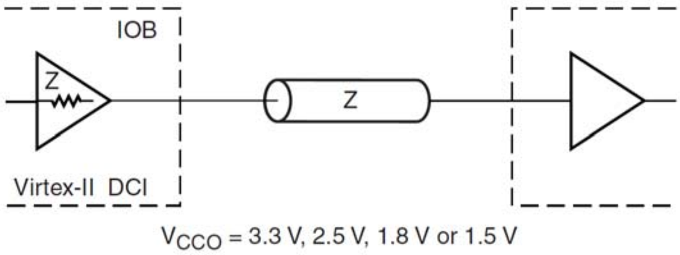


Figure 8 Internal Series Termination

Controlled Impedance Drives(Parallel Termination)

DCI also provides on-chip termination for SSTL3, SSTL2,HSTL (Class I, II, III, or IV), and GTL/GTLP receivers or transmitters on bidirectional lines.

Table 5 lists the on-chip parallel terminations available in BQR2V3000. VCCO must be set according to Table 6.Note that there is a VCCO requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

Table 5 SelectI/O-Ultra Controlled Impedance Buffers

I/O Standard	External Termination	On-Chip Termination
SSTL3 Class I	SSTL3_I	SSTL3_I_DCI (1)
SSTL3 Class II	SSTL3_II	SSTL3_II_DCI (1)
SSTL2 Class I	SSTL2_I	SSTL2_I_DCI (1)
SSTL2 Class II	SSTL2_II	SSTL2_II_DCI (1)
HSTL Class I	HSTL_I	HSTL_I_DC
HSTL Class II	HSTL_II	HSTL_II_DC
HSTL Class III	HSTL_III	HSTL_III_DC
HSTL Class IV	HSTL_IV	HSTL_IV_DC
GTL	GTL	GTL_DC
GTLP	GTLP	GTLP_DC

Table 6 Supported DCI I/O Standards

I/O Standard	**Output VCCO**	**Input VCCO**	**Input VREF**	**Termination Type**
LVDCI_33(1)	3.3	3.3	N/A	Series
LVDCI_DV2_33(1)	3.3	3.3	N/A	Series
LVDCI_25(1)	2.5	2.5	N/A	Series
LVDCI_DV2_25(1)	2.5	2.5	N/A	Series
LVDCI_18(1)	1.8	1.8	N/A	Series
LVDCI_DV2_18(1)	1.8	1.8	N/A	Series
LVDCI_15(1)	1.5	1.5	N/A	Series
LVDCI_DV2_15(1)	1.5	1.5	N/A	Series
GTL_DCI	1.2	1.2	0.8	Single
GTLP_DCI	1.5	1.5	1.0	Single
HSTL_I_DCI	1.5	1.5	0.75	Split
HSTL_II_DCI	1.5	1.5	0.75	Split
HSTL_III_DCI	1.5	1.5	0.9	Single
HSTL_IV_DCI	1.5	1.5	0.9	Single
HSTL_I_DCI	1.8	N/A	0.9	Split
HSTL_II_DCI	1.8	N/A	0.9	Split
HSTL_III_DCI	1.8	N/A	1.1	Single
HSTL_IV_DCI	1.8	N/A	1.1	Single
SSTL2_I_DCI(2)	2.5	2.5	1.25	Split
SSTL2_II_DCI(2)	2.5	2.5	1.25	Split
SSTL3_I_DCI(2)	3.3	3.3	1.5	Split
SSTL3_II_DCI(2)	3.3	3.3	1.5	Split

Notes:

1. LVDCI_XX and LVDCI_DV2_XX are LVCMOS controlled impedance buffers, matching the reference resistors or half of the reference resistors.

2. These are SSTL compatible.

3.2.2 Configurable Logic Blocks (CLBs)

BQR2V3000 configurable logic blocks (CLB) are organized in an array and are used to build combinatorial and synchronous logic designs. Each CLB element is tied to a switch matrix to access the general routing matrix, as shown Figure 9.A CLB element comprises four similar slices with fast local feedback within the CLB. The four slices are split into two columns of two slices with two independent carry logic chains and one common shift chain.

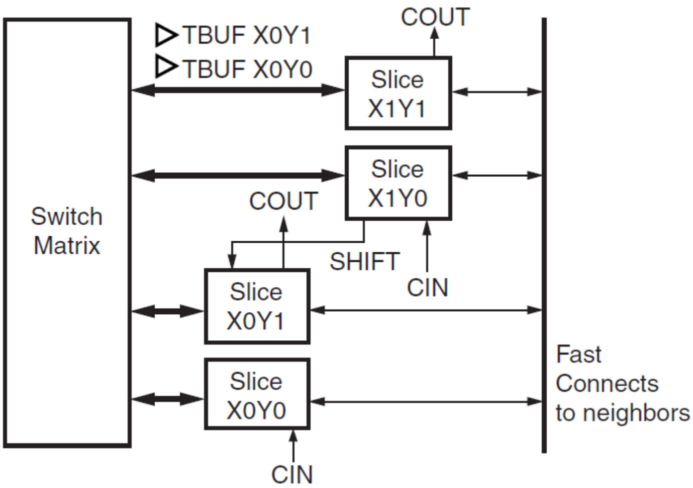


Figure 9 BQR2V3000 CLB Element

Slice Description

Each slice includes two 4-input function generators, carry logic, arithmetic logic gates, wide function multiplexers and two storage elements. As shown in Figure 10, each 4-input function generator is programmable as a 4-input LUT, 16 bits of distributed SelectRAM memory, or a 16-bit variable-tap shift register element.

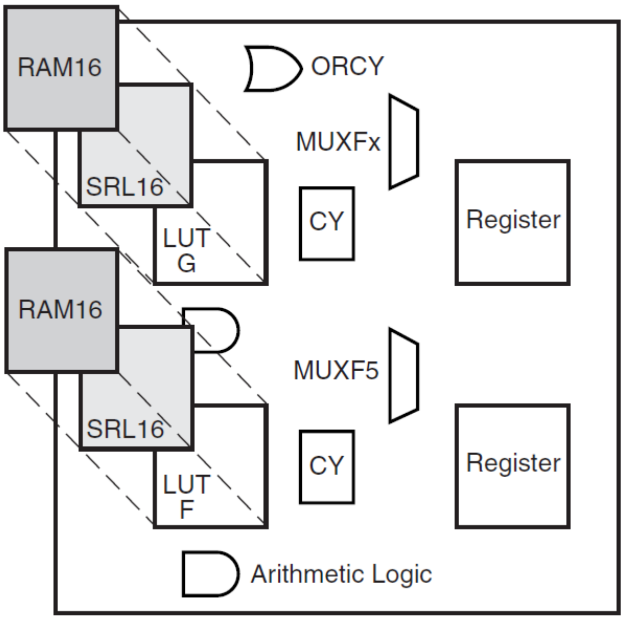


Figure 10 BQR2V3000 Slice Configuration

The output from the function generator in each slice drives both the slice output and the D input of the storage element. Figure 11 shows a more detailed view of a single slice.

Look-Up Table

BQR2V3000 function generators are implemented as 4-input look-up tables (LUTs). Four independent inputs are provided to each of the two function generators in a slice (F and G). These function generators are each capable of implementing any arbitrarily defined Boolean function of four inputs. The propagation delay is therefore independent of the function implemented. Signals from the function generators can exit the slice (X or Y output), can input the XOR dedicated gate (see arithmetic logic), or input the carry-logic multiplexer (see fast look-ahead carry logic), or feed the D input of the storage element, or go to the MUXF5 (not shown in Figure 11). In addition to the basic LUTs, the BQR2V3000 slice contains logic (MUXF5 and MUXFX multiplexers) that combines function generators to provide any function of five, six,seven, or eight inputs. The MUXFXs are either MUXF6,MUXF7, or MUXF8 according to the slice considered in the CLB. Selected functions up to nine inputs (MUXF5 multiplexer) can be implemented in one slice. The MUXFX can also be a MUXF6, MUXF7, or MUXF8 multiplexer to map any functions of six, seven, or eight inputs and selected wide logic functions.

Register/Latch

The storage elements in a BQR2V3000 slice can be configured as either edge-triggered D-type flip-flops or level-sensitive latches. The D input can be directly driven by the X or Y output via the DX or DY input, or by the slice inputs bypassing the function generators via the BX or BY input. The clock enable signal (CE) is active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.In addition to clock (CK) and clock enable (CE) signals, each slice has set and reset signals (SR and BY slice inputs). SR forces the storage element into the state specified by the attribute SRHIGH or SRLOW.SRHIGH forces a logic “1” when SR is asserted. SRLOW forces a logic “0”. When SR is used, a second input (BY) forces the storage element into the opposite state. The reset conditionis predominant over the set condition (Figure 12).The initial state after configuration or global initial state is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1.

For each slice, set and reset can be set to be synchronous or asynchronous. BQR2V3000 also have the ability to set INIT0 and INIT1 independent of SRHIGH and SRLOW.Control signals CLK,CE, and SR are common to both storage elements in one slice. All control signals have independent polarities. Any inverter placed on a control input is automatically absorbed.The set and reset functionality of a register or a latch can be configured as follows:

• No set or reset
• Synchronous set
• Synchronous reset
• Synchronous set and reset
• Asynchronous set (preset)
• Asynchronous reset (clear)
• Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

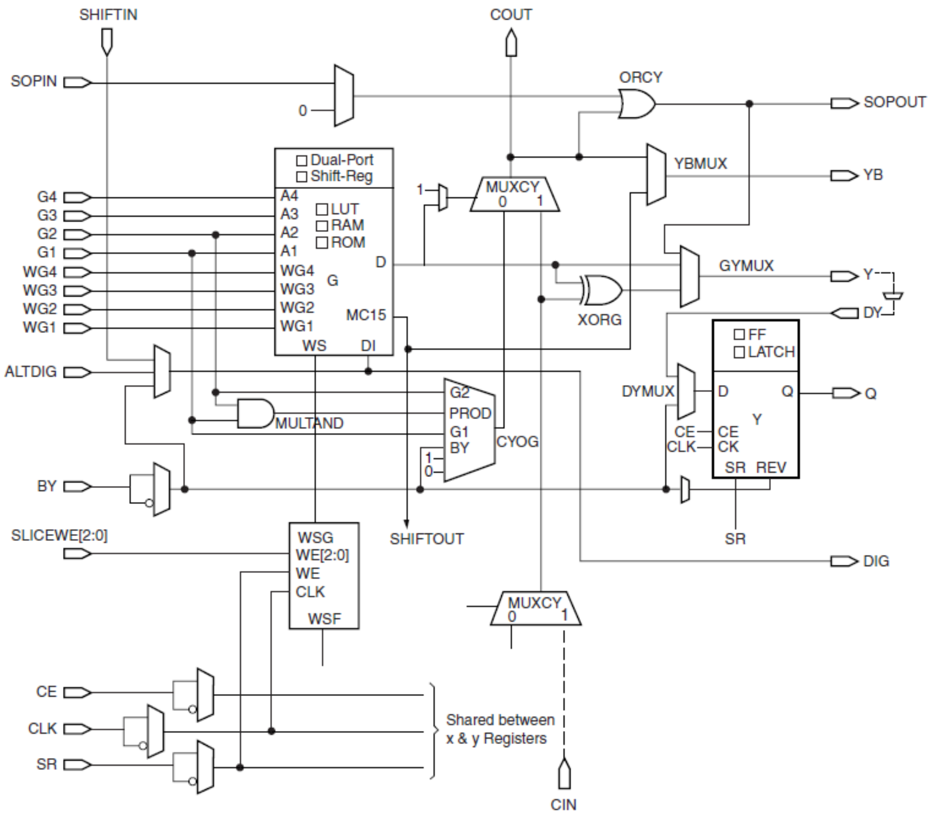


Figure 11 BQR2V3000 Slice(Top Half)

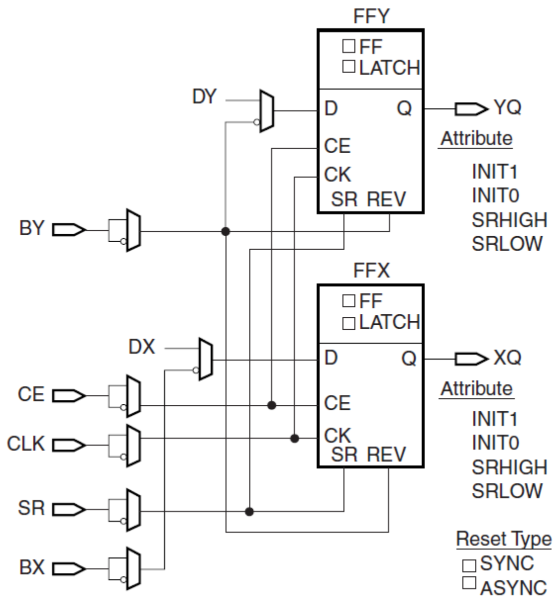


Figure 12 Register/Latch Configuration in a Slice

Distributed SelectRAM Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM element. The SelectRAM elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8 bit RAM
- Single-Port 32 x 4 bit RAM
- Single-Port 64 x 2 bit RAM
- Single-Port 128 x 1 bit RAM
- Dual-Port 16 x 4 bit RAM
- Dual-Port 32 x 2 bit RAM
- Dual-Port 64 x 1 bit RAM

Distributed SelectRAM memory modules are synchronous(write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.Table 7 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM configuration.

Table 7 Distributed SelectRAM Configurations

RAM	Number
16 x1S	1
16 x1D	2
32x1S	2
32x1D	4
64x1S	4
64x1D	8
128x1S	8

Notes:

1. S = single-port configuration, and D = dual-port configuration.

For single-port configurations, distributed SelectRAM memory has one address port for synchronous writes and asynchronous reads.For dual-port configurations, distributed SelectRAM memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port address.Figure 13,Figure 14, and Figure 15 illustrate various example configurations

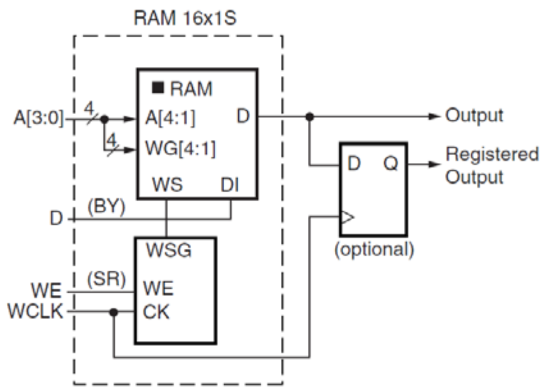


Figure 13 Distributed SelectRAM (RAM16x1S)

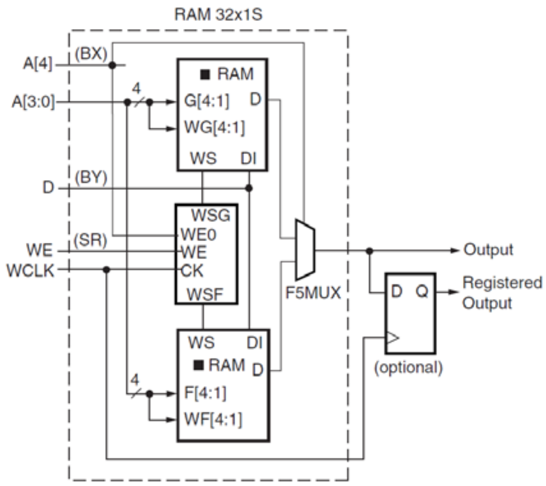


Figure 14 Single-Port Distributed SelectRAM(RAM32x1S)

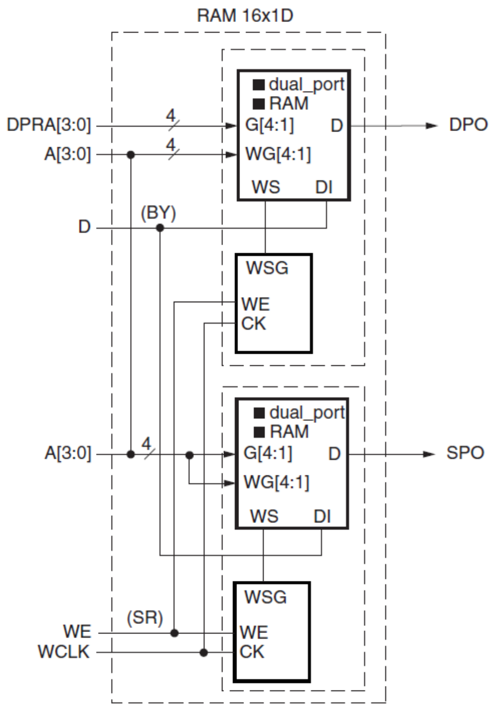


Figure 15 Dual-Port Distributed SelectRAM(RAM16x1D)

Similar to the RAM configuration, each function generator(LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1,ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM.ROM contents are loaded at configuration. Table 8 shows the number of LUTs occupied by each configuration.

Table 8 ROM Configuration

ROM	Number of LUTs
16 x1	1

32x1	2
64x1	4
128x1	8(1CLB)
256 x1	16(2CLB)

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 16. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous,however, the storage element or flip-flop is available to implement a synchronous read. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the seventh bit, the eighth bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

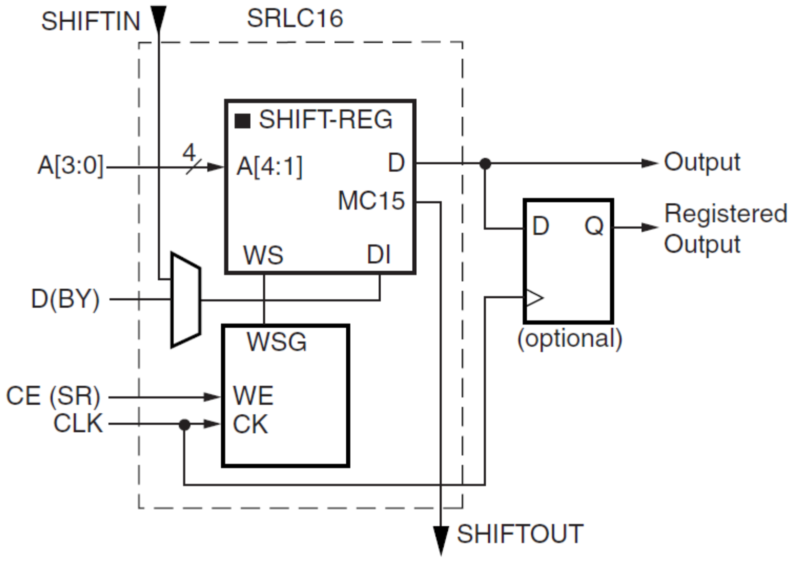


Figure 16 Shift Register Configurations

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output .Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

Multiplexers

BQR2V3000 function generators and associated multiplexers can implement the following:

• 4:1 multiplexer in one slice
• 8:1 multiplexer in two slices
• 16:1 multiplexer in one CLB element (4 slices)
• 32:1 multiplexer in two CLB elements (8 slices)

Each slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 17.Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Any LUT can implement a 2:1 multiplexer.

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The BQR2V3000 CLB has two separate carry chains.The height of the carry chains is two bits per slice. The carry chain in the BQR2V3000 is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 11)improves the efficiency of multiplier implementation.

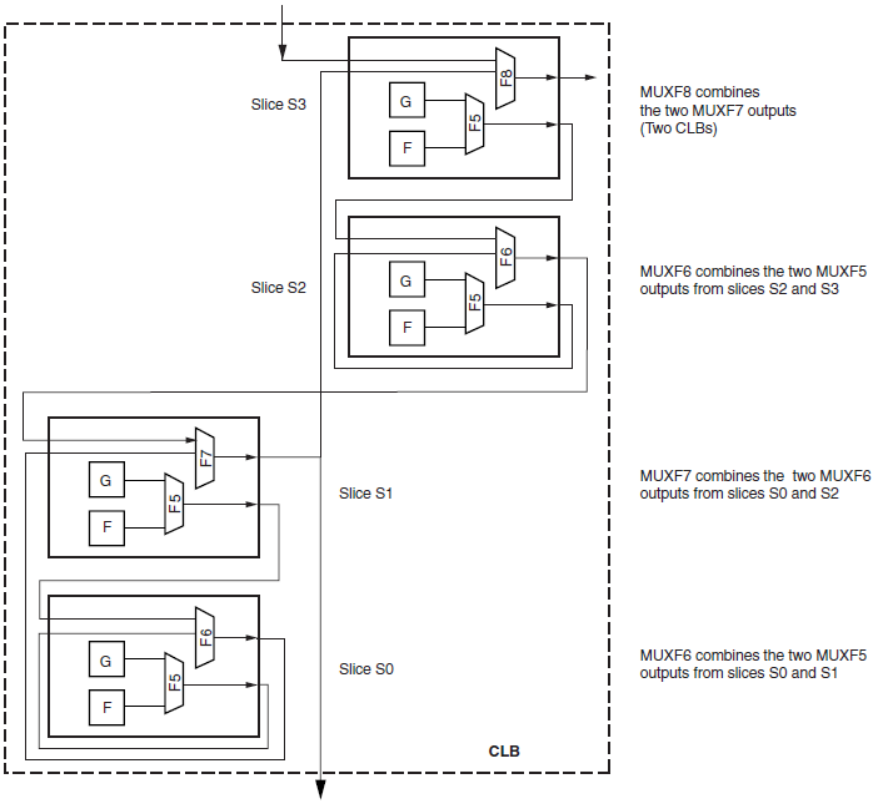


Figure 17 MUXF5 and MUXFX multiplexers

Sum of Products

Each slice has a dedicated OR gate named ORCY,ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice,as shown in Figure 18.LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 19 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

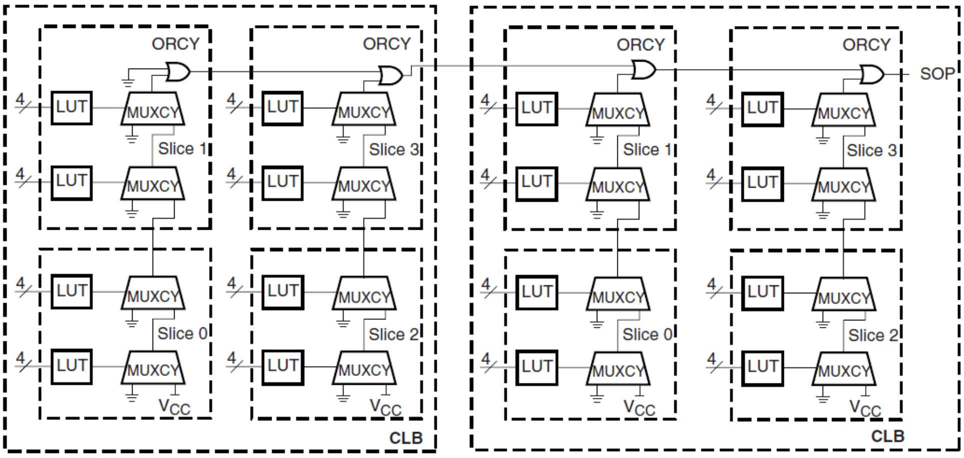


Figure 18 Horizontal Cascade Chain

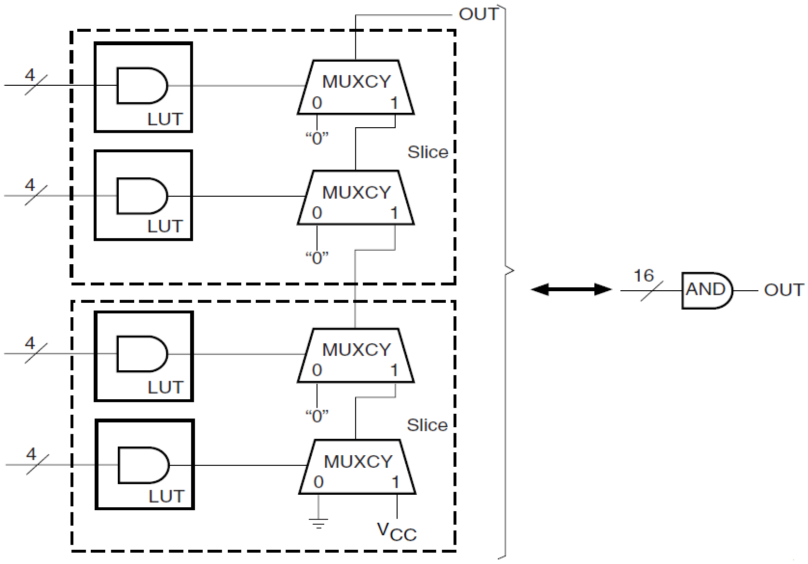


Figure 19 Wide-Input AND Gate(16Inputs)

3-State Buffers

Each CLB contains two 3-state drivers (TBUFs) that can drive on-chip buses. Each 3-state buffer has its own 3-state control pin and its own input pin.Each of the four slices have access to the two 3-state buffers through the switch matrix, as shown in Figure 20.TBUFs in neighboring CLBs can access slice outputs by direct connects. The outputs of the 3-state buffers drive horizontal routing resources used to implement 3-state buses.

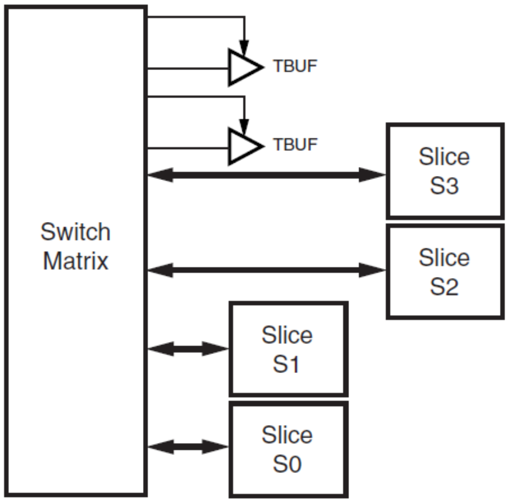


Figure 20 BQR2V3000 3-State Buffers

Four horizontal routing resources per CLB are provided for on-chip 3-state buses. Each 3-state buffer has access alternately to two horizontal lines, which can be partitioned as shown in Figure 21. The switch matrices corresponding to SelectRAM memory and multiplier or I/O blocks are skipped.Table 9 shows the number of 3-state buffers available in BQR2V3000.

Table 9 BQR2V3000 3-StateBuffers

Device	3-State Buffers per Row	Total Number of 3-State Buffers
BQR2V3000	112	7,168

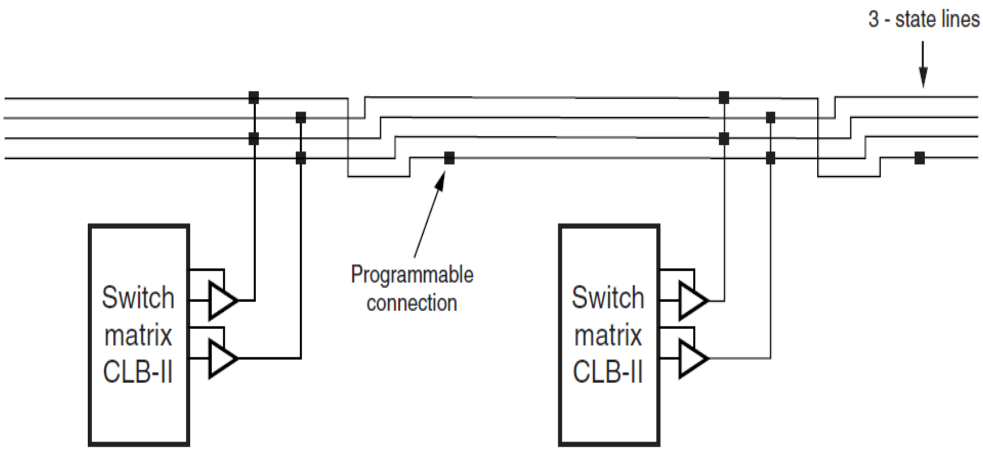


Figure 21 3-State Buffer Connection to Horizontal Lines

Table 10 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be implemented in one of the configurations listed. Table 11 shows the available resources in all CLBs.

Table 10 Logic Resources in One CLB

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic &CarryChains	SOP Chains	Distributed SelectRAM	Shift Registers	TBUF
4	8	8	8	2	2	128bits	128bits	2

Table 11 BQR2V3000 Logic Resource Avallable In All CLBs

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry Chains(1)	Number of SOP Chains(1)
BQR2V3000	64 x 56	14,336	28,672	458,752	28,672	112	128

Notes:

1. The carry chains and SOP chains can be split or cascaded.

3.2.3 Block SelectRAM Memory

BQR2V3000 incorporate large amounts of 18 Kbit block SelectRAM. These complement the distributed SelectRAM resources that provide shallow RAM structures implemented in CLBs. Each BQR2V3000 block SelectRAM is an 18 Kbit true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for writes) and Data/parity data outputs (for reads). Operation is synchronous. The block SelectRAM behaves like a register. Control, address, and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

The BQR2V3000 block SelectRAM supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 12

Table 12 Dual- and Single-Port Configurations

16Kx1 bit	2Kx9bits
8Kx2bits	1Kx18bits

4Kx4bits	512x36bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM has access to the 18 Kbit memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kbit memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of 9-bit, 18-bit, and 36-bit widths is the ability to store a parity bit for everyeight bits. Parity bits must be generated or checked externally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of BQR2V3000 block SelectRAM memory to advantage.

Each block SelectRAM cell is a fully synchronous memory,as illustrated in Figure 22. Input data bus and output data bus widths are identical.

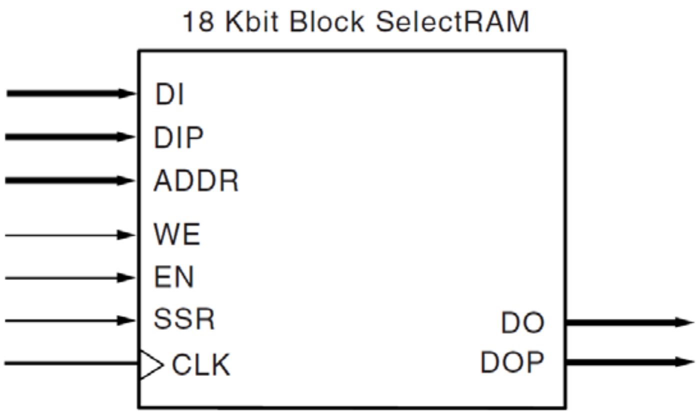


Figure 22 18 Kbit Block SelectRAM Memory in Single-Port Mode

Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM has access to a common 18 Kbit memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18 Kbit block is accessible from Port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations, the 16 Kbit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18 Kbit memory block and the other port having access to a 16 Kbit subset of the memory block equal to 16 Kbits. Each block SelectRAM cell is a fully synchronous memory,as illustrated in Figure 23.The two ports have independentinputs and outputs and are independently clocked.

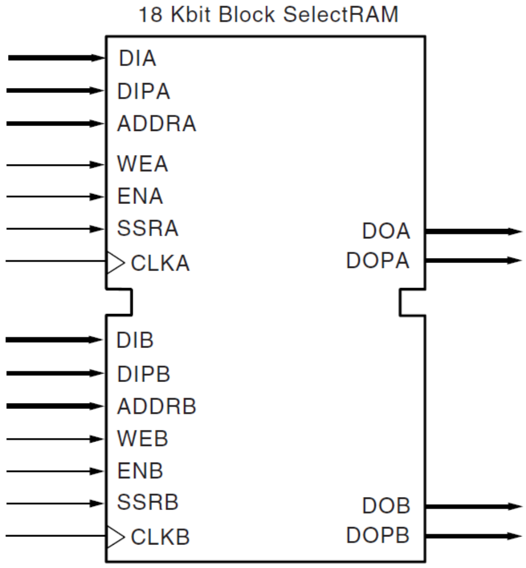


Figure 23 18 Kbit Block SelectRAM in Dual-Port Mode

Port Aspect Ratios

Table 13 shows the depth and the width aspect ratios for the 18 Kbit block SelectRAM. BQR2V3000 block SelectRAM also includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM, and multipliers.

Table 13 18Kbit Block SelectRAM Port Aspect Ratio

Width	Depth	Address Bus	Data Bus	Parity Bus
1	16,384	ADDR[13:0]	DATA[0]	N/A
2	8,192	ADDR[12:0]	DATA[1:0]	N/A
4	4,096	ADDR[11:0]	DATA[3:0]	N/A
9	2,048	ADDR[10:0]	DATA[70]	Parity[0]
18	1,024	ADDR[9:0]	DATA[15:0]	Parity[1:0]
36	512	ADDR[8:0]	DATA[31:0]	Parity[3:0]

Read/Write Operations

The BQR2V3000 block SelectRAM read operation is fully synchronous. An address is presented, and the read operation is enabled by control signals WEA and WEB in addition to ENA or ENB. Then, depending on clock polarity,a rising or falling clock edge causes the stored data to be loaded into output registers.The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA or WEB in addition to ENA or ENB.Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed. A write operation performs a simultaneous read operation.Three different options are available, selected by configuration:

1. WRITE_FIRST

The WRITE_FIRST option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO as shown in Figure 24.

2. READ_FIRST

The READ_FIRST option is a read-before-write mode.The same clock edge that writes data input (DI) into the memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 25

3. NO_CHANGE

The NO_CHANGE option maintains the content of the output registers, regardless of the write operation. The clock edge during the write mode has no effect on the content of the data output register DO. When the port is configured as NO_CHANGE, only a read operation loads a new value in the output register DO, as shown in Figure 26.

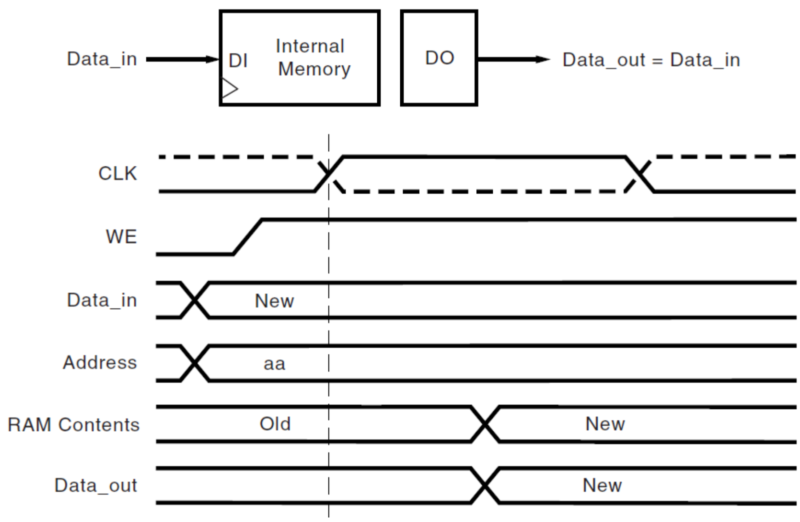


Figure 24 WRITE_FIRST Mode

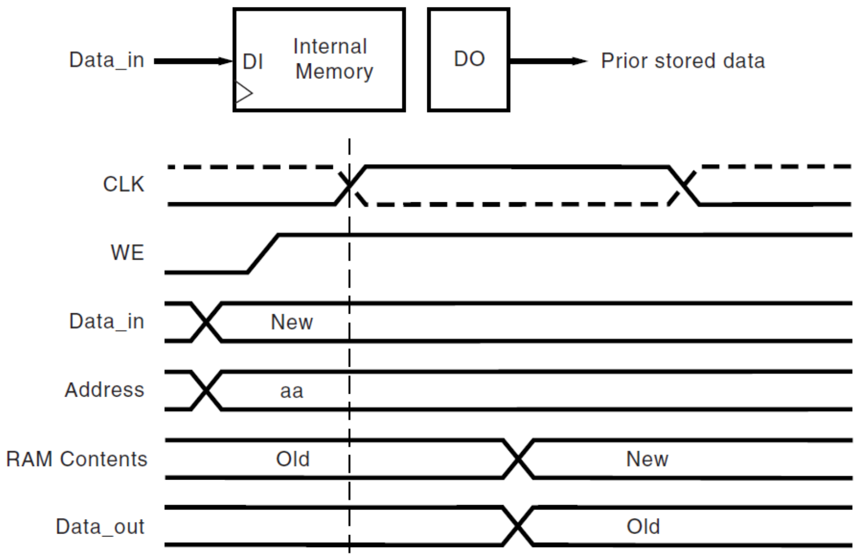


Figure 25 READ_FIRST Mode

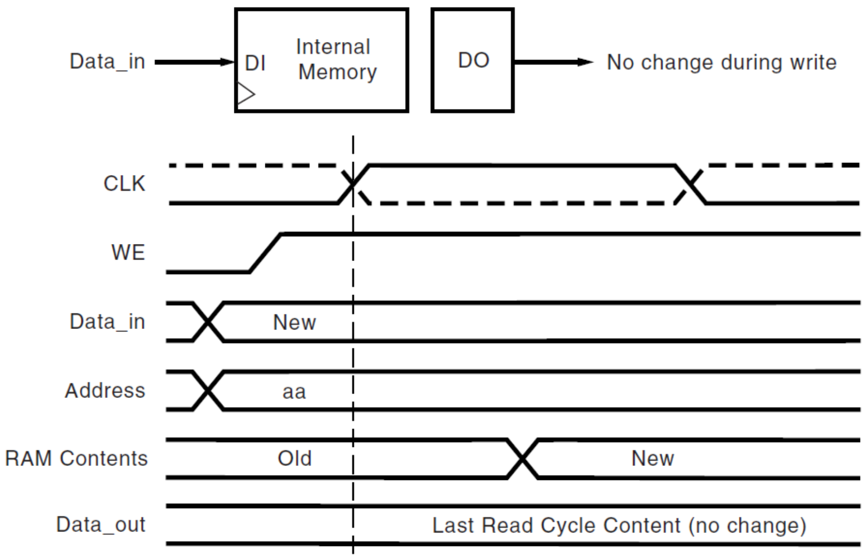


Figure 26 NO_CHANGE Mode

Control Pins and Attributes

BQR2V3000 SelectRAM memory has two independent ports with the control signals described in Table 14. All control inputs including the clock have an optional inversion.

Table 14 Control Functions

Control Signal	Function
CLK	Read and Write Clock
EN	Enable affects Read, Write, Set, Reset
WE	Write Enable

SSR	Set DO register to SRVAL (attribute)

Initial memory content is determined by the INIT_xx attributes. Separate attributes determine the output register value after device configuration (INIT) and SSR is asserted(SRVAL). Both attributes (INIT_B and SRVAL) are available for each port when a block SelectRAM resource is configured as dual-port RAM.

BQR2V3000 SelectRAM memory blocks are located in six columns. Column locations are shown in Table 15.

Table 15 SelectRAM Memory Floor Plan

Device	Columns	SelectRAM Blocks	
		Per Column	Total
BQR2V3000	6	16	96

Table 16 shows the amount of block SelectRAM memory available for BQR2V3000. The 18 Kbit SelectRAM blocks are cascadable to implement deeper or wider single- or dual-port memory resources.

Table 16 BQR2V3000 SelectRAM Memory Available

Device	Total SelectRAM Memory		
	Blocks	in Kbits	in Bits
BQR2V3000	96	1,728	1,769,472

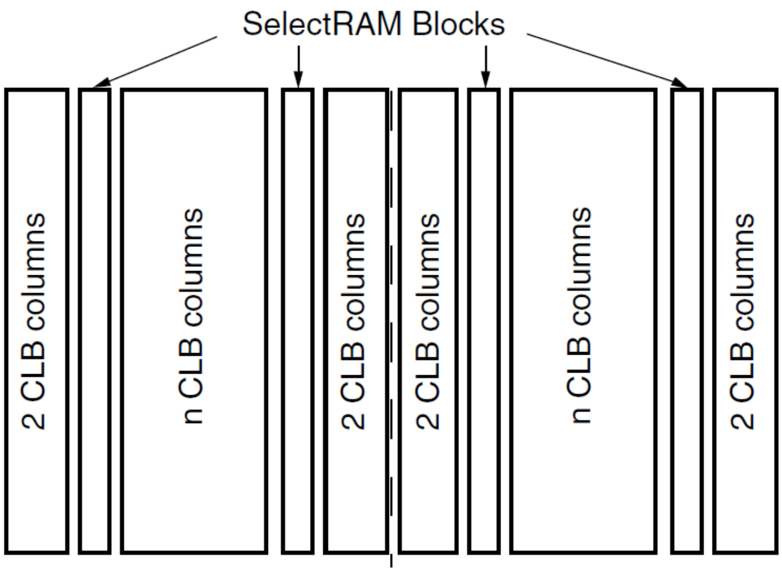


Figure 27 Block SelectRAM(4-column)

3.2.4 18-Bit×18-Bit Multipliers

A BQR2V3000 multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. BQR2V3000 incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kbit block SelectRAM resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit×18-bit multiplier in slices. Each SelectRAM memory and multiplier block is tied to four switch matrices, as shown in Figure 28.

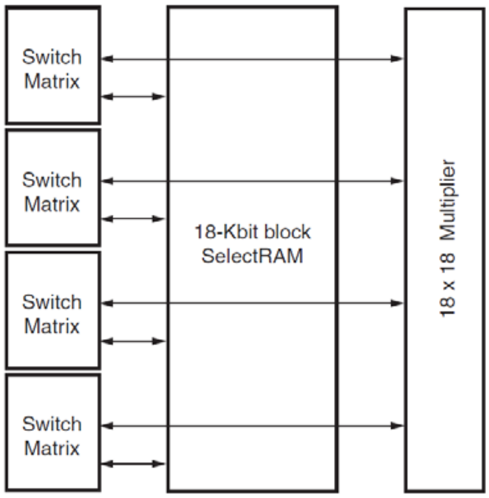


Figure 28 18-Bit×18-Bit Multipliers

The interconnect is designed to allow SelectRAM memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM and the multiplier. Thus, SelectRAM memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM resource feeding the multiplier. The use of SelectRAM memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits.Figure 29 shows a multiplier block.

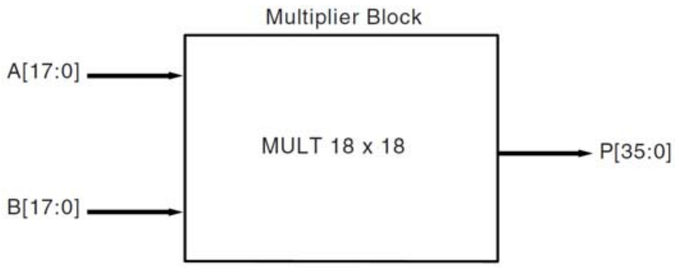


Figure 29 Multiplier Block

Multiplier organization is identical to the 18 Kbit SelectRAM organization, because each multiplier is associated with an 18 Kbit block SelectRAM resource.

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic.

Table 17 Multiplier Floor Plan

Device	Columns	Multipliers	
		Per Column	Total
BQR2V3000	6	16	96

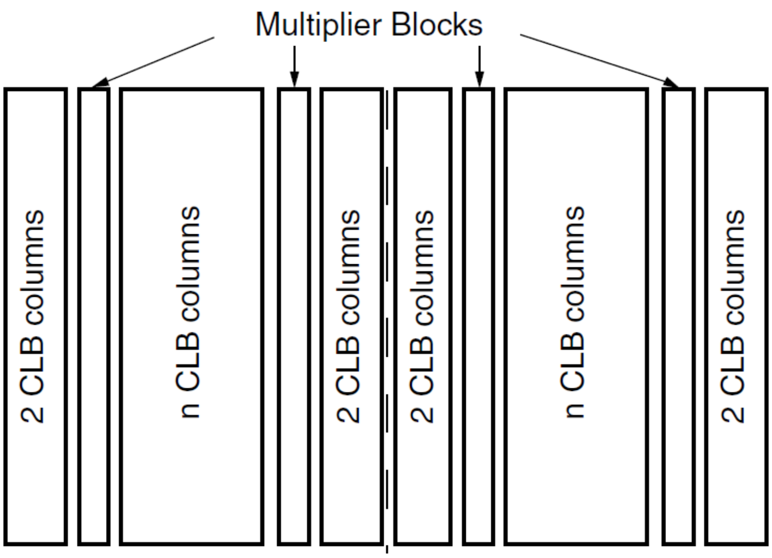


Figure 30 Multipliers(4-column)

3.2.5 Digital Clock Manager (DCM)

The BQR2V3000 DCM offers a wide range of powerful clock management features:

- Clock De-skew: The DCM generates new system clocks (either internally or externally to the FPGA),which are phase-aligned to the input clock, thus eliminating clock distribution delays.

- Frequency Synthesis: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- Phase Shifting: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 31). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

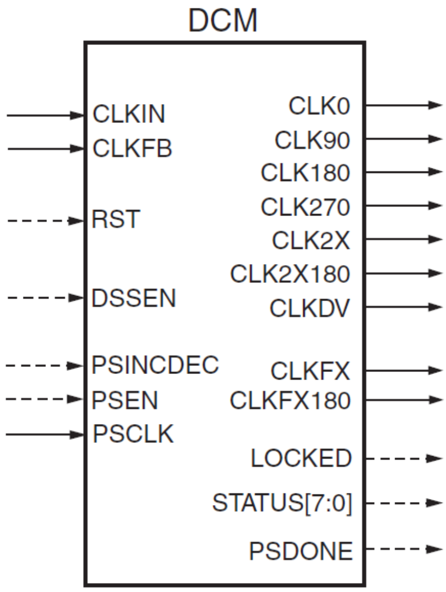


Figure 31 Digital Clock Manager

The DCM can be configured to delay the completion of the BQR2V3000 configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

The DCM has the following general control signals:

• RST input pin: resets the entire DCM.

• LOCKED output pin: asserted High when all enabled DCM circuits have locked.

• STATUS output pins (active High): shown in Table 18.

Table 18 DCM Statue Pins

Status Pin	Function
0	Phase Shift Overflow

1	CLKIN Stopped
2	CLKFX Stopped
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A

Clock De-Skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line.Additional delay is introduced so that clock edges arrive at internal registers and block RAMs simultaneously with the clock edges arriving at the input clock pad. Alternatively,external clocks, which are also de-skewed relative to the input clock, can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and,therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, the CLKFB input must be connected, and its source must be either CLK0 or CLK2X.CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs double the clock frequency.The CLKDV output creates divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7,7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

FREQCLKFX = (M/D) * FREQCLKIN

where M and D are two integers. By default, M=4 and D=1, which results in a clock output frequency four times faster than the clock input frequency(CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X.CLKFX180 is phase shifted 180 degrees relative to CLKFX.All frequency synthesis outputs automatically have 50/50 duty cycles (with the exception of the CLKDV output whenperforming a non-integer divide in high-frequency mode).

Note: CLK2X and CLK2X180 are not available in high-frequencymode.

Phase Shifting

The DCM provides additional control over clock skew through either coarse- or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by 1/4 of the input clock period relative to each other, providing coarse phase control.Note that CLK90 and CLK270 are not available in high-frequency mode.

Fine-phase adjustment affects all nine DCM output clocks.When activated, the phase shift between the rising edges of CLKIN and CLKFB is a specified fraction of the input clock period.

In variable mode, the PHASE SHIFT value can also be dynamically incremented or decremented as determined by PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 32 illustrates the effects of fine-phase shifting.

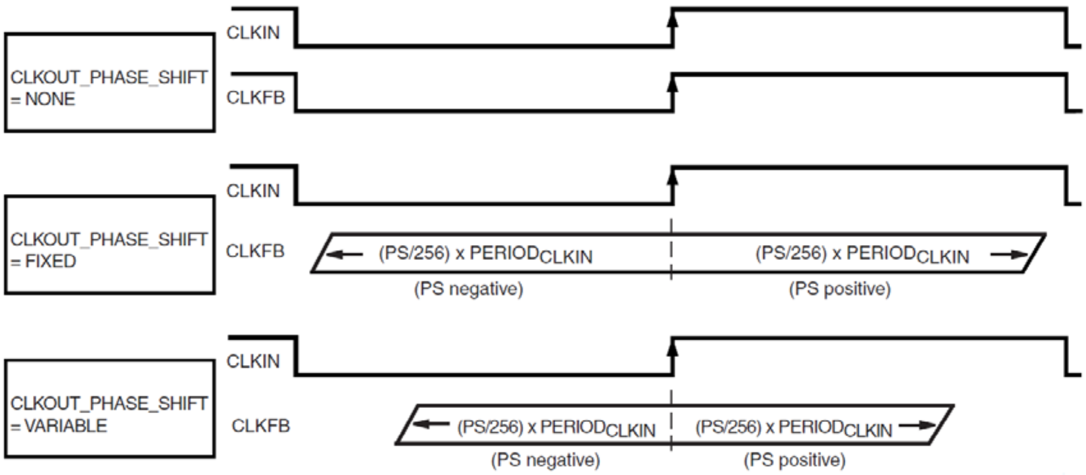


Figure 32 Fine-Phase Shifting Effects

Table 19 lists fine-phase shifting control pins, when used in variable mode.

Table 19 Fine-Phase Shifting Control Pins

Control Pin	Direction	Function
PSINCDEC	In	Increment or decrement
PSEN	In	Enable±phase shift
PSCLK	In	Clock for phase shift
PSDONE	Out	Active when completed

Two separate components of the phase shift range must be understood:

• PHASE_SHIFT attribute range

• FINE_SHIFT_RANGE DCM timing parameter range

The PHASE_SHIFT attribute is the numerator in the following equation:

Phase Shift (ns) = (PHASE_SHIFT/256) * PERIODCLKIN

The full range of this attribute is always -255 to +255, but its practical range varies with CLKIN frequency, as constrained by the FINE_SHIFT_RANGE component, which represents the total delay achievable by the phase shift delay line. Total delay is a function of the number of delay taps used in the circuit.

Absolute range (fixed mode) = ± FINE_SHIFT_RANGE

Absolute range (variable mode) = ± FINE_SHIFT_RANGE/2

The reason for the difference between fixed and variable modes is as follows. For variable mode to allow symmetric,dynamic sweeps from -255/256 to +255/256, the DCM sets the "zero phase skew" point as the middle of the delay line,thus dividing the total delay line range in half. In fixed mode,since the PHASE_SHIFT value never changes after configuration, the entire delay line is available for insertioninto either the CLKIN or CLKFB path (to create either positive or negative skew).

Taking both of these components into consideration, the following are some usage examples:

- If PERIODCLKIN = 2 * FINE_SHIFT_RANGE, then PHASE_SHIFT in fixed mode is limited to ± 128, and in variable mode it is limited to ± 64.
- If PERIODCLKIN = FINE_SHIFT_RANGE, then PHASE_SHIFT in fixed mode is limited to ± 255, and in variable mode it is limited to ± 128.
- If PERIODCLKIN ≤ 0.5 * FINE_SHIFT_RANGE, then PHASE_SHIFT is limited to ± 255 in either mode.

Operating Modes

The frequency ranges of DCM input and output clocks depend on the operating mode specified, either low-frequency mode or high-frequency mode, according to Table 20. The CLK2X, CLK2X180,CLK90, and CLK270 outputs are not available in high-frequency mode.High or low-frequency mode is selected by an attribute.

Table 20 DCM Frequency Ranges

Output Clock	**Low-Frequency Mode**		**High-Frequency Mode**	
	CLKIN Input	**CLK Output**	**CLKIN Input**	**CLK Output**
CLK0,CLK180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_1X_HF
CLK90,CLK270	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	NA	NA
CLK2X,CLK2X180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_2X_LF	NA	NA

Output Clock	Low-Frequency Mode		High-Frequency Mode	
	CLKIN Input	**CLK Output**	**CLKIN Input**	**CLK Output**
CLKDV	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_DV_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_DV_HF
CLKFX,CLKFX180	CLKIN_FREQ_FX_LF	CLKOUT_FREQ_FX_LF	CLKIN_FREQ_FX_HF	CLKOUT_FREQ_FX_HF

BQR2V3000 DCMs are placed on the top and the bottom of each block RAM and multiplier column. The number of DCMs as shown in Table 21.

Table 21 DCM Organization

Device	Columns	DCMs
BQR2V3000	6	12

3.2.6 .Global Clock Multiplexer Buffers

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clocking schemes.

BQR2V3000 have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads are on the top edge of the device, in the middle of the array, and eight are on the bottom edge, as illustrated in Figure 33.

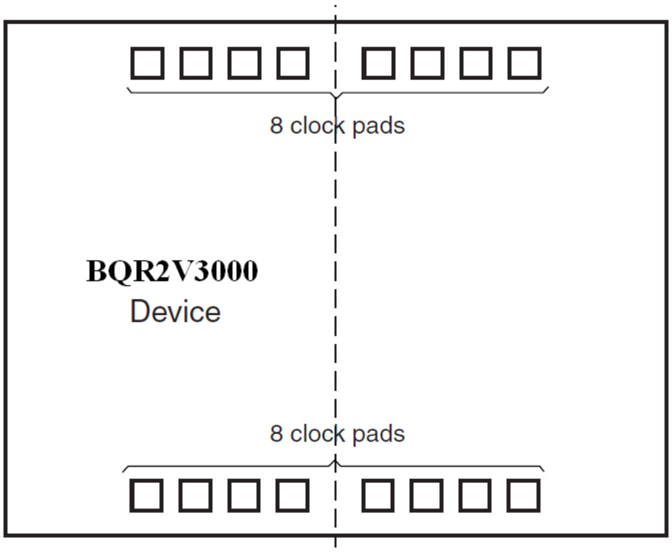


Figure 33 BQR2V3000 Clock Pads

Each global clock buffer can be driven by either the clock pad to distribute a clock directly to the device, or the Digital Clock Manager (DCM).Each global clock buffer can also be driven by local interconnects. The DCM has clock output(s) that can be connected to global clock buffer inputs, as shown in Figure 34.

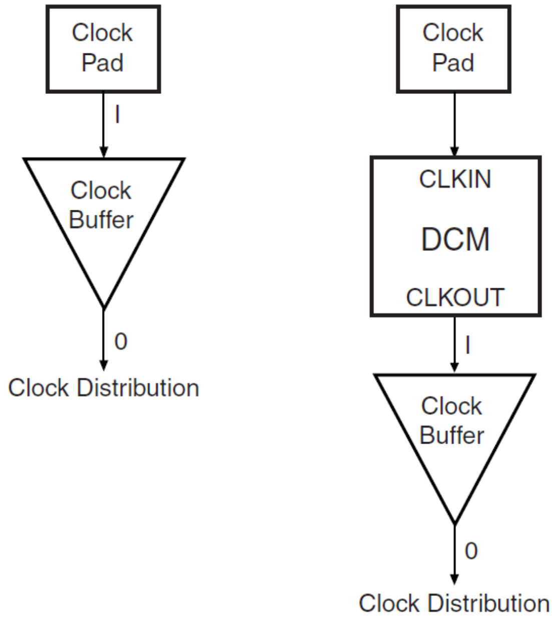


Figure 34 BQR2V3000 Clock Distribution Configurations

Global clock buffers are used to distribute the clock to some or all synchronous logic elements (such as registers in CLBs and IOBs, and SelectRAM blocks).Eight global clocks can be used in each quadrant of the BQR2V3000 device. Designers should consider the clock distribution detail of the device prior to pin-locking and floorplanning.Figure 35 shows clock distribution in BQR2V3000.

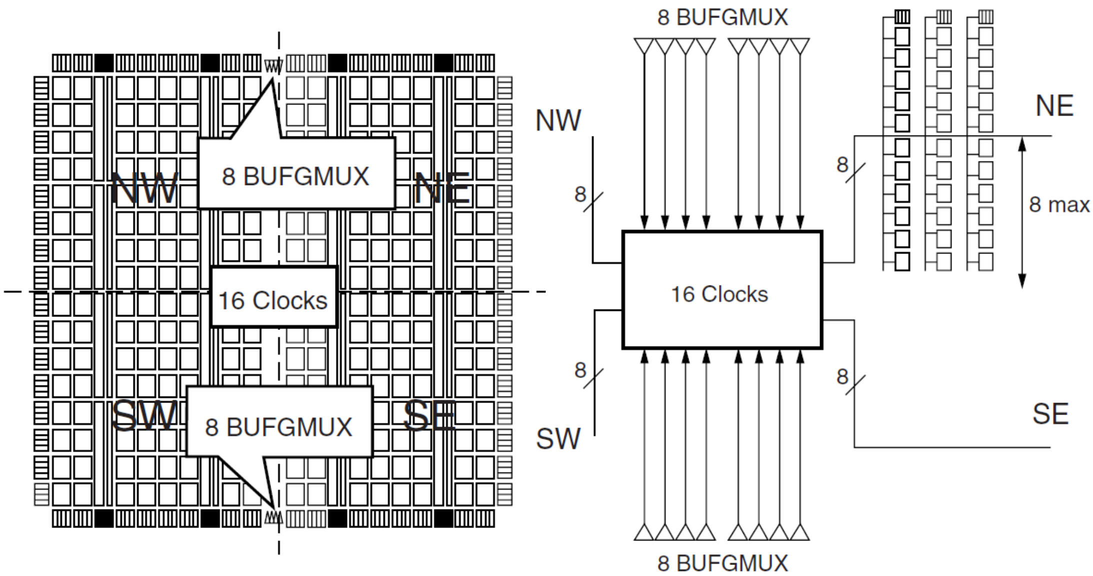


Figure 35 BQR2V3000 Clock Distribution

In each quadrant, up to eight clocks are organized in clock rows. A clock row supports up to 16 CLB rows (eight up and eight down). For the largest devices a new clock row is added, as necessary.

To reduce power consumption, any unused clock branches remain static.

Global clocks are driven by dedicated clock buffers (BUFG),which can also be used to gate the clock (BUFGCE) or to multiplex between two independent clock inputs (BUFGMUX).

The most common configuration option of this element is as a buffer. A BUFG function in this (global buffer) mode, is shown in Figure 36.

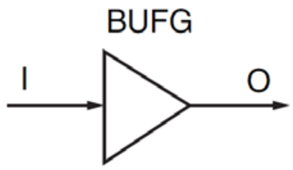


Figure 36 BQR2V3000 BUFG Function

The BQR2V3000 global clock buffer BUFG can also be configured as a clock enable/disable circuit (Figure 37), as well as a two-input clock multiplexer (Figure 38). A functional description of these two options is provided below. Each of them can be used in either of two modes,selected by configuration: rising clock edge or falling clock edge.

This section describes the rising clock edge option. For the opposite option, falling clock edge, just change all "rising" references to "falling" and all "High" references to "Low",except for the description of the CE or S levels. The rising clock edge option uses the BUFGCE and BUFGMUX primitives. The falling clock edge option uses the BUFGCE_1 and BUFGMUX_1 primitives.

BUFGCE

If the CE input is active (High) prior to the incoming rising clock edge, this Low-to-High-to-Low clock pulse passes through the clock buffer. Any level change of CE during the incoming clock High time has no effect.

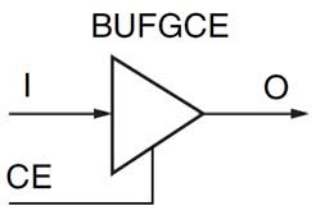


Figure 37 BQR2V3000 BUFGCE Function

If the CE input is inactive (Low) prior to the incoming rising clock edge, the following clock pulse does not pass through the clock buffer, and the output stays Low. Any level change of CE during the incoming clock High time has no effect. CE must not change during a short setup window just prior to the rising clock edge on the BUFGCE input I. Violating this setup time requirement can result in an undefined runt pulse output.

BUFGMUX

BUFGMUX can switch between two unrelated, even asynchronous clocks. Basically, a Low on S selects the I0 input, and a High on S selects the I1 input. Switching from one clock to the other is done in such a way that the output High and Low time is never shorter than the shortest High or Low time of either input clock. As long as the presently selected clock is High, any level change of S has no effect.

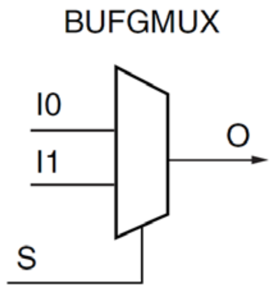


Figure 38 BQR2V3000 BUFGMUX Function

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock, that is, prior to the rising edge of the BUFGMUX output O. Violating this setup time requirement can result in an undefined runt pulse output.

BQR2V3000 have 16 global clock multiplexer buffers. Figure 39 shows a switchover from CLK0 to CLK1. In Figure 39:

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.

No glitches or short pulses can appear on the output.

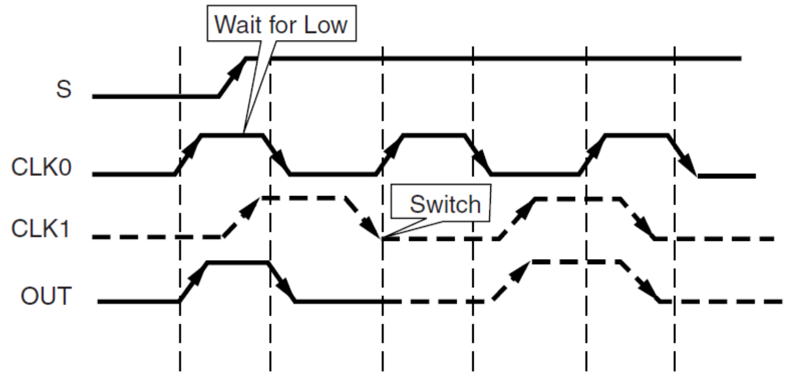


Figure 39 Clock Multiplexer Waveform Diagram

3.2.7 Routing Resources

Local and global BQR2V3000 routing resources are optimized for speed and timing predictability, as well as to facilitate cores implementation. BQR2V3000 Active Interconnect Technology is a fully buffered programmable routing matrix.All routing resources are segmented to offer the advantages of a hierarchical solution. BQR2V3000 logic features like CLBs,IOBs, block RAM, multipliers, and DCMs are all connected to an identical switch matrix for access to global routing resources, as shown in Figure 40.

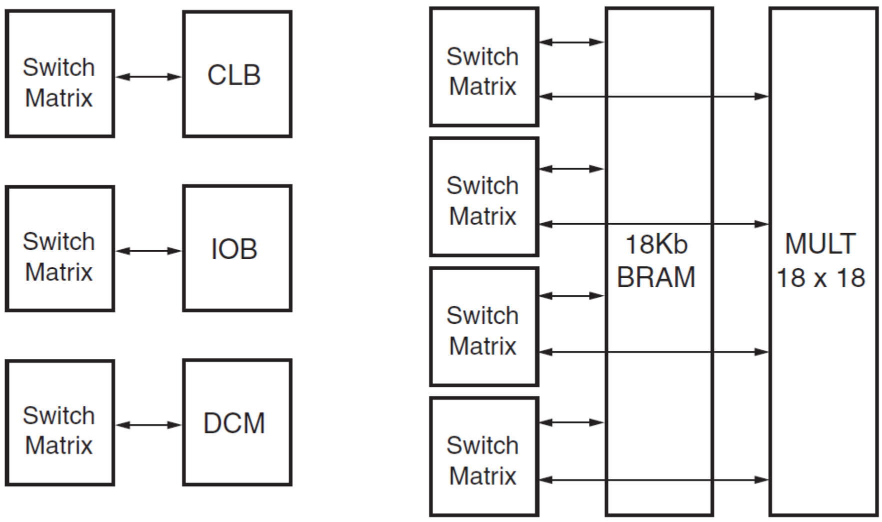


Figure 40 Active Interconnect Technology

Each BQR2V3000 device can be represented as an array of switch matrices with logic blocks attached, as illustrated in Figure 41.

Place-and-route software takes advantage of this regular array to deliver optimum system performance and fast compile times. The segmented routing resources are essential to guarantee IP cores portability and to efficiently handle an incremental design flow that is based on modular implementations. Total design time is reduced due to fewer and shorter design iterations.

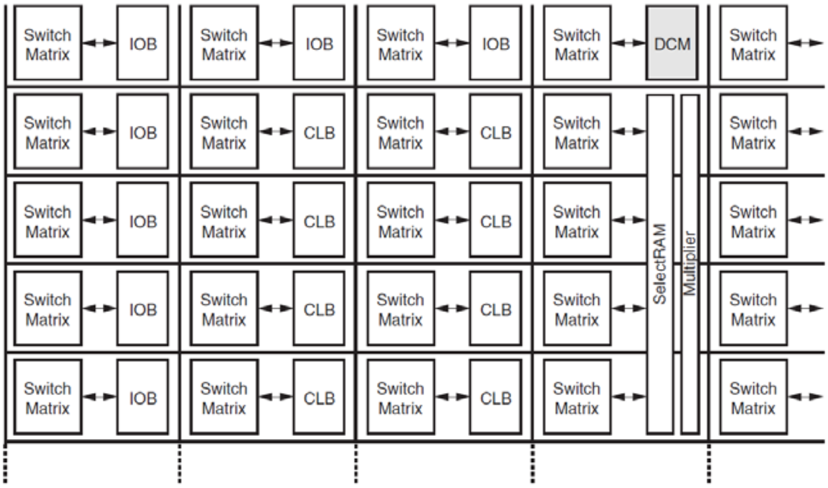


Figure 41 Routing Resource

Hierarchical Routing Resources

Most BQR2V3000 signals are routed using the global routing resources, which are located in horizontal and vertical routing channels between each switch matrix.As shown in Figure 42, BQR2V3000 device have fully buffered programmable interconnections, with a number of resources counted between any two adjacent switch matrix rows or columns. Fanout has minimal impact on the performance of each net. In Figure 42:

•Long lines are bidirectional wires that distribute signals across the device. Vertical and horizontal long lines span the full height and width of the device.

• Hex lines route signals to every third or sixth block away in all four directions. Organized in a staggered pattern, hex lines can only be driven from one end.Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source).

• Double lines route signals to every first or second block away in all four directions. Organized in a staggered pattern, double lines can be driven only at their endpoints. Double-line signals can be accessed either at the endpoints or at the midpoint (one block from thesource).

• Direct connect lines route signals to neighboring blocks: vertically, horizontally, and diagonally.

• Fast connect lines are the internal CLB local interconnections from LUT outputs to

LUT inputs.

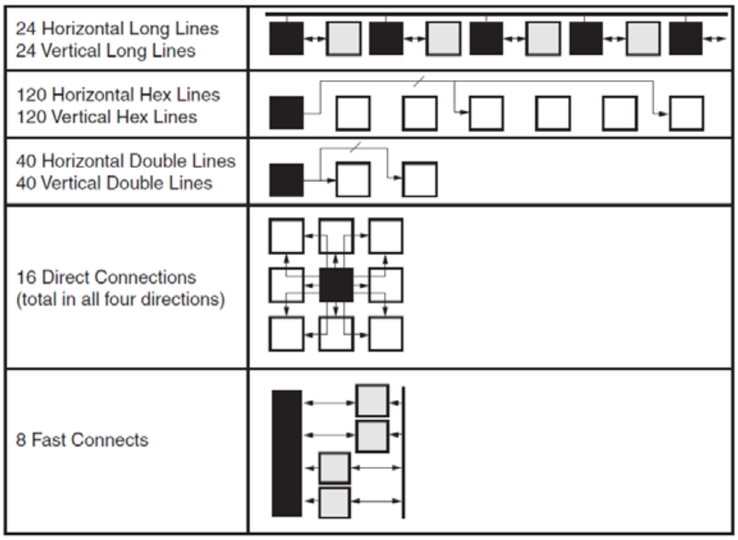


Figure 42 Hierachical Routing Resources

Dedicated Routing

In addition to the global and local routing resources,dedicated signals are available:

• There are eight global clock nets per quadrant .

• Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row.

• Two dedicated carry-chain resources per slice column (two per CLB column) propagate carry-chain MUXCY output signals vertically to the adjacent slice.

• One dedicated SOP chain per slice row (two per CLB row) propagates ORCY output logic signals horizontally to the adjacent slice.

• One dedicated shift chain per CLB connects the output of LUTs in shift-register mode to the input of the next LUT in shift-register mode (vertically) inside the CLB.

3.2.8 Boundary Scan

Boundary-scan instructions and associated data registers support a standard methodology for accessing and configuring BQR2V3000 device that complies with IEEE standards 1149.1-1993 and 1532. A system mode and a test mode are implemented. In system mode, a BQR2V3000 device performs its intended mission even while executing non-test boundary-scan instructions. In test mode, boundary-scan test instructions control the I/O pins for testing purposes. The BQR2V3000 Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

3.3 Combinations and Maximum Number of Available I/Os

Table 22 Combinations and Maximum Number of Available I/Os

Package	Available I/Os
CCGA717	516

4. Configuration

The BQR2V3000 device are configured by loading application-specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are dedicated, while others can be re-used as general purpose inputs and outputs once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M2, M1, and M0 are dedicated pins. An additional pin, HSWAP_EN, is used in conjunction with the mode pins to select whether user I/O pins have pull-ups during configuration. By default, HSWAP_EN is tied High (internal pull-up), which shuts off the pull-ups on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. Other dedicated pins are CCLK (the configuration clock pin), DONE, PROG_B, and the boundary-scan pins: TDI, TDO, TMS, and TCK. Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or an input accepting an externally generated clock. The configuration pins and boundary-scan pins are independent of the VCCO. The auxiliary power supply (VCCAUX) of 3.3V is used for these pins. All configuration pins are LVTTL 12 mA.

A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected, then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the boundary-scan related pins. The persist feature is valuable in applications which employ partial reconfiguration or reconfiguration on the fly.

4.1 Configuration Modes

BQR2V3000 supports the following five configuration modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532/IEEE 1149)

4.2 Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

Slave-serial mode is selected by applying <111> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

4.3 Master-Serial Mode

In master-serial mode, the CCLK pin is an output pin. It is the BQR2V3000 device that drives the configuration clock on the CCLK pin to a BMTI or Xilinx Serial PROM, which in turn feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

4.4 Slave SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the BQR2V3000 device with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, an active-Low Chip Select (CS_B) signal, and a Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback using the persist option.

Multiple BQR2V3000 can be configured using the SelectMAP mode, and can be made to start-up simultaneously. To configure multiple device in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the device in parallel. The individual device are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.

4.5 Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the BQR2V3000. Timing is similar to the Slave SerialMAP mode except that CCLK is supplied by the BQR2V3000.

4.6 Boundary-Scan (JTAG, IEEE 1532) Mode

In boundary-scan mode, dedicated pins are used for configuring the BQR2V3000 device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). BQR2V3000 device configuration using boundary scan is compliant with IEEE 1149.1-1993 standard and the new

IEEE 1532 standard for In-System Configurable (ISC) device. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) device is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes.

Table 23 BQR2V3000 Configuration Mode Pin Settings

Configuration Mode(1)	**M2**	**M1**	**M0**	**CCLK Direction**	**Data Width**	**Serial Dout(2)**
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary Scan	1	0	1	N/A	1	No

Notes:

1. The HSWAP_EN pin controls the pullups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pullups are used.

2. Daisy chaining is possible only in modes where Serial DOUT is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream device.

4.7 Configuration Sequence

The configuration of BQR2V3000 device is a three-phase process after Power On Reset or POR. POR occurs when VCCINT is greater than 1.2V, VCCAUX is greater than 2.5V, and VCCO (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a BQR2V3000 device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple device all going High, forcing the device to start synchronously. The sequence can also be paused at any stage, until lock has been achieved on any or all DCMs, as well as the DCI.

4.8 Readback

In this mode, configuration data from the BQR2V3000 device can be read back. Readback is supported only in the SelectMAP (master and slave) and Boundary Scan modes.

Along with the configuration data, it is possible to read back the contents of all registers, distributed SelectRAM, and block RAM resources. This capability is used for real-time debugging.

4.9 Bitstream Encryption

BQR2V3000 device have an on-chip decryptor using one or two sets of three keys for triple-key Data Encryption Standard (DES) operation. Xilinx software tools offer an optional encryption of the configuration data (bitstream) with a triple-key DES determined by the designer.

The keys are stored in the FPGA by JTAG instruction an retained by a battery connected to the VBATT pin, when the device is not powered. BQR2V3000 device can be configured with the corresponding encrypted bitstream, using any of the configuration modes described previously.

4.10 Partial Reconfiguration

Partial reconfiguration of BQR2V3000 device can be accomplished in either

Slave SelectMAP mode or Boundary-Scan mode. Instead of resetting the chip and doing a full configuration, new data is loaded into a specified area of the chip, while the rest of the chip remains in operation. Data is loaded on a column basis, with the smallest load unit being a configuration "frame" of the bitstream (device size dependent).

Partial reconfiguration is useful for applications that require different designs to be loaded into the same area of a chip, or that require the ability to change portions of a design without having to reset or reconfigure the entire chip.

5. Electrical Characteristics

BQR2V3000 DC and AC characteristics are specified for military and space grade.All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

5.1 DC Characteristics

Table 24 Absolute Maximum Ratings

Symbol	Description(1)		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.65	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 4.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 4.0	V
V_{BATT}	Key memory battery backup supply	–0.5 to 4.0	V
V_{REF}	Input reference voltage	–0.5 to V_{CCO} + 0.5	V
V_{IN}(2)	Input voltage relative to GND (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state output (user and dedicated I/Os)	–0.5 to 4.0	V
T_{STG}	Storage temperature (ambient)	–65 to +150	℃
T_{SOL}	Maximum soldering temperature	+220	℃
T_J	Operating junction temperature	+145	℃

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to

Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

2. Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

Table 25 Recommended Operating Conditions

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_C = –55°C to +125°C	1.425	1.575	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_C = –55°C to +125°C	3.135	3.465	V
V_{CCO}	Supply voltage relative to GND, T_C = –55°C to +125°C	1.2	3.6	V
V_{BATT}	Battery voltage relative to GND, T_C = –55°C to +125°C	1.0	3.6	V

Notes:

1. If battery is not used, connect V_{BATT} to GND or V_{CCAUX}.

2. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.

3. The thresholds for Power On Reset are V_{CCINT} > 1.2V, V_{CCAUX} > 2.5V, and V_{CCO} (Bank 4) > 1.5 V.

4. Limit the noise at the power supply to be within 200 mV peak-to-peak.

Table 26 DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage	All	1.2		V
V_{DRI}	Data Retention V_{CCAUX} Voltage	All	2.5		V
I_{REF}	V_{REF} current per bank	All	–10	+10	µA
I_L	Input leakage current	All	–10	+10	µA
C_{IN}	Input capacitance	All		20	pF
I_{RPU}	Pad pull-up (when selected) @ Vin = 0 V, VCCO = 3.3 V (sample tested)	All	Note 1	250	µA
I_{RPD}	Pad pull-down (when selected) @ Vin = 3.6 V (sample tested)	All	Note 1	250	µA
I_{BATT}	Battery supply current	All		100	nA

Notes:

1. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Table 27 Quiescent Supply Current

Symbo	Description	Min	Typical	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current(3)	–	100	0.50	A
I_{CCOQ}	Quiescent V_{CCO} supply current(1,2)	–	1.0	6.25	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current(1,2)	–	10	95	mA

Notes:

1. With no output current loads and no active input pull-up resistors. All I/O pins are 3-stated and floating.
2. If DCI or differential signaling is used, more accurate values can be obtained by using the Power Estimator or XPOWER.
3. Quiescent V_{CCINT} supply current may attain hundreds milliampere at high temperature, which should be considered when supply system is designing.

5.2 Power-On Power Supply Requirements

BQR2V3000 requires a certain amount of supply current during power-on to ensure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply.

The VCCINT, VCCAUX, and VCCO power supplies shall each ramp on no faster than 200 μs and no slower than 50 ms. Ramp on is defined as: 0 VDC to minimum supply voltages.

Table 28 shows the minimum current required by BQR2V3000 device for proper power on and configuration.

Power supplies can be turned on in any sequence. If any VCCO bank powers up before VCCAUX, then each bank draws up to 300 mA, worst case, until the VCCAUX powers on. This does not harm the device. If the current is limited to the minimum value above, or larger, the device powers on properly after all three supplies have passed through their power on reset threshold voltages.

Note: The 300 mA is transient current (peak). It eventually disappears even if V_{CCAUX} does not power up.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

Table 28 Maximum Power On Current Required for BQR2V3000 Device

Current	Device (mA)
	BQR2V3000
$I_{CCINTMAX}$	1300
$I_{CCAUXMAX}$	95
I_{CCOMAX}	6.25

Notes:

1. Values specified for power on current parameters are Military Grade.

2. I_{CCOMAX} values listed here apply to the entire device (all banks).

5.3 General Power Supply Requirements

Proper decoupling of all FPGA power supplies is essential. Consult Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors, for detailed information on power distribution system design.

Quiescent VCCINT supply current may attain hundreds milliampere at high temperature, which should be considered when supply system is designing.

VCCAUX powers critical resources in the FPGA. Thus, VCCAUX is especially susceptible to power supply noise.

Changes in VCCAUX voltage outside of 200 mV peak to peak should take place at a rate no faster than 10 mV per millisecond.

VCCAUX can share a power plane with 3.3V VCCO, but only if VCCO does not have excessive noise. Using simultaneously switching output (SSO) limits are essential for keeping power supply noise to a minimum.

5.4 DC Input and Output Levels

Values for VIL and VIH are recommended input voltages. Values for IOL and IOH are guaranteed over the recommended operating conditions at the VOL and VOH test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum VCCO with the respective VOL and VOH voltage levels shown. Other standards are sample tested.

5.5 LDT Differential Signal DC Specifications (LDT_25)

Table 29 LDT DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage	V_{OD}	R_T = 100Ω across Q and ~Q signals	500	600	700	mV
Change in V_{OD} Magnitude	ΔV_{OD}		–15		15	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and ~Q signals	560	600	640	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		–15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV
Change in V_{ID} Magnitude	ΔV_{ID}		–15		15	mV
Input Common Mode Voltage	V_{ICM}		500	600	700	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		–15		15	mV

5.6 LVDS DC Specifications (LVDS_33 and LVDS_25)

Table 30 LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and Q	V_{OH}	R_T = 100 Ω across Q and ~Q signals			1.575	V
Output Low Voltage for Q and Q	V_{OL}	R_T = 100 Ω across Q and ~Q signals	0.925			V
Differential Output Voltage (Q – Q), Q = High (Q – Q), Q = High	V_{ODIFF}	R_T = 100 Ω across Q and ~Q signals	250	350	400	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and ~Q signals	1.125	1.2	1.375	V
Differential Input Voltage (Q – Q), Q = High (Q – Q), Q = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350	0.2	1.25	V_{CCO} – 0.5	V

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
		mV				

5.7 Extended LVDS DC Specifications (LVDSEXT_33 and LVDSEXT_25)

Table 31 Extended LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and Q	V_{OH}	R_T = 100 Ω across Q and ~Q signals			1.785	V
Output Low Voltage for Q and Q	V_{OL}	R_T = 100 Ω across Q and ~Q signals	0.705			V
Differential Output Voltage (Q – Q), Q = High (Q – Q), Q = High	V_{ODIFF}	R_T = 100 Ω across Q and ~Q signals	440		820	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and ~Q signals	1.125	1.2	1.375	V
Differential Input Voltage (Q – Q), Q = High (Q – Q), Q = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	V_{CCO} – 0.5	V

5.8 LVPECL DC Specifications

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The VOH levels are 200mV below standard LVPECL levels and are compatible with device tolerant of lower common-mode ranges. Table 32 summarizes the DC output specifications of LVPECL.

Table 32 LVPECL DC Specifications

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V

V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

6. Pin Definitions

Table 33 provides a description of each pin type listed in BQR2V3000 pinout tables.

Table 33 BQR2V3000 Pin Definitions

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled IO_LXXY_#", where: • IO indicates a user I/O pin. • LXXY indicates a differential pair, with XX a unique pair in the bank and Y = P/N for the positive and negative sides of the differential pair. • # indicates the bank number (0 through 7).
Dual-Function Pins		
IO_LXXY_#/ZZZ		• The dual-function pins are labelled "IO_LXXY_#/ZZZ", where ZZZ can be one of the following pins: • Per Bank - VRP, VRN, or VREF • Globally - GCLKX(S/P), BUSY/DOUT, INIT_B, DIN/D0 – D7, RDWR_B, or CS_B
With /ZZZ		
DIN/D0, D1, D2, D3, D4, D5, D6, D7	Input/Output	• In SelectMAP mode, D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. • In bit-serial modes, DIN (D0) is the single-data input. This pin becomes a user I/O afterconfiguration.
CS_B	Input	In SelectMAP mode, this is the active-Low Chip Select signal. This

Pin Name	Direction	Description
		pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-Low Write Enable signal. This pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	• In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. This pin becomes a user I/O after configuration, unless the SelectMAP port is retained. • In bit-serial modes, DOUT provides preamble and configuration data to downstream device in a daisy chain. This pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. This pin becomes a user I/O after configuration.
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
VRP	Input	This pin is for the DCI voltage reference resistor of the P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of the N transistor (per bank).
ALT_VRP	Input	This is the alternative pin for the DCI voltage reference resistor of the P transistor.
ALT_VRN	Input	This is the alternative pin for the DCI voltage reference resistor of the N transistor.
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins[(1)]		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the

Pin Name	Direction	Description
		configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection.
HSWAP_EN	Input	Enable I/O pullups during configuration.
TCK	Input	Boundary Scan Clock.
TDI	Input	Boundary Scan Data Input.
TDO	Output	Boundary Scan Data Output.
TMS	Input	Boundary Scan Mode Select.
PWRDWN_B	Input *(unsupported)*	Active Low power-down pin (unsupported). *Driving this pin Low can adversely affect device operation and configuration.* PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. (Do not connect if battery is not used.)
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).

7. Pinout Information and Package

As shown in Table 34, the BQR2V3000 device is available in the CCGA717 packages.

Table 34 BQR2V3000 packages

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
E14	I/O_L96P_0/GCLK4S	P8	I/O_L94N_7	AF13	I/O_L95P_5/GCLK4P	R24	I/O_L94P_3
F14	I/O_L96N_0/GCLK5P	P7	I/O_L94P_7	AG13	I/O_L95N_5/GCLK5S	R25	I/O_L94N_3
C14	I/O_L95P_0/GCLK6S	P6	I/O_L96N_7	AB14	I/O_L96P_5/GCLK6P	R26	I/O_L96P_3
C13	I/O_L95N_0/GCLK7P	P5	I/O_L96P_7	AC14	I/O_L96N_5/GCLK7S	R27	I/O_L96N_3
A13	I/O_L94P_0	R1	I/O_L96N_6	AA14	I/O_L96P_4/GCLK0P	P23	I/O_L96P_2
B13	I/O_L94N_0/VREF_0	R2	I/O_L96P_6	Y14	I/O_L96N_4/GCLK1S	P22	I/O_L96N_2
D13	I/O_L93P_0	P3	I/O_L94N_6	AG15	I/O_L95P_4/GCLK2P	P21	I/O_L94P_2
E13	I/O_L93N_0	R3	I/O_L94P_6	AF15	I/O_L95N_4/GCLK3S	P20	I/O_L94N_2
F13	I/O_L92P_0	R6	I/O_L93N_6/VREF_6	AE14	I/O_L94P_4	N27	I/O_L93P_2/VREF_2
G13	I/O_L92N_0	R5	I/O_L93P_6	AE15	I/O_L94N_4/VREF_4	N26	I/O_L93N_2
H13	I/O_L91P_0	R8	I/O_L91N_6	AD15	I/O_L93P_4	P25	I/O_L91P_2
J13	I/O_L91N_0/VREF_0	R7	I/O_L91P_6	AC15	I/O_L93N_4	N25	I/O_L91N_2
A12	I/O_L78P_0	T1	I/O_L78N_6	AA15	I/O_L92P_4	N23	I/O_L78P_2
B12	I/O_L78N_0	T2	I/O_L78P_6	AB15	I/O_L92N_4	N22	I/O_L78N_2
D12	I/O_L76P_0	R4	I/O_L76N_6	Y15	I/O_L91P_4	N21	I/O_L76P_2
E12	I/O_L76N_0	T4	I/O_L76P_6	W15	I/O_L91N_4/VREF_4	N20	I/O_L76N_2
J12	I/O_L75P_0/VREF_0	T6	I/O_L75N_6/VREF_6	AG16	I/O_L78P_4	M27	I/O_L75P_2/VREF_2

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
H12	I/O_L75N_0	T5	I/O_L75P_6	AF16	I/O_L78N_4	M26	I/O_L75N_2
A11	I/O_L73P_0	R9	I/O_L73N_6	AD16	I/O_L76P_4	N24	I/O_L73P_2
B11	I/O_L73N_0	T9	I/O_L73P_6	AC16	I/O_L76N_4	M24	I/O_L73N_2
C11	I/O_L72P_0	U1	I/O_L72N_6	W16	I/O_L75P_4/VREF_4	M23	I/O_L72P_2
D11	I/O_L72N_0	U2	I/O_L72P_6	Y16	I/O_L75N_4	M22	I/O_L72N_2
F12	I/O_L70P_0	U3	I/O_L70N_6	AG17	I/O_L73P_4	N19	I/O_L70P_2
F11	I/O_L70N_0	U4	I/O_L70P_6	AF17	I/O_L73N_4	M19	I/O_L70N_2
H11	I/O_L69P_0/VREF_0	U7	I/O_L69N_6/VREF_6	AE17	I/O_L72P_4	L27	I/O_L69P_2/VREF_2
G11	I/O_L69N_0	U6	I/O_L69P_6	AD17	I/O_L72N_4	L26	I/O_L69N_2
A10	I/O_L67P_0	T8	I/O_L67N_6	AB16	I/O_L70P_4	L25	I/O_L67P_2
B10	I/O_L67N_0	U8	I/O_L67P_6	AB17	I/O_L70N_4	L24	I/O_L67N_2
C10	I/O_L54P_0	V1	I/O_L54N_6	Y17	I/O_L69P_4/VREF_4	L22	I/O_L54P_2
D10	I/O_L54N_0	V2	I/O_L54P_6	AA17	I/O_L69N_4	L21	I/O_L54N_2
E10	I/O_L52P_0	V3	I/O_L52N_6	AG18	I/O_L67P_4	M20	I/O_L52P_2
F10	I/O_L52N_0	V4	I/O_L52P_6	AF18	I/O_L67N_4	L20	I/O_L52N_2
H10	I/O_L51P_0/VREF_0	V6	I/O_L51N_6/VREF_6	AE18	I/O_L54P_4	K27	I/O_L51P_2/VREF_2
G10	I/O_L51N_0	V5	I/O_L51P_6	AD18	I/O_L54N_4	K26	I/O_L51N_2
A9	I/O_L49P_0	V8	I/O_L49N_6	AC18	I/O_L52P_4	K25	I/O_L49P_2
A8	I/O_L49N_0	V7	I/O_L49P_6	AB18	I/O_L52N_4	K24	I/O_L49N_2
B9	I/O_L30P_0	W2	I/O_L48N_6	Y18	I/O_L51P_4/VREF_4	K23	I/O_L48P_2
C9	I/O_L30N_0	W3	I/O_L48P_6	AA18	I/O_L51N_4	K22	I/O_L48N_2

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
D9	I/O_L28P_0	W4	I/O_L46N_6	AF19	I/O_L49P_4	K21	I/O_L46P_2
E9	I/O_L28N_0	W5	I/O_L46P_6	AE19	I/O_L49N_4	K20	I/O_L46N_2
G9	I/O_L27P_0/VREF_0	W7	I/O_L45N_6/VREF_6	AD19	I/O_L30P_4	J26	I/O_L45P_2/VREF_2
F9	I/O_L27N_0	W6	I/O_L45P_6	AC19	I/O_L30N_4	J25	I/O_L45N_2
J9	I/O_L25P_0	W9	I/O_L43N_6	AA19	I/O_L28P_4	J24	I/O_L43P_2
H9	I/O_L25N_0	W8	I/O_L43P_6	AB19	I/O_L28N_4	J23	I/O_L43N_2
A7	I/O_L24P_0	W1	I/O_L28N_6	AG19	I/O_L27P_4/VREF_4	J27	I/O_L30P_2
B7	I/O_L24N_0	Y1	I/O_L28P_6	AG20	I/O_L27N_4	H27	I/O_L30N_2
C8	I/O_L22P_0	Y3	I/O_L27N_6/VREF_6	AD20	I/O_L25P_4	H25	I/O_L28P_2
C7	I/O_L22N_0	Y4	I/O_L27P_6	AC20	I/O_L25N_4	H24	I/O_L28N_2
E8	I/O_L21P_0/VREF_0	Y6	I/O_L25N_6	AA20	I/O_L24P_4	J22	I/O_L27P_2/VREF_2
F8	I/O_L21N_0	Y5	I/O_L25P_6	AB20	I/O_L24N_4	H22	I/O_L27N_2
D8	I/O_L19P_0	AA2	I/O_L24N_6	AG21	I/O_L22P_4	J21	I/O_L25P_2
E7	I/O_L19N_0	AA3	I/O_L24P_6	AF21	I/O_L22N_4	H21	I/O_L25N_2
A6	I/O_L06P_0	AA6	I/O_L22N_6	AE20	I/O_L21P_4/VREF_4	G26	I/O_L24P_2
B6	I/O_L06N_0	AA5	I/O_L22P_6	AE21	I/O_L21N_4	G25	I/O_L24N_2
D6	I/O_L05P_0	AA1	I/O_L21N_6/VREF_6	AB21	I/O_L19P_4	H23	I/O_L22P_2
E6	I/O_L05N_0	AB1	I/O_L21P_6	AC21	I/O_L19N_4	G23	I/O_L22N_2
A5	I/O_L04P_0	AB2	I/O_L19N_6	AG22	I/O_L06P_4	G27	I/O_L21P_2/VREF_2
B5	I/O_L04N_0/VREF_0	AB3	I/O_L19P_6	AF22	I/O_L06N_4	F27	I/O_L21N_2
C6	I/O_L03P_0/VRN_0	AB4	I/O_L06N_6	AE22	I/O_L05P_4/VRN_4	F26	I/O_L19P_2

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
C5	I/O_L03N_0/VRP_0	AB5	I/O_L06P_6	AD22	I/O_L05N_4/VRP_4	F25	I/O_L19N_2
A4	I/O_L02P_0	AC1	I/O_L04N_6	AG23	I/O_L04P_4	F24	I/O_L06P_2
B4	I/O_L02N_0	AC2	I/O_L04P_6	AF23	I/O_L04N_4/VREF_4	F23	I/O_L06N_2
A3	I/O_L01P_0	AC3	I/O_L03N_6/VREF_6	AE23	I/O_L03P_4/D3/ALT_VRN_4	E27	I/O_L04P_2
B3	I/O_L01N_0	AC4	I/O_L03P_6	AD23	I/O_L03N_4/D2/ALT_VRP_4	E26	I/O_L04N_2
G8	DXN	AD2	I/O_L02N_6/VRP_6	AG24	I/O_L02P_4/D1	E25	I/O_L03P_2/VREF_2
F7	DXP	AD3	I/O_L02P_6/VRN_6	AF24	I/O_L02N_4/D0/DIN	E24	I/O_L03N_2
D5	HSWAP_EN	AD1	I/O_L01N_6	AG25	I/O_L01P_4/INIT_B	D26	I/O_L02P_2/VRN_2
C4	PROG_B	AE1	I/O_L01P_6	AF25	I/O_L01N_4/BUSY/DOUT	D25	I/O_L02N_2/VRP_2
H7	TDI	Y7	M1	AC22	DONE	D27	I/O_L01P_2
D3	I/O_L01N_7	AC6	M0	AE24	PWRDWN_B	C27	I/O_L01N_2
D2	I/O_L01P_7	AE4	M2	AA22	CCLK	G22	TDO
E4	I/O_L02N_7/VRP_7	AF3	I/O_L01P_5/CS_B	AD25	I/O_L01P_3	G20	TCK
E3	I/O_L02P_7/VRN_7	AG3	I/O_L01N_5/RDWR_B	AD26	I/O_L01N_3	F21	TMS
C1	I/O_L03N_7	AF4	I/O_L02P_5/D7	AE27	I/O_L02P_3/VRN_3	D23	VBATT
D1	I/O_L03P_7/VREF_7	AG4	I/O_L02N_5/D6	AD27	I/O_L02N_3/VRP_3	B25	I/O_L01P_1
E2	I/O_L04N_7	AD5	I/O_L03P_5/D5/ALT_VRN_5	AC24	I/O_L03P_3	A25	I/O_L01N_1
E1	I/O_L04P_7	AE5	I/O_L03N_5/D4/ALT_VRP_5	AC25	I/O_L03N_3/VREF_3	B24	I/O_L02P_1
F5	I/O_L06N_7	AF5	I/O_L04P_5/VREF_5	AC26	I/O_L04P_3	A24	I/O_L02N_1
F4	I/O_L06P_7	AG5	I/O_L04N_5	AC27	I/O_L04N_3	B23	I/O_L03P_1/VRN_1
G6	I/O_L19N_7	AD6	I/O_L05P_5/VRN_5	AB23	I/O_L06P_3	A23	I/O_L03N_1/VRP_1

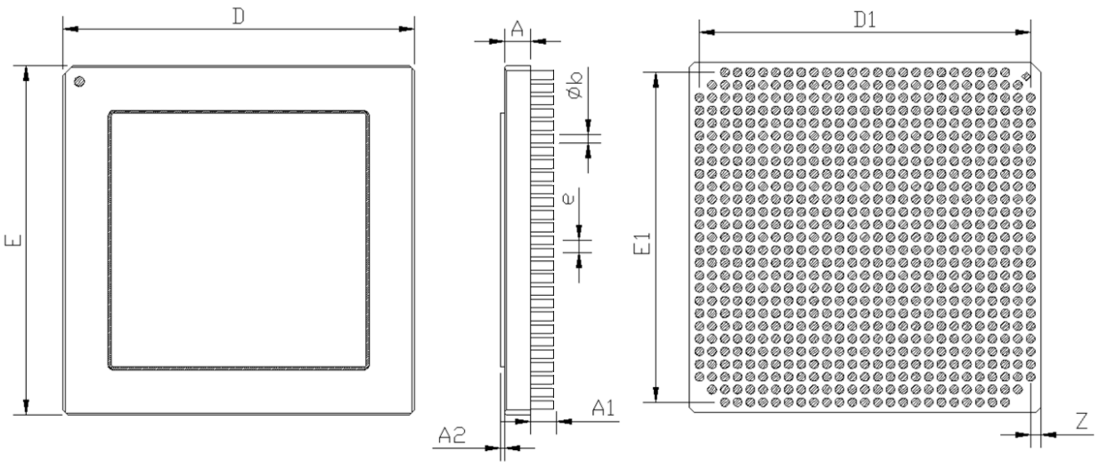
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
G5	I/O_L19P_7	AE6	I/O_L05N_5/VRP_5	AB24	I/O_L06N_3	E22	I/O_L04P_1/VREF_1
F3	I/O_L21N_7	AF6	I/O_L06P_5	AB25	I/O_L19P_3	D22	I/O_L04N_1
F2	I/O_L21P_7/VREF_7	AG6	I/O_L06N_5	AB26	I/O_L19N_3	C23	I/O_L05P_1
G3	I/O_L22N_7	AB7	I/O_L19P_5	AA25	I/O_L21P_3	C22	I/O_L05N_1
G2	I/O_L22P_7	AC7	I/O_L19N_5	AA26	I/O_L21N_3/VREF_3	B22	I/O_L06P_1
F1	I/O_L24N_7	AF7	I/O_L21P_5	AB27	I/O_L22P_3	A22	I/O_L06N_1
G1	I/O_L24P_7	AG7	I/O_L21N_5/VREF_5	AA27	I/O_L22N_3	B21	I/O_L19P_1
J8	I/O_L25N_7	AA8	I/O_L22P_5	Y21	I/O_L24P_3	A21	I/O_L19N_1
J7	I/O_L25P_7	AB8	I/O_L22N_5	Y22	I/O_L24N_3	F20	I/O_L21P_1
H6	I/O_L27N_7	AC8	I/O_L24P_5	AA23	I/O_L25P_3	E20	I/O_L21N_1/VREF_1
H5	I/O_L27P_7/VREF_7	AD8	I/O_L24N_5	Y23	I/O_L25N_3	E21	I/O_L22P_1
J6	I/O_L28N_7	AE7	I/O_L25P_5	Y24	I/O_L27P_3	D20	I/O_L22N_1
J5	I/O_L28P_7	AE8	I/O_L25N_5	Y25	I/O_L27N_3/VREF_3	C21	I/O_L24P_1
H4	I/O_L30N_7	AA9	I/O_L27P_5	Y19	I/O_L28P_3	C20	I/O_L24N_1
H3	I/O_L30P_7	AB9	I/O_L27N_5/VREF_5	W19	I/O_L28N_3	J20	I/O_L25P_1
J4	I/O_L43N_7	AC9	I/O_L28P_5	W20	I/O_L43P_3	J19	I/O_L25N_1
K3	I/O_L43P_7	AD9	I/O_L28N_5	W21	I/O_L43N_3	G19	I/O_L27P_1
J3	I/O_L45N_7	AE9	I/O_L30P_5	W23	I/O_L45P_3	F19	I/O_L27N_1/VREF_1
J2	I/O_L45P_7/VREF_7	AF9	I/O_L30N_5	W24	I/O_L45N_3/VREF_3	E19	I/O_L28P_1
H1	I/O_L46N_7	AG8	I/O_L49P_5	W25	I/O_L46P_3	D19	I/O_L28N_1
J1	I/O_L46P_7	AG9	I/O_L49N_5	W26	I/O_L46N_3	C19	I/O_L30P_1

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
K8	I/O_L48N_7	Y10	I/O_L51P_5	Y27	I/O_L48P_3	B19	I/O_L30N_1
L8	I/O_L48P_7	Y9	I/O_L51N_5/VREF_5	W27	I/O_L48N_3	A20	I/O_L49P_1
K7	I/O_L49N_7	AB10	I/O_L52P_5	V20	I/O_L49P_3	A19	I/O_L49N_1
K6	I/O_L49P_7	AC10	I/O_L52N_5	V21	I/O_L49N_3	H18	I/O_L51P_1
L7	I/O_L51N_7	AD10	I/O_L54P_5	W22	I/O_L51P_3	H19	I/O_L51N_1/VREF_1
L6	I/O_L51P_7/VREF_7	AE10	I/O_L54N_5	V22	I/O_L51N_3/VREF_3	F18	I/O_L52P_1
K5	I/O_L52N_7	AF10	I/O_L67P_5	V23	I/O_L52P_3	E18	I/O_L52N_1
K4	I/O_L52P_7	AG10	I/O_L67N_5	V24	I/O_L52N_3	D18	I/O_L54P_1
K2	I/O_L54N_7	AA11	I/O_L69P_5	V26	I/O_L54P_3	C18	I/O_L54N_1
K1	I/O_L54P_7	AA10	I/O_L69N_5/VREF_5	V27	I/O_L54N_3	B18	I/O_L67P_1
L4	I/O_L67N_7	AD11	I/O_L70P_5	U20	I/O_L67P_3	A18	I/O_L67N_1
L3	I/O_L67P_7	AE11	I/O_L70N_5	U21	I/O_L67N_3	G17	I/O_L69P_1
L2	I/O_L69N_7	AF11	I/O_L72P_5	V25	I/O_L69P_3	G18	I/O_L69N_1/VREF_1
L1	I/O_L69P_7/VREF_7	AG11	I/O_L72N_5	U25	I/O_L69N_3/VREF_3	D17	I/O_L70P_1
M9	I/O_L70N_7	Y11	I/O_L73P_5	U26	I/O_L70P_3	C17	I/O_L70N_1
M8	I/O_L70P_7	Y12	I/O_L73N_5	U27	I/O_L70N_3	B17	I/O_L72P_1
M5	I/O_L72N_7	AB11	I/O_L75P_5	T19	I/O_L72P_3	A17	I/O_L72N_1
M4	I/O_L72P_7	AB12	I/O_L75N_5/VREF_5	T20	I/O_L72N_3	H17	I/O_L73P_1
M2	I/O_L73N_7	AC12	I/O_L76P_5	U22	I/O_L73P_3	H16	I/O_L73N_1
M1	I/O_L73P_7	AD12	I/O_L76N_5	T22	I/O_L73N_3	F17	I/O_L75P_1
M6	I/O_L75N_7	AF12	I/O_L78P_5	U24	I/O_L75P_3	F16	I/O_L75N_1/VREF_1

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
N5	I/O_L75P_7/VREF_7	AG12	I/O_L78N_5	T24	I/O_L75N_3/VREF_3	E16	I/O_L76P_1
N8	I/O_L76N_7	W12	I/O_L91P_5/VREF_5	T26	I/O_L76P_3	D16	I/O_L76N_1
N9	I/O_L76P_7	W13	I/O_L91N_5	T27	I/O_L76N_3	B16	I/O_L78P_1
N7	I/O_L78N_7	Y13	I/O_L92P_5	R19	I/O_L78P_3	A16	I/O_L78N_1
N6	I/O_L78P_7	AA13	I/O_L92N_5	R20	I/O_L78N_3	J16	I/O_L91P_1/VREF_1
N4	I/O_L91N_7	AB13	I/O_L93P_5	R21	I/O_L91P_3	J15	I/O_L91N_1
N3	I/O_L91P_7	AC13	I/O_L93N_5	R22	I/O_L91N_3	H15	I/O_L92P_1
N2	I/O_L93N_7	AD13	I/O_L94P_5/VREF_5	T23	I/O_L93P_3	G15	I/O_L92N_1
N1	I/O_L93P_7/VREF_7	AE13	I/O_L94N_5	R23	I/O_L93N_3/VREF_3	F15	I/O_L93P_1
E15	I/O_L93N_1	C15	I/O_L94N_1	A15	I/O_L95N_1/GCLK1P	G14	I/O_L96N_1/GCLK3P
D15	I/O_L94P_1/VREF_1	B15	I/O_L95P_1/GCLK0S	H14	I/O_L96P_1/GCLK2S	K13	VCCO_0
K12	VCCO_0	K11	VCCO_0	J11	VCCO_0	J10	VCCO_0
G12	VCCO_0	D7	VCCO_0	C12	VCCO_0	K17	VCCO_1
K16	VCCO_1	K15	VCCO_1	J18	VCCO_1	J17	VCCO_1
G16	VCCO_1	D21	VCCO_1	C16	VCCO_1	N18	VCCO_2
M25	VCCO_2	M21	VCCO_2	M18	VCCO_2	L19	VCCO_2
L18	VCCO_2	K19	VCCO_2	G24	VCCO_2	AA24	VCCO_3
V19	VCCO_3	U19	VCCO_3	U18	VCCO_3	T25	VCCO_3
T21	VCCO_3	T18	VCCO_3	R18	VCCO_3	AE16	VCCO_4
AD21	VCCO_4	AA16	VCCO_4	W18	VCCO_4	W17	VCCO_4
V17	VCCO_4	V16	VCCO_4	V15	VCCO_4	AE12	VCCO_5

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
AD7	VCCO_5	AA12	VCCO_5	W11	VCCO_5	W10	VCCO_5
V13	VCCO_5	V12	VCCO_5	V11	VCCO_5	AA4	VCCO_6
V9	VCCO_6	U10	VCCO_6	U9	VCCO_6	T10	VCCO_6
T7	VCCO_6	T3	VCCO_6	R10	VCCO_6	M10	VCCO_7
M7	VCCO_7	M3	VCCO_7	L10	VCCO_7	L9	VCCO_7
K9	VCCO_7	G4	VCCO_7	N10	VCCO_7	AF14	VCCAUX
AE26	VCCAUX	AE2	VCCAUX	P26	VCCAUX	P2	VCCAUX
C26	VCCAUX	C2	VCCAUX	B14	VCCAUX	V18	VCCINT
V14	VCCINT	V10	VCCINT	U17	VCCINT	U16	VCCINT
U15	VCCINT	U14	VCCINT	U13	VCCINT	U12	VCCINT
U11	VCCINT	T17	VCCINT	T11	VCCINT	R17	VCCINT
R11	VCCINT	P18	VCCINT	P17	VCCINT	P11	VCCINT
P10	VCCINT	N17	VCCINT	N11	VCCINT	M17	VCCINT
M11	VCCINT	L17	VCCINT	L16	VCCINT	L15	VCCINT
L14	VCCINT	L13	VCCINT	L12	VCCINT	L11	VCCINT
K18	VCCINT	K14	VCCINT	K10	VCCINT	AG14	GND
AF26	GND	AF20	GND	AF8	GND	AF2	GND
AE25	GND	AE3	GND	AD24	GND	AD14	GND
AD4	GND	AC23	GND	AC17	GND	AC5	GND
AB22	GND	AB6	GND	AA21	GND	AA7	GND
Y26	GND	Y20	GND	Y8	GND	Y2	GND
W14	GND	U23	GND	U5	GND	T16	GND
T15	GND	T14	GND	T13	GND	T12	GND
R16	GND	R15	GND	R14	GND	R13	GND
R12	GND	P27	GND	P24	GND	P19	GND

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
P16	GND	P15	GND	P14	GND	P13	GND
P12	GND	P9	GND	P4	GND	P1	GND
N16	GND	N15	GND	N14	GND	N13	GND
N12	GND	M16	GND	M15	GND	M14	GND
M13	GND	M12	GND	L23	GND	L5	GND
J14	GND	H26	GND	H20	GND	H8	GND
H2	GND	G21	GND	G7	GND	F22	GND
F6	GND	E23	GND	E17	GND	E11	GND
E5	GND	D24	GND	D14	GND	D4	GND
C25	GND	C3	GND	B26	GND	B20	GND
B8	GND	B2	GND	A14	GND	AC11	GND
C24	RSVD						



SYMBOL	MILLIMETERS (Unit:mm)		
	MIN	NOM	MAX
A	2.33	—	2.85
A1	2.0	2.2	2.4
A2	0.33	0.381	0.43
Z	0.66	—	1.32
D	34.65	—	35.35

SYMBOL	MILLIMETERS (Unit:mm)		
	MIN	NOM	MAX
E	34.65	—	35.35
D1	—	33.02	—
E1	—	33.02	—
e	—	1.27	—
ϕb	0.46	0.51	0.56
NOTE：Millimeters which is not mentioned above conform to Table 1 in GB/T1804-2000			

Appendix I Electrical performance characteristics

Table I-1： Electrical performance characteristics

Test	Symbol	Conditions Limits $1.425V \le V_{CCINT} \le 1.575V$, $3.0V \le V_{CCO} \le 3.6V$, $3.0V \le V_{CCAUX} \le 3.6V$, $-55℃ \le T_A \le 125℃$	Group A Subgroups	Limits		units
				Min	Max	
Data retention VCCINT voltage below which,configuration may be lost	V_{DRINT}		A1, A2, A3	1.2	—	V
Data retention VCCAUX voltage below which configuration may be lost	V_{DRI}		A1, A2, A3	2.5	—	V
High-level input voltage	V_{IH}	lvttl	A1, A2, A3	2.0	—	V
High-level input voltage	V_{IH}	lvdse	A1, A2, A3	1.425	—	V
High-level input voltage Low	V_{IH}	lvds	A1, A2, A3	0.25	—	V
High-level input voltage Med	V_{IH}	lvds	A1, A2, A3	1.625	—	V
High-level input voltage High	V_{IH}	lvds	A1, A2, A3	2.5	—	V
High-level input voltage	V_{IH}	ldt	A1, A2, A3	1.425	—	V
High-level input voltage Low	V_{IH}	sstl	A1, A2, A3	0.7	—	V
High-level input voltage Med	V_{IH}	sstl	A1, A2, A3	1.2	—	V

Test	Symbol	Conditions Limits 1.425V≤V_{CCINT}≤1.575 V，3.0V≤V_{CCO}≤3.6V，3.0V≤V_{CCAUX}≤3.6V，-55℃≤T_A≤125℃	Group A Subgroups	Limits		units
				Min	Max	
High-level input voltage High	V_{IH}	sstl	A1, A2, A3	1.7	—	V
Low-level input voltage	V_{IL}	lvttl	A1, A2, A3	—	0.8	V
Low-level input voltage	V_{IL}	lvdse	A1, A2, A3	—	1.025	V
Low-level input voltage Low	V_{IL}	lvds	A1, A2, A3	—	0.0	V
Low-level input voltage Med	V_{IL}	lvds	A1, A2, A3	—	1.375	V
Low-level input voltage High	V_{IL}	lvds	A1, A2, A3	—	2.25	V
Low-level input voltage	V_{IL}	ldt	A1, A2, A3	—	1.025	V
Low-level input voltage Low	V_{IL}	sstl	A1, A2, A3	—	0.5	V
Low-level input voltage Med	V_{IL}	sstl	A1, A2, A3	—	1.0	V
Low-level input voltage High	V_{IL}	sstl	A1, A2, A3	—	1.5	V
High-level output voltage	V_{OH}	I_{OH} = -1.75,-3.5,-4, -8 or –12mA (ttl2, ttl4,ttl8,ttl16,ttl24), V_{CCO} = 3.0V V_{CCINT} = 1.425V	A1, A2, A3	2.4	—	V
Low-level output voltage	V_{OL}	I_{OL} = 8, or 12 mA (ttl16, ttl24) V_{CCO} = 3.0V, V_{CCINT}=1.425V	A1, A2, A3	—	0.45	V

Test	Symbol	Conditions Limits $1.425V \le V_{CCINT} \le 1.575$ V，$3.0V \le V_{CCO} \le 3.6V$，$3.0V \le V_{CCAUX} \le 3.6V$，$-55℃ \le T_A \le 125℃$	Group A Subgroups	Limits		units
				Min	Max	
Quiescent VCCINT Supply current	I_{CCINTQ}		A1, A2, A3	—	500	mA
Quiescent VCCO Supply current	I_{CCOQ}		A1, A2, A3	—	6.25	mA
Quiescent VCCAUX Supply current	I_{CCAUXQ}		A1, A2, A3	—	95	mA
Input or output leakage current	I_L		A1, A2, A3	-10	10	μA
VREF current per bank	I_{REF}		A1, A2, A3	-10	10	μA
Pad pull-up (when selected)	I_{RPU}	V_{IN} = 0V V_{CCO} = 3.3 V	A1, A2, A3	—	0.25	mA
Pad pull-down (when selected)	I_{RPD}	V_{IN} = 3.6V V_{CCO} = 3.6 V	A1, A2, A3	—	0.25	mA
Battery supply current	I_{BATT}		A1, A2, A3		100	nA
Minimum required current supply	$I_{CCINTMIN}$		A1, A2, A3	1300		mA
Minimum required current supply	$I_{CCAUXMIN}$		A1, A2, A3	95		mA
Minimum required current supply	I_{CCOMIN}		A1, A2, A3	6.25		mA
Functional test	f		A7, A8A, A8B	—	—	—

Test	Symbol	Conditions Limits 1.425V≤V_{CCINT}≤1.575 V，3.0V≤V_{CCO}≤3.6V，3.0V≤V_{CCAUX}≤3.6V，-55℃≤T_A≤125℃	Group A Subgroups	Limits		units
				Min	Max	
Input capacitance (sample tested)	C_{in}，C_{out}	f=1.0MHz，V_{OUT}=0V	A4	—	20	pF
CLK0，CLK90，CLK190，CLK270	*CLKOUT_FREQ_1X_LF_Min*		A9, A10, A11	24	—	MHz
CLK0，CLK90，CLK190，CLK270	*CLKOUT_FREQ_1X_LF_Max*		A9, A10, A11	—	180	MHz
CLK2X，CLK2X180	*CLKOUT_FREQ_2X_LF_Min*		A9, A10, A11	48	—	MHz
CLK2X，CLK2X180	*CLKOUT_FREQ_2X_LF_Max*		A9, A10, A11	—	360	MHz
CLKDV	*CLKOUT_FREQ_DV_LF_Min*		A9, A10, A11	1.5	—	MHz
CLKDV	*CLKOUT_FREQ_DV_LF_Max*		A9, A10, A11	—	120	MHz
CLKFX，CLKFX180	*CLKOUT_FREQ_FX_LF_Min*		A9, A10, A11	24	—	MHz
CLKFX，CLKFX180	*CLKOUT_FREQ_FX_LF_Max*		A9, A10, A11	—	210	MHz
CLKIN (using DLL outputs)	*CLKIN_FREQ_DLL_LF_Min*		A9, A10, A11	24		MHz
CLKIN (using DLL outputs)	*CLKIN_FREQ_DLL_LF_Max*		A9, A10, A11		180.00	MHz
CLKIN(using CLKFX outputs)	*CLKIN_FREQ_FX_LF_Min*		A9, A10, A11	1.00		MHz

Test	Symbol	Conditions Limits $1.425V \le V_{CCINT} \le 1.575V$，$3.0V \le V_{CCO} \le 3.6V$，$3.0V \le V_{CCAUX} \le 3.6V$，$-55℃ \le T_A \le 125℃$	Group A Subgroups	Limits		units
				Min	Max	
CLKIN (using CLKFX outputs)	*CLKIN_FREQ_FX_LF_Max*		A9, A10, A11		210.00	MHz
CLKI0，CLK180	*CLKOUT_FREQ_1X_HF_Min*		A9, A10, A11	48	—	MHz
CLKI0，CLK180	*CLKOUT_FREQ_1X_HF_Max*		A9, A10, A11	—	360	MHz
CLKDV	*CLKOUT_FREQ_DV_HF_Min*		A9, A10, A11	3	—	MHz
CLKDV	*CLKOUT_FREQ_DV_HF_Max*		A9, A10, A11	—	240	MHz
CLKFX，CLKFX180	*CLKOUT_FREQ_FX_HF_Min*		A9, A10, A11	210	—	MHz
CLKFX，CLKFX180	*CLKOUT_FREQ_FX_HF_Max*		A9, A10, A11	—	270	MHz
CLKIN (using DLLoutputs)	*CLKIN_FREQ_DLL_HF_Min*		A9, A10, A11	48		MHz
CLKIN (using DLLoutputs)	*CLKIN_FREQ_DLL_HF_Max*		A9, A10, A11		360.00	MHz
CLKIN (using CLKFXoutputs)	*CLKIN_FREQ_FX_HF_Min*		A9, A10, A11	50.00		MHz
CLKIN (using CLKFXoutputs)	*CLKIN_FREQ_FX_HF_Max*		A9, A10, A11		270.00	MHz

Test	Symbol	Conditions Limits $1.425V \le V_{CCINT} \le 1.575V$，$3.0V \le V_{CCO} \le 3.6V$，$3.0V \le V_{CCAUX} \le 3.6V$，$-55℃ \le T_A \le 125℃$	Group A Subgroups	Limits		units
				Min	Max	
TMS and TDI Setup times before TCK	T_{TAPTK}		A9, A10, A11	5.5		ns
TMS and TDI Hold times after TCK	T_{TCKTAP}		A9, A10, A11	0		ns
Output delay from clock TCK to output TDO	T_{TCKTDO}		A9, A10, A11		10	ns
Maximum TCK clock frequency	F_{TCK}		A9, A10, A11		33	MHz
LVTTL Global Clock Input to Output Delay using Output Flipflop,12 mA, Fast Slew Rate,with DCM. Global Clock and OFF with DCM	$T_{ICKOFDCM}$		A9, A10, A11		2.88	ns
LVTTL Global Clock Input to Output Delay using Output Flipflop, 12 mA, Fast Slew Rate, without DLL. Global Clock and OFF without DCM	T_{ICKOF}		A9, A10, A11		6.62	ns

Test	Symbol	Conditions Limits 1.425V≤V_{CCINT}≤1.575 V，3.0V≤V_{CCO}≤3.6V，3.0V≤V_{CCAUX}≤3.6V，-55℃≤T_A≤125℃	Group A Subgroups	Limits		units
				Min	Max	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. No Delay Global Clock and IFF with DCM	T_{PSDCM}/ T_{PHDCM}		A9, A10, A11		1.96/ -0.76	ns
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. Full Delay Global Clock and IFF without DCM	T_{PSFD}/ T_{PHFD}		A9, A10, A11		2.21/ 0.0	ns

Appendix II Application Notes

- Master CCLK Frequency

In Master Serial configuration mode, the CCLK frequency driven by BQR2V3000 is correlated to the OSCFSEL-Specified Master CCLK Frequencies set by the ISE design suit. The actual Master CCLK Frequency is much smaller than the setting value. Because of the structures of the internal oscillators，master CCLK frequency is accurate to ±45%. If the configuration time matters for designer, the master CCLK Frequency deviation should be considered.

- CS_B&RDWR_B

Even the configuration mode is not SelectMAP, Chip Select (CS_B) signal, and a Write signal (RDWR_B) should be kept in a stable state. The logic level changing in those two pins may cause a failure during configuration.

- Develop tools

Xilinx ISE10.1 and synthesis tool XST are recommended. Third-party synthesis tools may compress the utility of logic resources, according to XST report the actual resources usage could exceed 100%, which should be avoided.

- PROM program

XCF series、 XC18 series and XQR17 series PROMs are supported. In-System Programmable PROMs such as XCF series and XC18 series can be programmed individually, or two or more can be chained together and programmed in-system via the standard 4-pin JTAG protocol. When programming, JTAG signals are vulnerable, a PCB design should consider the JTAG signal integrity. If the programming process is failed, please check the JTAG connections and make sure the cable and connections are not disturbed by any other signals.

Appendix III BitGen and PROMGen Switches and Options

Using BitGen

BitGen produces a bitstream for device configuration. After the design has been completely routed, it is necessary to configure the device so that it can execute the desired function. The bitstream necessary to configure the device is generated with BitGen. BitGen takes a fully routed NCD (Circuit Description) file as its input and produces a configuration bitstream—a binary file with a .bit extension. The BIT file contains all of the configuration information from the NCD file defining the internal logic and interconnections of the FPGA, plus device-specific information from other files associated with the target device. The binary data in the BIT file can then be downloaded into the FPGA memory cells, or it can be used to create a PROM file (see Figure III-1).

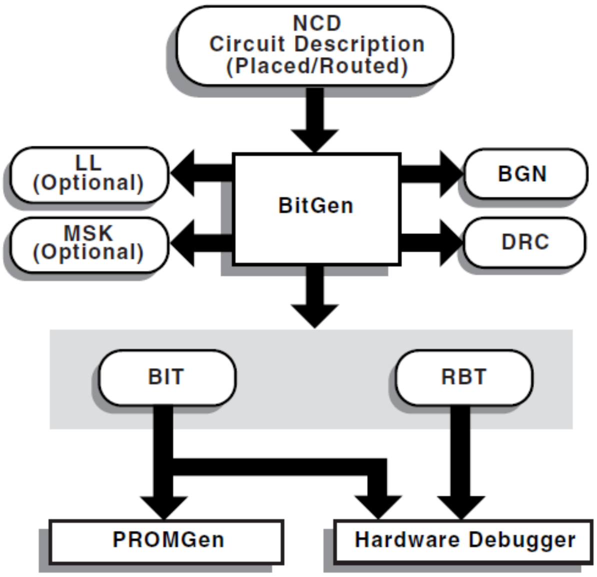


Figure III-1 BitGen

BitGen Syntax

The following syntax creates a bitstream from your NCD file.

bitgen [*options*] *infile*[**.ncd**] [*outfile*] [*pcf_file*]

options is one or more of the options listed in the "BitGen Options". *Infile* is the name of the NCD design for which you want to create the bitstream. You can specify only one design file, and it must be the first file specified on the command line. You do not have to use an extension. If you do not, **.ncd** is assumed. If you do use an extension, it must be **.ncd**. *Outfile* is the name of the output file. If you do not specify an output file name, BitGen creates one in the same directory as the input file. If you specify -l on the command line, the extension is .ll (see -l command line option). If you specify -m (see -m command line option), the extension is .msk. If you specify -b, the extension is .rbt. Otherwise the extension is .bit. If you do not specify an extension, BitGen appends one according to the aforementioned rules. If you do include an extension, it must also conform to the rules. *Pcf_file* is the name of a physical constraints (PCF) file. BitGen uses this file to determine which nets in the design are critical for tiedown. BitGen automatically reads the .pcf file by default. If the physical constraints file is the second file specified on the command line, it must have a .pcf extension. If it is the third file specified, the extension is optional; .pcf is assumed. If a .pcf file name is specified, it must exist, otherwise the input design name with a .pcf extension is read if that file exists. A report file containing all BitGen's output is automatically created under the same directory as the output file. The report file has the same root name as the output file with a .bgn extension.

BitGen Files

This section describes input files that BitGen requires and output files that BitGen generates.

Input Files

Input to BitGen consists of the following files.

• NCD file—a physical description of the design mapped, placed and routed in the target device. The NCD file must be fully routed.

• PCF—an optional user-modifiable ASCII Physical Constraints File. If you specify a PCF file on the BitGen command line, BitGen uses this file to determine which nets in the design are critical for tiedown (not used for Virtex families).

Output Files

Output from BitGen consists of the following files.

• BIT file—a binary file with a .bit extension. The BIT file contains all of the configuration information from the NCD file defining the internal logic and interconnections of the FPGA, plus device-specific information from other files associated with the target device. The binary data in the BIT file can then be downloaded into the FPGA memory cells, or it can be used to create a PROM file.

• RBT file—an optional "rawbits" file with an .rbt extension. The rawbits file is

ASCII ones and zeros representing the data in the bitstream file. If you enter a -b option on the BitGen command line, an RBT file is produced in addition to the binary BIT file.

• LL file—an optional ASCII logic allocation file with a .ll extension. The logic allocation file indicates the bitstream position of latches, flip-flops, and IOB inputs and outputs.A .ll file is produced if you enter a -l option on the BitGen command line.

• MSK file—an optional mask file with an .msk extension. This file is used to compare relevant bit locations for executing a readback of configuration data contained in an operating FPGA. A MSK file is produced if you enter a -m option on the BitGen command line.

• BGN file—a report file containing information about the BitGen run.

• DRC file—a Design Rule Check (DRC) file for the design. A DRC runs and the DRC file is produced unless you enter a -d option on the BitGen command line.

BitGen Options

Following is a description of command line options and how they affect BitGen behavior.

-b (Create Rawbits File)

Create a “rawbits” (*file_name*.rbt) file. The rawbits file consists of ASCII ones and zeros representing the data in the bitstream file. If you are using a microprocessor to configure a single FPGA, you can include the rawbits file in the source code as a text file to represent the configuration data. The sequence of characters in the rawbits file is the same as the sequence of bits written into the FPGA.

-d (Do Not Run DRC)

Do not run DRC (Design Rule Check). Without the -d option, BitGen runs a DRC and saves the DRC results in two output files: the BitGen report file (*file_name*.bgn) and the DRC file (*file_name*.drc). If you enter the -d option, no DRC information appears in the report file and no DRC file is produced. Running DRC before a bitstream is produced detects any errors that could cause the FPGA to malfunction. If DRC does not detect any errors, BitGen produces a bitstream file (unless you use the -j option).

-f (Execute Commands File)

-f command_file

The -f option executes the command line arguments in the specified
command_file.

-g (Set Configuration)

-g option:setting

The -g option specifies the startup timing and other bitstream options for FPGAs.The settings for the -g option depend on the design's architecture. These options have the following syntax:

Binary

Creates a binary file with programming data only. Use this option to extract and view programming data. Any changes to the header will not affect the extraction process.

Settings: No, Yes

Default: No

Cclk Pin

Adds an internal pull-up to the Cclk pin. The Pullnone setting disables the pullup.

Settings: Pullnone, Pullup

Default: Pullup

Compress

This option uses the multiple frame write feature in the bitstream to reduce the size of the bitstream, not just the .bit file. Using the Compress option does not guarantee that the size of the bitstream will shrink.

Config Rate

An internal oscillator to generate the configuration clock, CCLK, when configuring in a master mode. Use the configuration rate option to select the rate for this clock.

Settings: 4, 5, 7, 8, 9, 10, 13, 15, 20, 26, 30, 34, 41, 45, 51, 55, 60

Default: 4

DCM Shutdown

When DCM Shutdown is enabled, the DCM (Digital Clock Manager) resets if the SHUTDOWN and AGHIGH commands are loaded into the configuration logic.

Settings: Disable, Enable

Default: Disable

Debug Bitstream

If the device does not configure correctly, you can debug the bitstream using the Debug Bitstream option. A debug bitstream is significantly larger than a standard bitstream. The values allowed for the Debug Bitstream option are No and Yes.

Note: You should use this option only if your device is configured to use slave or master serial mode.

Values: No, Yes

In addition to a standard bitstream, a debug bitstream offers the following features:

• Writes 32 0s to the LOUT register after the synchronization word

• Loads each frame individually

• Performs a cyclical redundancy check (CRC) after each frame

• Writes the frame address to the LOUT register after each frame

Disable Bandgap

Disables bandgap generator for DCMs to save power.

Settings: No, Yes

Default: No

DONE_cycle

Selects the Startup phase that activates the FPGA Done signal. Done is delayed when DonePipe=Yes.

Settings: 1, 2, 3, 4, 5, 6

Default: 4

Done Pin

Adds an internal pull-up to the DONE Pin pin. The Pullnone setting disables the pullup. Use this option only if you are planning to connect an external pull-up resistor to this pin. The internal pull-up resistor is automatically connected if you do not use this option.

Settings: Pullup, Pullnone

Default: Pullup

Done Pipe

This option is intended for use with FPGAs being set up in a high-speed daisy chain configuration. When set to Yes, the FPGA waits on the CFG_DONE (DONE) pin to go High and then waits for the first clock edge before moving to the Done state.

Settings: No, Yes

Default: No

Drive Done

This option actively drives the DONE Pin high as opposed to using a pullup.

Settings: No, Yes

Default: No

Encrypt

Encrypts the bitstream.

Settings: No, Yes

Default: No

GTS_cycle

Selects the Startup phase that releases the internal 3-state control to the I/O buffers. The Done setting releases GTS when the DoneIn signal is High. DoneIn is either the value of the Done pin or a delayed version if DonePipe=Yes

Settings: Done, 1, 2, 3, 4, 5, 6, Keep

Default: 5

GWE_cycle

Selects the Startup phase that asserts the internal write enable to flip-flops, LUT RAMs, and shift registers. It also enables the BRAMs. Before the Startup phase both BRAM writing and reading are disabled.The Done setting asserts GWE when the DoneIn signal is High. DoneIn is either the value of the Done pin or a delayed version if DonePipe=Yes. The Keep setting is used to keep the current value of the GWE signal

Settings: Done, 1, 2, 3, 4, 5, 6, Keep

Default: 6

Key0, Key1, Key2, Key3, Key4, Key5

Sets Key*x* for bitstream encryption. The Pick option causes BitGen to select a random number for the value.

Settings: Pick, <*hex_string*>

Default: Pick

Key File

Specifies the name of the input encryption file.

Settings: <*string*>

Keyseq0, Keyseq1, Keyseq2, Keyseq3, Keyseq4, Keyseq5

Sets the key sequence for key*x*. The settings are equal to the following:

• S = single

• F = first

• M = middle

• L = last

Settings: S, F, M, L

Default: S

LCK_cycle

Selects the Startup phase to wait until DLLs/DCMs lock. If NoWait is selected, the Startup sequence does not wait for DLLs/DCMs.

Settings: 0, 1, 2, 3, 4, 5, 6, NoWait

Default: NoWait

M0 Pin

The M0 pin is used to determine the configuration mode. Adds an internal pull-up, pulldown or neither to the M0 pin. The following settings are available. The default is PullUp. Select Pullnone to disable both the pull-up resistor and pull-down resistor on the M0 pin.

Settings: Pullup, Pulldown, Pullnone

Default: Pullup

M1 Pin

The M1 pin is used to determine the configuration mode. Adds an internal pull-up, pulldown or neither to the M1 pin. The following settings are available. The default is PullUp. Select Pullnone to disable both the pull-up resistor and pull-down resistor on the M1 pin.

Settings: Pullup, Pulldown, Pullnone

Default: Pullup

M2 Pin

The M2 pin is used to determine the configuration mode. Adds an internal pull-up, pulldown or neither to the M2 pin. The default is PullUp. Select Pullnone to disable both the pull-up resistor and pull-down resistor on the M2 pin.

Settings: Pullup, Pulldown, Pullnone

Default: Pullup

Match_cycle

Specifies a stall in this Startup cycle until DCI (Digitally Controlled Impedance) match signals are asserted.

Settings: NoWait, 0, 1, 2, 3, 4, 5, 6

Default: NoWait

Persist

This option is needed for Readback and Partial Reconfiguration using the SelectMAP configuration pins. If Persist is set to Yes, the pins used for SelectMAP mode are prohibited for use as user IO. Refer to the data sheet for a description of SelectMAP mode and the associated pins.

Settings: No, Yes

Default: No

ProgPin

Adds an internal pull-up to the ProgPin pin. The Pullnone setting disables the pull-up. The pull-up affects the pin after configuration.

Settings: Pullup, Pullnone

Default: Pullnone

ReadBack

This option allows you to perform Readback by the creating the necessary bitstream. When specifying the -g Readback option, the .rba, .rbb, .rbd, and .msd file are created.

Security

Selecting Level1 disables Readback. Selecting Level2 disables Readback and Partial Reconfiguration.

Settings: None, Level1, Level2

Default: None

StartCBC

Sets the starting CBC (Cipher Block Chaining) value. The pick option causes BitGen to select a random number for the value.

Settings: Pick, <*hex_string*>

Default: Pick

StartKey

Sets the starting key number.

Settings: 0, 3

Default: 0

StartupClk

The startup sequence following the configuration of a device can be synchronized to either Cclk, a User Clock, or the JTAG Clock. The default is Cclk.

Cclk

Enter Cclk to synchronize to an internal clock provided in the FPGA device.

JTAG Clock

Enter JtagClk to synchronize to the clock provided by JTAG. This clock sequences the TAP controller which provides the control logic for JTAG.

UserClk

Enter UserClk to synchronize to a user-defined signal connected to the CLK pin of the STARTUP symbol.

Settings: Cclk (pin—see Note), UserClk (user-supplied), JtagCLK

Default: Cclk

NOTE: In modes where Cclk is an output, the pin is driven by an internal oscillator.

Tck Pin

Adds a pull-up, a pull-down or neither to the TCK pin, the JTAG test clock. Selecting one setting enables it and disables the others. The Pullnone setting indicates there is no connection to either the pull-up or the pull-down.

Settings: Pullup, Pulldown, Pullnone

Default: Pullup

Tdi Pin

Adds a pull-up, a pull-down, or neither to the TDI pin, the serial data input to all JTAG instructions and JTAG registers. Selecting one setting enables it and disables the others. The Pullnone setting indicates there is no connection to either the pull-up or the pulldown.

Settings: Pullup, Pulldown, Pullnone

Default: Pullup

Tdo Pin

Adds a pull-up, a pull-down, or neither to the TdoPin pin, the serial data output for all JTAG instruction and data registers. Selecting one setting enables it and disables the others. The Pullnone setting indicates there is no connection to either the pull-up or the pulldown.

Settings: Pullup, Pulldown, Pullnone

Default: Pullup

Tms Pin

This option selects an internal pullup or pulldown on the TMS (JTAG Mode Select) pin.

Settings: Pullnone, Pullup, Pulldown

Default: Pullup

Unused Pin

Adds a pull-up, a pull-down, or neither to the Unused Pin, the serial data output for all JTAG instruction and data registers. Selecting one setting enables it and disables the others.The Pullnone setting indicates there is no connection to either the pull-up or the pulldown.The following settings are available. The default is PullDown.

Settings: Pullup, Pulldown, Pullnone

Default: Pulldown

User ID

You can enter up to an 8-digit hexadecimal code in the User ID register. You can use the register to identify implementation revisions.

-h or -help (Command Usage)

-h architecture

Displays a usage message for BitGen. The usage message displays all available options for BitGen operating on the specified *architecture*.

-j (No BIT File)

Do not create a bitstream file (.bit file). This option is generally used when you want to generate a report without producing a bitstream. For example, if you wanted to run DRC without producing a bitstream file, you would use the -j option.

Note: The .msk or .rbt files might still be created.

-l (Create a Logic Allocation File)

This option creates an ASCII logic allocation file (*design*.**ll**) for the selected design. The logic allocation file indicates the bitstream position of latches, flip-flops, and IOB inputs and outputs. In some applications, you may want to observe the contents of the FPGA internal registers at different times. The file created by the -l option helps you identify which bits in the current bitstream represent outputs of flip-flops and latches. Bits are referenced by frame and bit number within the frame. The Hardware Debugger uses the **design.ll** file to locate signal values inside a readback bitstream.

-m (Generate a Mask File)

Creates a mask file. This file is used to compare relevant bit locations for executing a readback of configuration data contained in an operating FPGA.

-w (Overwrite Existing Output File)

Enables you to overwrite an existing BIT, LL, MSK, or RBT output file.

Using PROMGen

PROMGen formats a BitGen-generated configuration bitstream (BIT) file into a PROM format file (Figure III-2).

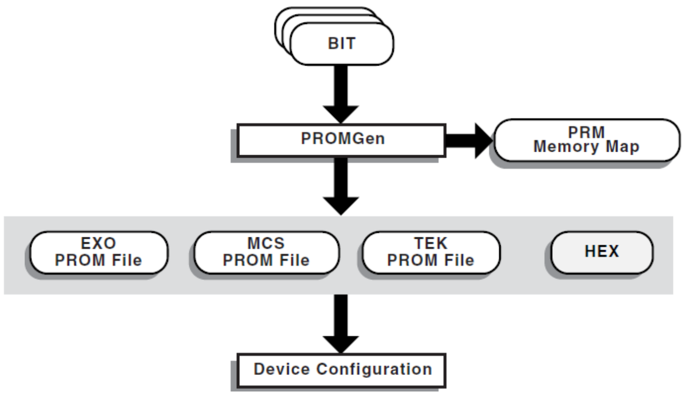


Figure III-2 PROMGen

The PROM file contains configuration data for the FPGA device. PROMGen converts a BIT file into one of three PROM formats: MCS-86 (Intel), EXORMAX (Motorola), or TEKHEX (Tektronix). It can also generate a Hex file format. You can also use PROMGen to concatenate bitstream files to daisy-chain FPGAs.

Note: If the destination PROM is one of the Xilinx Serial PROMs, you are using a Xilinx PROM Programmer, and the FPGAs are not being daisy-chained, it is not necessary to make a PROM file.

PROMGen Syntax

Use the following syntax to start PROMGen from the operating system prompt:

promgen [*options*]

Options can be any number of the options listed in "PROMGen Options".

Separate multiple options with spaces.

PROMGen Files

This section describes the PROMGen input and output files.

Input Files

The input to PROMGEN consists of BIT files— one or more bitstream files. BIT files contain configuration data for an FPGA design.

Output Files

Output from PROMGEN consists of the following files.

• PROM files—The file or files containing the PROM configuration information. Depending on the PROM file format used by the PROM programmer, you can output a TEK, MCS, or EXO file. If you are using a microprocessor to configure your devices, you can output a HEX file, containing a hexadecimal representation of the bitstream.

• PRM file—The PRM file is a PROM image file. It contains a memory map of the output PROM file. The file has a **.prm** extension.

Bit Swapping in PROM Files

PROMGen produces a PROM file in which the bits within a byte are swapped compared to the bits in the input BIT file. Bit swapping (also called "bit mirroring") reverses the bits within each byte, as shown in Figure III-3.

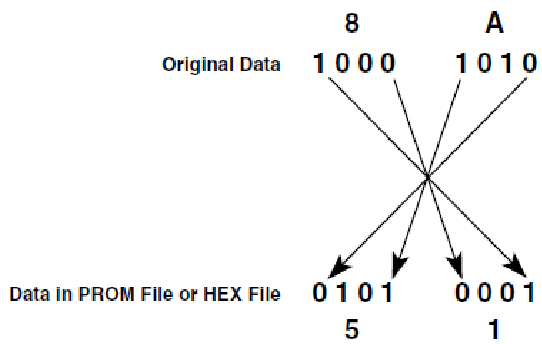


Figure III-3 Bit Swapping

In a bitstream contained in a BIT file, the Least Significant Bit (LSB) is always on the left side of a byte. But when a PROM programmer or a microprocessor reads a data byte, it identifies the LSB on the right side of the byte. In order for the PROM programmer or microprocessor to read the bitstream correctly, the bits in each byte must first be swapped so they are read in the correct order In this release of the Xilinx Development System, the bits are swapped for all of the PROM formats: MCS, EXO, and TEK. For a HEX file output, bit swapping is on by default, but it can be turned off by entering a -b PROMGen option that is available only for HEX file format.

PROMGen Options

This section describes the options that are available for the PROMGen command.

-b (Disable Bit Swapping—HEX Format Only)

This option only applies if the -p option specifies a HEX file for the output of PROMGen. By default (no -b option), bits in the HEX file are swapped compared to bits in the input BIT files. If you enter a -b option, the bits are not swapped. Bit swapping is described in "Bit Swapping in PROM Files".

-c (Checksum)

promgen -c

The -c option generates a checksum value appearing in the .prm file. This value should match the checksum in the prom programmer. Use this option to verify that correct data was programmed into the prom.

-d (Load Downward)

promgen -d *hexaddress0 filename filename...*

This option loads one or more BIT files from the starting address in a downward direction. Specifying several files after this option causes the files to be concatenated in a daisy chain. You can specify multiple -d options to load files at different addresses. You must specify this option immediately before the input bitstream file. The multiple file syntax is as follows:

promgen -d *hexaddress0 filename filename...*

The multiple **-d** options syntax is as follows:

promgen -d *hexaddress1 filename* **-d** *hexaddress2 filename...*

-f (Execute Commands File)

-f *command_file*

The -f option executes the command line arguments in the specified *command_file*.

-help (Command Help)

This option displays help that describes the PROMGen options.

-n (Add BIT FIles)

-n *file1*[**.bit**] *file2*[**.bit**]...

This option loads one or more BIT files up or down from the next available address following the previous load. The first -n option *must* follow a -u or -d option because –n does not establish a direction. Files specified with this option are not daisy-chained to previous files. Files are loaded in the direction established by the nearest prior -u, -d, or –n option. The following syntax shows how to specify multiple files. When you specify multiple files, PROMGen daisy-chains the files.

promgen -d *hexaddress file0* **-n** *file1 file2...*

The following syntax when using multiple -n options prevents the files from being daisychained:

promgen -d *hexaddress file0* **-n** *file1* **-n** *file2...*

-o (Output File Name)

-o *file1*[.*ext*] *file2*[.*ext*]...

This option specifies the output file name of a PROM if it is different from the default. If you do not specify an output file name, the PROM file has the same name as the first BIT file loaded. *ext* is the extension for the applicable PROM format. Multiple file names may be specified to split the information into multiple files. If only one name is supplied for split PROM files (by you or by default), the output PROM files are named *file_#*.ext, where *file* is the base name, # is 0, 1, etc., and *ext* is the extension for the applicable PROM format.

promgen -d *hexaddress file0* **-o** *filename*

-p (PROM Format)

-p {**mcs** | **exo** | **tek** | hex}

This option sets the PROM format to one of the following: MCS (Intel MCS86), EXO (Motorola EXORMAX), TEK (Tektronix TEKHEX). The option may also produce a HEX file, which is a hexadecimal representation of the configuration bitstream used for microprocessor downloads. If specified, the -p option must precede any -u, -d, or –n options. The default format is MCS.

-r (Load PROM File)

-r *promfile*

This option reads an existing PROM file as input instead of a BIT file. All of the PROMGen output options may be used, so the -r option can be used for splitting an existing PROM file into multiple PROM files or for converting an existing PROM file to another format.

-s (PROM Size)

-s *promsize1 promsize2...*

This option sets the PROM size in kilobytes. The PROM size must be a power of 2. The default value is 64 kilobytes. The -s option must precede any -u, -d, or -n options. Multiple *promsize* entries for the -s option indicates the PROM will be split into multiple PROM files.

Note: PROMGen PROM sizes are specified in bytes. The Programmable Logic Data Book specifies PROM sizes in bits for Xilinx serial PROMs (see -x option).

-u (Load Upward)

-u *hexaddress0 filename1 filename2...*

This option loads one or more BIT files from the starting address in an upward direction. When you specify several files after this option, PROMGen concatenates the files in a daisy chain. You can load files at different addresses by specifying multiple -u options. This option must be specified immediately before the input bitstream file.

-x (Specify Xilinx PROM)

-x xilinx*_prom1* xilinx*_prom2...*

The -x option specifies one or more Xilinx serial PROMs for which the PROM files are targeted. Use this option instead of the -s option if you know the Xilinx PROMs to use. Multiple xilinx*_prom* entries for the -x option indicates the PROM will be split into multiple PROM files.

Examples

To load the file test.bit up from address 0x0000 in MCS format, enter the following information at the command line.

promgen -u 0 test

To daisy-chain the files test1.bit and test2.bit up from address 0x0000 and the files test3.bit and test4.bit from address 0x4000 while using a 32K PROM and the Motorola EXORmax format, enter the following information at the command line.

promgen -s 32 -p exo -u 00 test1 test2 -u 4000 test3 test4

To load the file test.bit into the PROM programmer in a downward direction starting at address 0x400, using a Xilinx XC1718D PROM, enter the following information at the command line.

promgen -x xc1718d -d 0x400 test

To specify a PROM file name that is different from the default file name enter the following information at the command line.

promgen *options filename* **-o** *newfilename*

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