Ver 1.1

Radiation-Hardened FPGA

Datasheet

Part Number：BQVR300RH

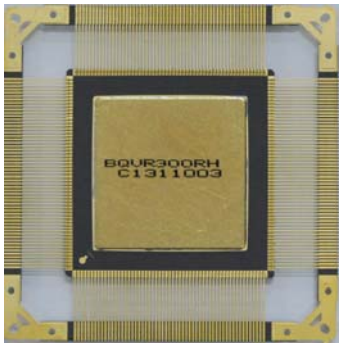
中国航天 北京微电子技术研究所
Beijing Microelectronics Technology Institute

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2017.2		Initial release.	
1.1	2018.3		Update format	

TABLE OF CONTENTS

1. Features



- ●0.25 μm 5-layer epitaxial process
- ●GJB597A-1996 CLASS B \ CAST C
- ●Radiation hardened FPGAs for space and satellite Applications
- ●Guaranteed over the full military temperature range(–55 ℃to +125℃)
- ●Fast, high-density Field-Programmable Gate Arrays
  - -Densities of 322,970 system gates
  - -System performance up to 200 MHz
  - -66-MHz PCI Compliant
  - -Hot-swappable for Compact PCI
- ●Multi-standard SelectIO™ interfaces
  - -16 high-performance interface standards
  - -Connects directly to ZBTRAM devices
- ●Built-in clock-management circuitry
  - -Four dedicated delay-locked loops (DLLs) for advanced clock control
  - -Four primary low-skew global clock distribution nets, plus 24 secondary local clock nets
- ●Hierarchical memory system
  - -LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - -Configurable synchronous dual-ported 4k-bit RAMs
  - -Fast interfaces to external high-performance RAMs
- ●Flexible architecture that balances speed and density
  - -Dedicated carry logic for high-speed arithmetic
  - -Cascade chain for wide-input functions
  - -Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - -Internal 3-state bussing
  - -IEEE 1149.1 boundary-scan logic
  - -Die-temperature sensor diode
- ●Supported by Xilinx develop tools
  - -Complete support for ISE10.1
  - - Complete support for PC with Windows XP system
- ●SRAM-based in-system configuration
  - -Unlimited re-programmability
  - -Four programming modes
- ●Guaranteed total ionizing dose to 100K Rad(Si)
- ●SEL immune to LET ＞75 MeV·cm^2/mg
- ●SEU threshold value is 15 MeV·cm^2/mg (10% saturation cross section)

2. General Description

The BQVR300RH delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.25um CMOS process. These advances make BQVR300RH powerful and flexible alternatives to mask-programmed gate arrays. The BQVR300RH comprises sorts of resources shown in Table1.

Building on experience gained from previous generations of FPGA, the BQVR300RH represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the BQVR300RH a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

The anti-radiation capacity of BQVR300RH is as follows:

- Total Ionizing Dose: no less than 1.0×10^5 rad(Si)[1]
- LET of Single Event Latch-up: no less than 75 MeV·cm^2/mg
- LET of Single Event Latch-up: no less than 15 MeV·cm^2/mg（10% saturation cross section）

If a user first start BQVR300RH, some important information should be noticed, see in appendix II.

Table 1: BQVR300RH Field-Programmable Gate Array resources

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	Block RAM Bits	Maximum SelectRAM+™ Bits
BQVR300RH	322,970	32x48	6,912	162	65,536	98,304

Note：

1，As device characteristics are changed during Total Ionizing Dose test, the device may fail the power-on. The devices should only power on for just one time during the radiation experiment and be kept in a state of none configuration. After 1.0×10^5 rad(si) radiation the devices should be directly put under the temperature of 100 centigrade for 168 hours and then the function of the device can be tested.

3. BQVR300RH Architecture

BQVR300RH feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the BQVR300RH to accommodate even the largest and most complex designs.

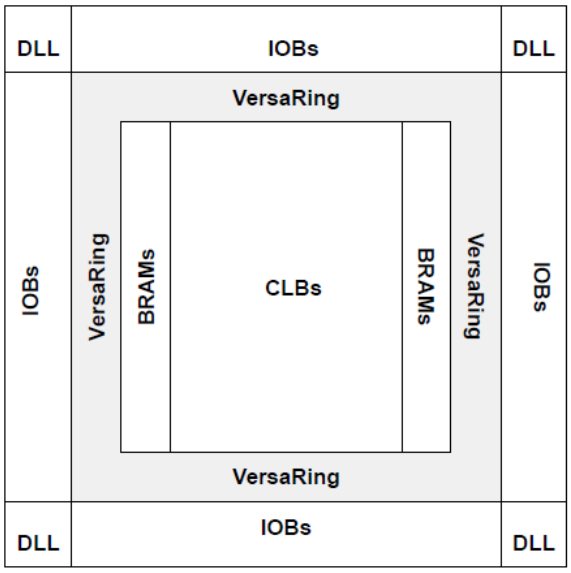


Figure 1: Virtex Architecture Overview

The BQVR300RH user-programmable gate array, shown in Figure 1, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks(IOBs).

• CLBs provide the functional elements for constructing logic

• IOBs provide the interface between the package pins and the CLBs

CLBs interconnect through a general routing matrix (GRM).The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock that also provides local routing resources to connect the CLB to the GRM. The VersaRing I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking. The BQVR300RH architecture also includes the following circuits that connect to the GRM.

• Dedicated block memories of 4096 bits each

• Clock DLLs for clock-distribution delay compensation and clock domain

control

• 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

3.1Input/Output Block

The BQVR300RH IOB, Figure 2, that support a wide variety of I/O signalling standards, see Table 2.The three IOB storage elements function either as edge-triggered D-type flip-flops or as level sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop. In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

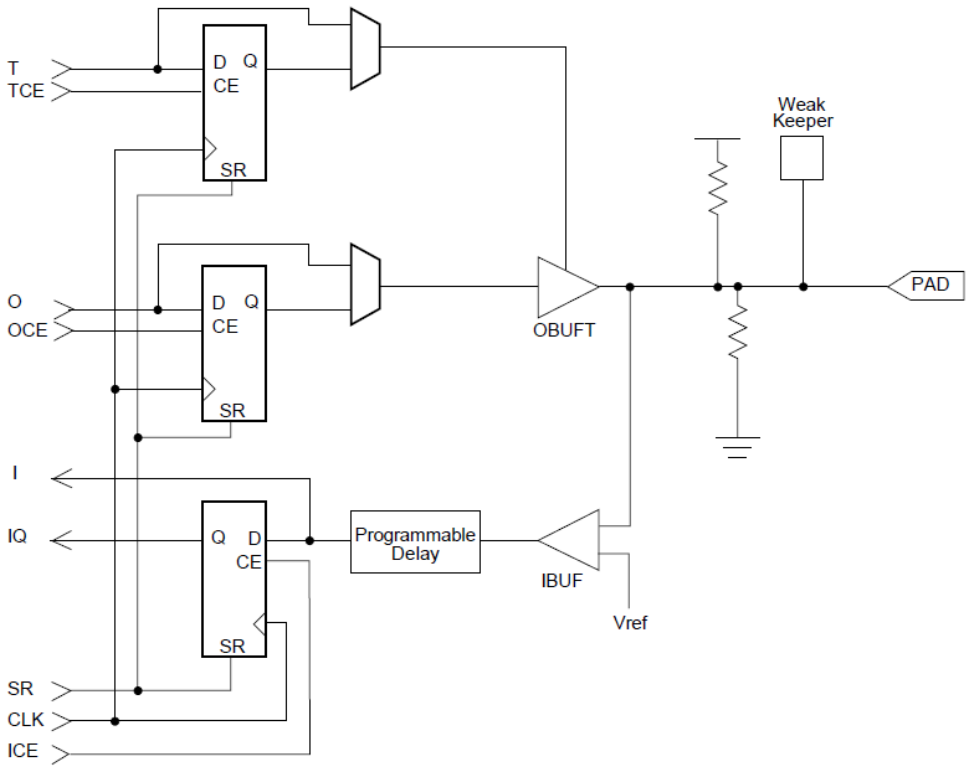


Figure 2: Input/Output Block (IOB)

The output buffer and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Two forms of over-voltage protection are provided, one that permits 5 V compliance, and one that does not. For 5 V compliance, a Zener-like structure connected to ground turns on when the output rises to approximately 6.5 V. When PCI 3.3 V compliance is required, a conventional clamp diode is connected to the output supply voltage, VCCO. Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each pad. Prior to configuration, all pins not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs can optionally be pulled up. The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration. All BQVR300RH IOBs support IEEE 1149.1-compatible boundary scan testing.

Table 2: Supported Select I/O Standards

I/O Standard	**Input Reference Voltage (VREF)**	**Output Source Voltage (VCCO)**	**Board Termination Voltage (VTT)**	**5V Tolerant**
LVTTL 2 – 24 mA	N/A	3.3	N/A	Yes
LVCMOS2	N/A	2.5	N/A	Yes
PCI, 5 V	N/A	3.3	N/A	Yes
PCI, 3.3 V	N/A	3.3	N/A	No
GTL	0.8	N/A	1.2	No
GTL+	1.0	N/A	1.5	No
HSTL Class I	0.75	1.5	0.75	No
HSTL Class III	0.9	1.5	1.5	No
HSTL Class IV	0.9	1.5	1.5	No
SSTL3 Class I &II	1.5	3.3	1.5	No
SSTL2 Class I & II	1.25	2.5	1.25	No
CTT	1.5	3.3	1.5	No

AGP	1.32	3.3	N/A	No

Input Path

A buffer In the BQVR300RH IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, VREF. The need to supply VREF imposes constraints on which standards can used in close proximity to each other. See I/O Banking, page 6. There are optional pull-up and pull-down resistors at each input for use after configuration. Their value is in the range 20 kΩ – 70 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied VCCO voltage. The need to supply VCCO imposes constraints on which standards can be used in close proximity to each other. See I/O Banking, page 6.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate VREF voltage must be provided if the signalling standard

requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require VCCO and/or VREF voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

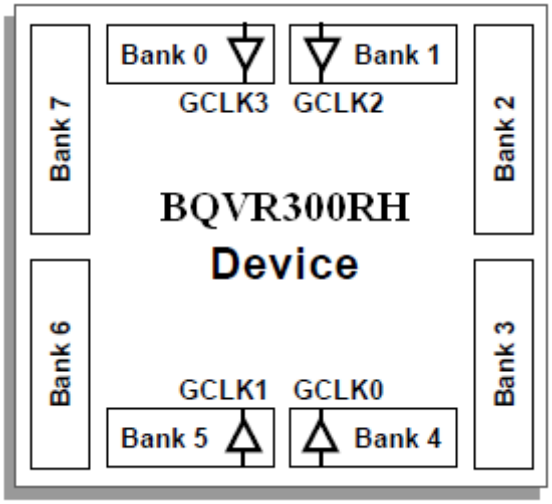


Figure 3: BQVR300RH I/O Banks

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple VCCO pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

Within a bank, output standards can be mixed only if they use the same VCCO. Compatible standards are shown in Table 3. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on VCCO.

Table 3: Compatible Output Standards

VCCO	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, VREF. In this case, certain user-I/O pins are automatically configured as inputs for the VREF voltage. Approximately one in six of the I/O pins in the bank assume this role.

The VREF pins within a bank are interconnected internally and consequently only one VREF voltage can be used within each bank. All VREF pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require VREF can be mixed with those that do not. However, only one VREF voltage can be used within a bank. Input buffers that use VREF are not 5 V tolerant. LVTTL, LVCMOS2, and PCI 33 MHz 5 V, are 5 V tolerant.

The VCCO and VREF pins for each bank appear in the device Pinout tables.

Within a given package, the number of VREF and VCCO pins can vary depending on the size of device. In larger devices, more I/O pins convert to VREF pins. Since these are always a superset of the VREF pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the VREF pins for the largest device anticipated must be connected to the VREF voltage, and not used for I/O.

In BQVR300RH, all VCCO pins are bonded together internally, and consequently the same VCCO voltage must be connected to all of them, the VREF pins remain internally connected as eight banks, and can be used as described previously.

3.2Configurable Logic Block

The basic building block of the BQVR300RH CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each CLB contains four LCs, organized in two similar slices, as shown in Figure 4.

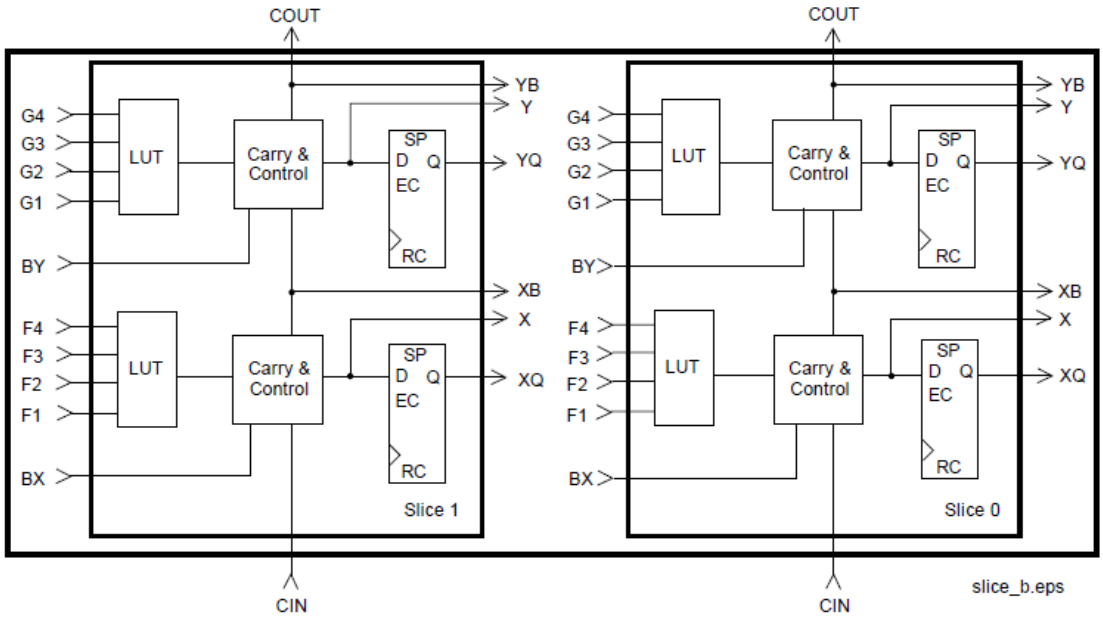


Figure 4: 2-Slice CLB

Figure 5 shows a more detailed view of a single slice. In addition to the four basic LCs, the CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

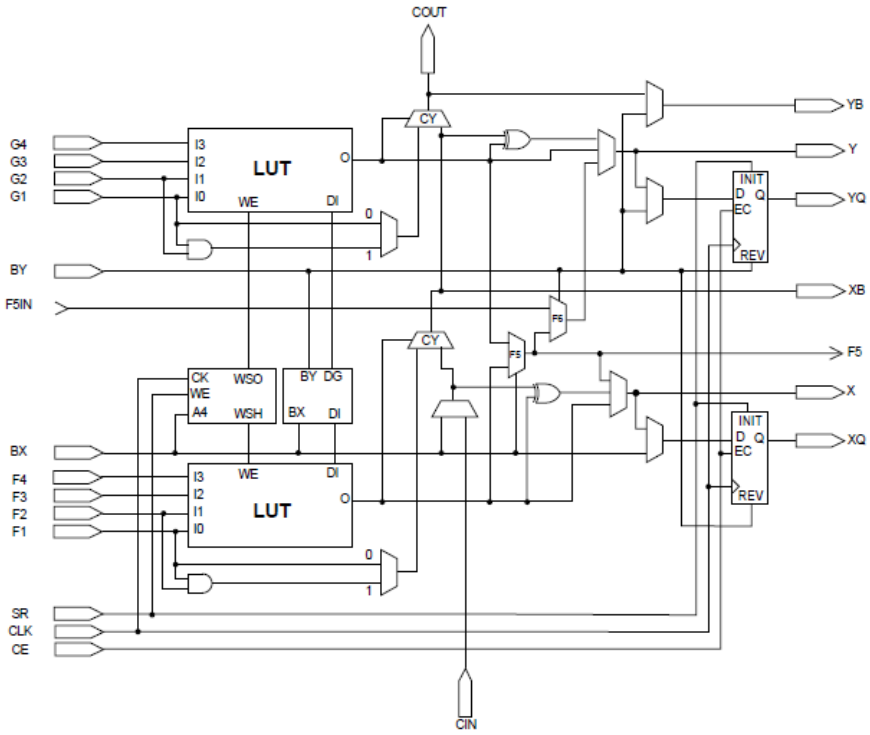


Figure 5: Detailed View of Slice

Look-Up Tables

BQVR300RH function generators are implemented as 4-input look-up tables

(LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16x1-bit dual-port synchronous RAM.

The BQVR300RH LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

The storage elements in the slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals can be configured to operate asynchronously. All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs. Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The BQVR300RH CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the

efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See Dedicated Routing, page 11.

Each BUFT has an independent 3-state control pin and an independent input pin.

3.3Block SelectRAM

BQVR300RH FPGAs incorporate several large Block SelectRAM memories. These complement the distributed LUT SelectRAMs that provide shallow RAM structures implemented in CLBs.

Block SelectRAM memory blocks are organized in columns. BQVR300RH contains two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a device contains 16 memory blocks.

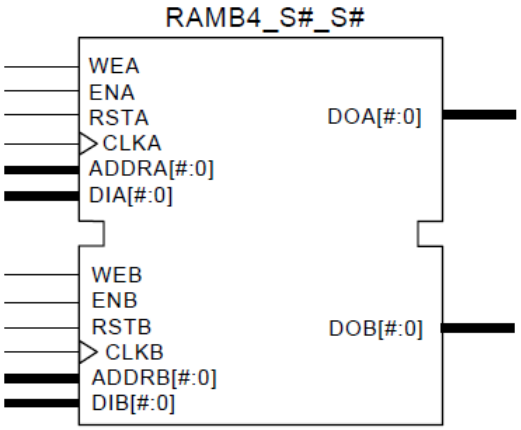


Figure 6: Dual-Port Block SelectRAM

Each Block SelectRAM cell, as illustrated in Figure 6, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 4: Block SelectRAM Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus

1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Table 4 shows the depth and width aspect ratios for the Block SelectRAM. The Block SelectRAM also includes dedicated routing to provide an efficient interface with both CLBs and other Block SelectRAMs.

3.4Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the BQVR300RH routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Local Routing

The VersaBlock provides local routing resources, as shown in Figure 7, providing the following three types of connections.

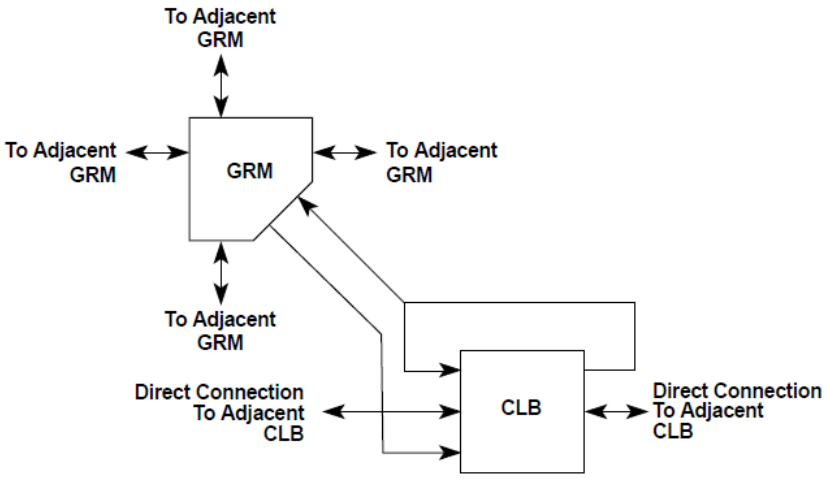


Figure 7: Local Routing

• Interconnections among the LUTs, flip-flops, and GRM

• Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay

• Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

General Purpose Routing

Most BQVR300RH signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy.

The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns CLBs. The general-purpose routing resources are listed below.

• Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.

• 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.

• 72 buffered Hex lines route GRM signals to another GRMs six-blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines can be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are uni-directional.

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. BQVR300RH devices include two tiers of global routing resources referred to as primary global and secondary local clock routing resources.

• The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets can only be driven by global buffers. There are four global buffers, one for each global net.

• 12 Longlines are buffered, bidirectional wires that distribute signals across the

device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

BQVR300RH devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the BQVR300RH architecture, dedicated routing resources are provided for two classes of signal.

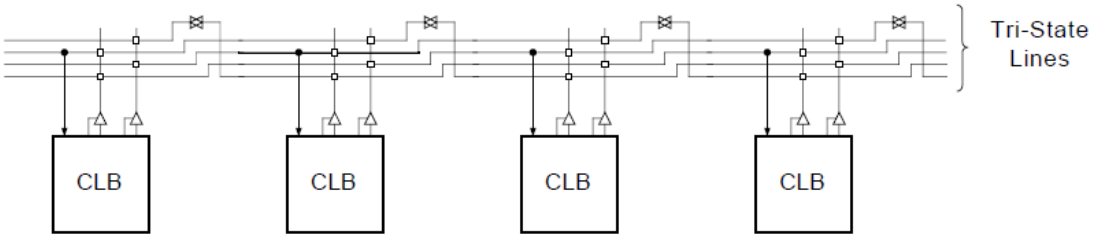


Figure 8: BUFT Connections to Dedicated Horizontal Bus Lines

• Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 8.

• Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

• The secondary local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

Clock Distribution

BQVR300RH provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 9.

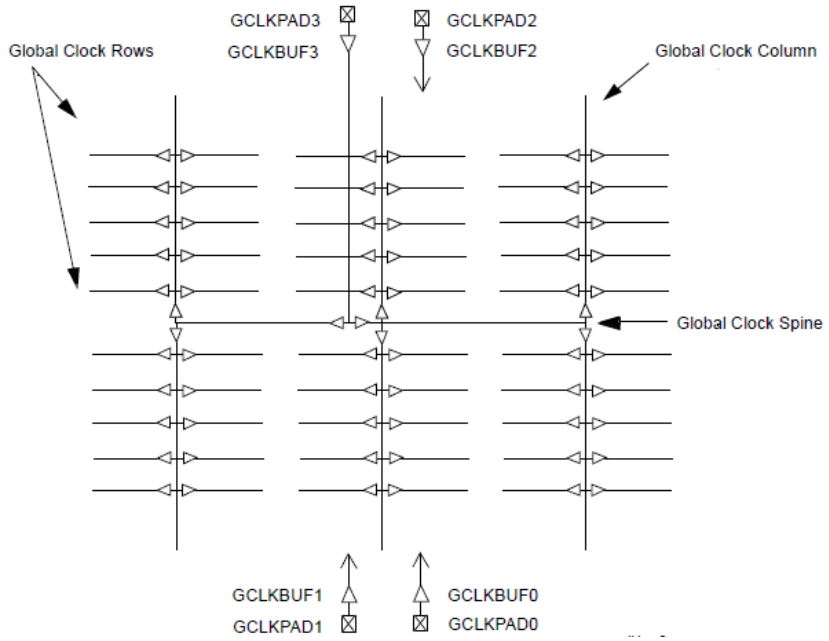


Figure 9: Global Clock Distribution Network

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin. Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

3.5Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clocknetworks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element.

Clock edges reach internal flip-flops one to four clock periods after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL

off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple BQVR300RH devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

3.6Boundary Scan

BQVR300RH devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device. The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the VCCO for Bank 2 should be 3.3 V.

Otherwise, TDO switches rail-to-rail between ground and VCCO. Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 5 lists the boundary-scan instructions supported in BQVR300RH FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Table 5: Boundary Scan Instructions

Boundary-Scan Command	**Binary Code(4:0)**	**Description**
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE/PRELOAD	00001	Enables boundary-scan SAMPLE/PRELOAD operation
USER 1	00010	Access user-defined

		register 1
USER 2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for read operations.
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	3-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	reserved instructions

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

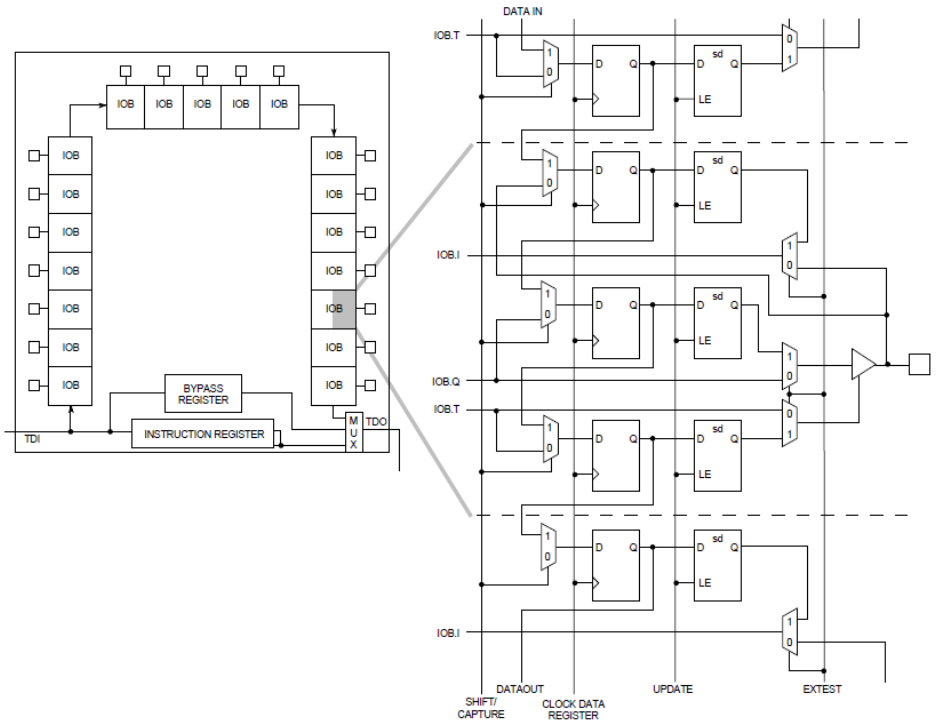


Figure 10: Boundary Scan Logic

Figure 10 is a diagram of the BQVR300RH boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Instruction Set

The boundary scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in Table 5.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only.

Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively.

For these instructions, two corresponding pins (TDO1 and TDO2) allow user scan data to be shifted out of TDO. Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

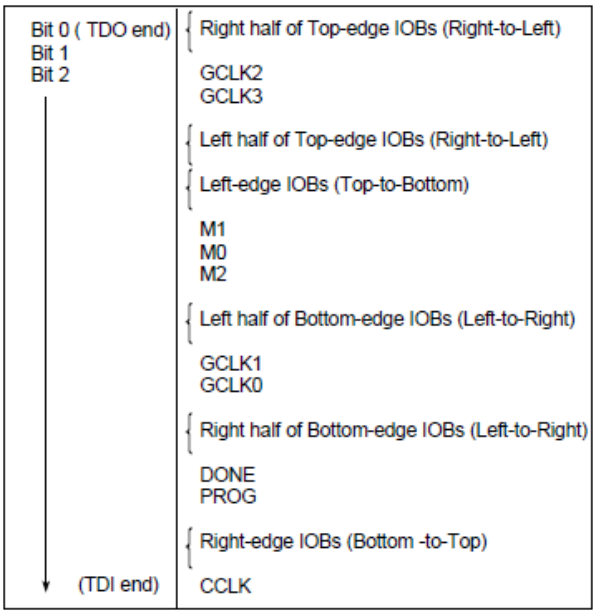


Figure 11: Boundary Scan Bit Sequence

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 11.

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined. The IDCODE of BQVR300RH is: v0620093

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code is embedded in the bitstream during bitstream generation and is valid only after configuration.

Including Boundary Scan in a Design

Since the boundary scan pins are dedicated, no special element needs to be added

to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the boundary scan symbol and connect the necessary pins as appropriate.

3.7Development System

BQVR300RH FPGAs are supported by the Xilinx ISE tools. The basic methodology for BQVR300RH design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Modelsim), while BMTI provides proprietary architecture-specific tools for implementation.

The development system is integrated under the ISE software, providing designers with a common user interface regardless of their choice of entry and verification tools.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the ISE software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the ISE provides interfaces to the following synthesis design environments.

• FPGA Express

• XST

• Synplify

For schematic design entry, the ISE provides interfaces to the following schematic-capture design environments.

Third-party vendors support many other environments. A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

BQVR300RH supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers,

decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process.

User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry.

The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific

timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because BQVR300RH devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

4. Configuration

BQVR300RH are configured by loading configuration data into the internal configuration memory. Some of the pins used for this are dedicated configuration pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- PROGRAM pin
- DONE pin
- Boundary-scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or it can be generated externally and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these

pins can require a VCCO of 3.3 V to permit LVTTL operation. All the pins affected are in banks 2 or 3.

After BQVR300RH device is configured, unused IOBs function as 3-state OBUFTs with weak pull downs.

4.1 Configuration Modes

BQVR300RH supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of

having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 6.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

Table 6: Configuration Codes

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial Dout	Configuration Pull-ups
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary-scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary-scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

4.2Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for mixed configuration chains. This change was made to improve serial configuration rates for BQVR300RH-only chains.

Figure 12 shows a full master/slave system. A BQVR300RH device in slave-serial mode should be connected as shown in the third device from the left.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave-serial the default mode if the pins are left unconnected. Figure 13 shows slave-serial configuration timing.

Table 7 provides more detail about the characteristics shown in Figure 13. Configuration must be delayed until the INIT pins of all daisy-chained FPGAs are High.

Table 7: Master/Slave Serial Mode Programming Switching

	Description	Figure References	Symbol	Value	Units
CCLK	DIN setup/hold, slave mode	1/2	TDCC/TCCD	5.0 / 0	ns, min
	DIN setup/hold, master mode	1/2	TDSCK/TCKDS	5.0 / 0	ns, min
	DOUT	3	TCCO	12.0	ns, max
	High time	4	TCCH	5.0	ns, min
	Low time	5	TCCL	5.0	ns, min
	Maximum Frequency		FCC	30	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% –45%	

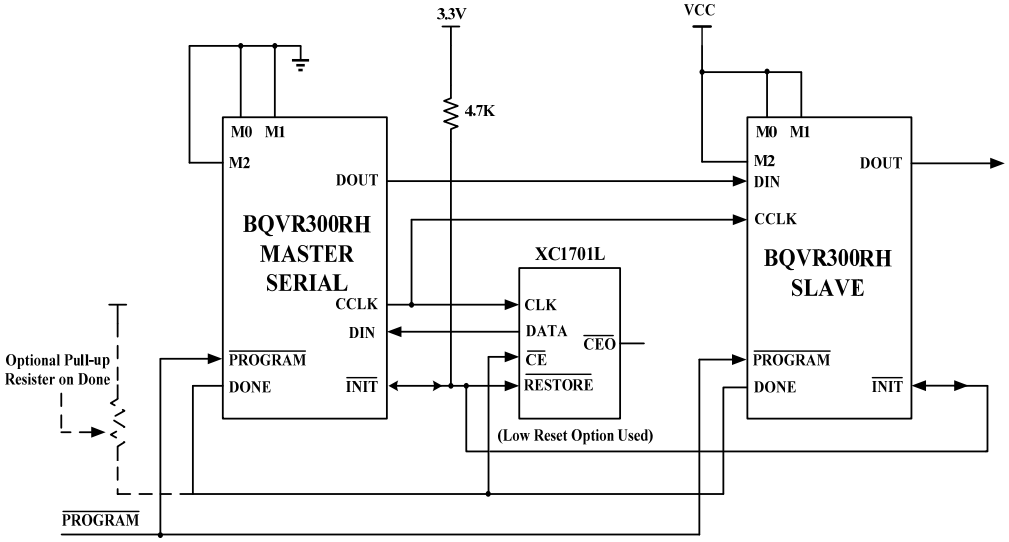


Figure 12: Master/Slave Serial Mode Circuit Diagram

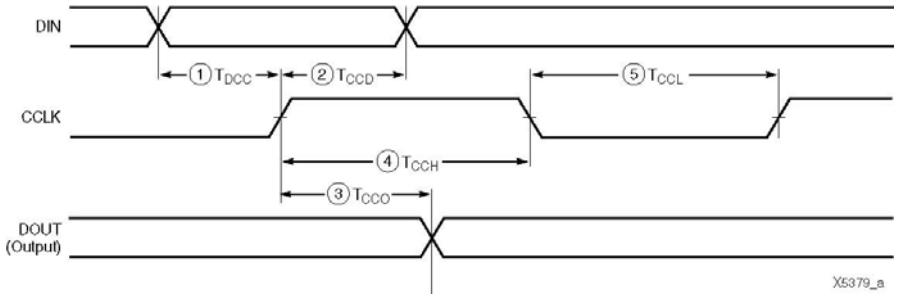


Figure 13: Slave-Serial Mode Programming Switching Characteristics

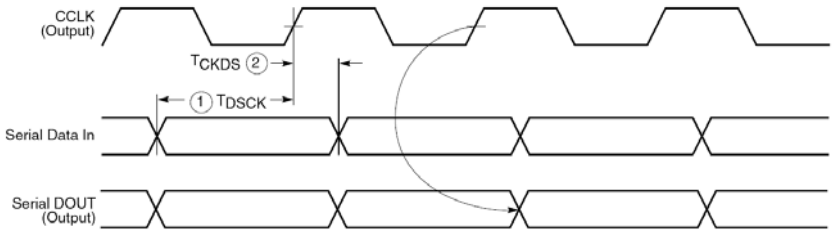


Figure 14: Master-Serial Mode Programming Switching Characteristics

4.3Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a BMTI Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be

selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any CCLK (Output) Serial Data In Serial DOUT (Output) On power-up, the CCLK frequency is 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The CCLK frequency set by software options is not actual frequency. The master CCLK frequency has deviations between the test value and the design one, for more information refer to appendix IV.

Figure 12 shows a full master/slave system. In this system, the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The PROM RESET pin is driven by INIT, and the CE input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

Figure 14 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 7 shows the timing information for Figure 13 and Figure 14.

The sequence of operations necessary to configure a BQVR300RH serially appears in Figure 15.

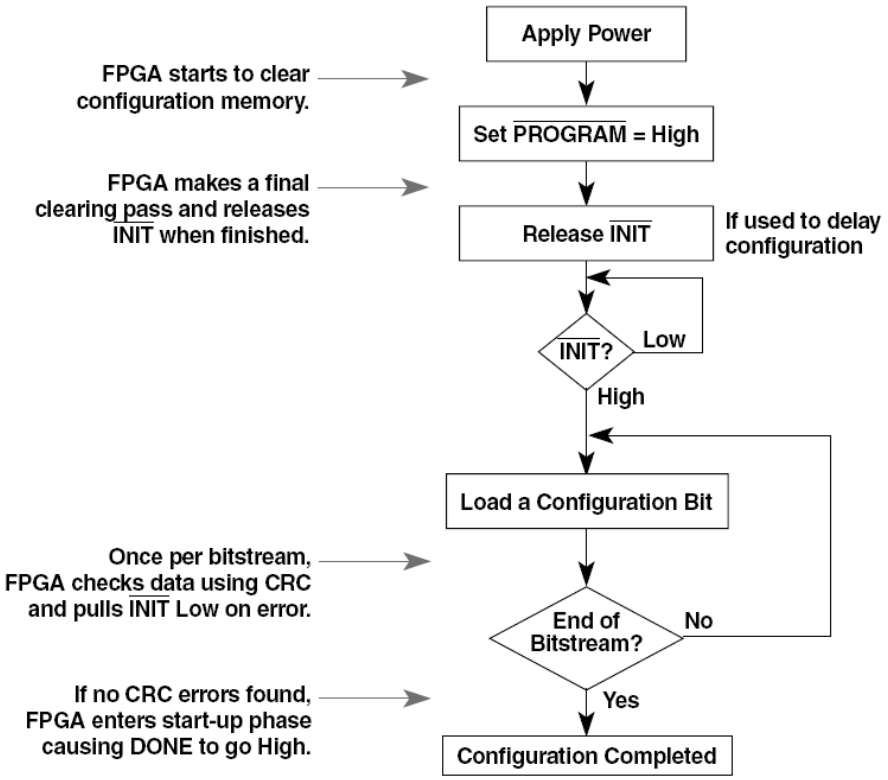


Figure 15: Serial Configuration Flowchart

4.4SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select (CS) signal and a Write signal (WRITE). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If WRITE is not asserted, configuration data is read out of the FPGA as part of a readback operation.

In the SelectMAP mode, multiple BQVR300RH devices can be chained in parallel. DATA pins (D7:D0), CCLK, WRITE, BUSY, PROGRAM, DONE, and INIT can be connected in parallel between all the FPGAs. Note that the data is organized with the MSB of each byte on pin DO and the LSB of each byte on D7. The CS pins are kept separate, insuring that each FPGA can be selected individually. WRITE should be Low before loading the first bitstream and returned High after the last device has been programmed. Use CS to select the appropriate FPGA for loading the bitstream and sending the configuration data. at the end of the bitstream, deselect the loaded device and select the next target FPGA by setting its CS pin High. A

free-running oscillator or other externally generated signal can be used for CCLK. The BUSY signal can be ignored for frequencies below 50 MHz. BQVR300RH Configuration and Readback. Once all the devices have been programmed, the DONE pin goes High.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback. Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O. Multiple BQVR300RH can be configured using the Select-MAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data. See Table 8 for SelectMAP Write Timing Characteristics.

Table 8: SelectMAP Write Timing Characteristics

	Description	Value	Symbol	Value	Units
CCLK	D0-7 Setup/Hold	1/2	TSMDCC/TSMCCD	5.0 / 1.7	ns, min
	CS Setup/Hold	3/4	TSMCSCC/TSMCCCS	7.0 / 1.7	ns, min
	WRITE Setup/Hold	5/6	TSMCCW/TSMWCC	7.0 / 1.7	ns, min
	BUSY Propagation Delay	7	TSMCKBY	12.0	ns, max
	Maximum Frequency		FCC	30	MHz, max
	Maximum Frequency with no handshake		FCCNH	20	MHz, max

Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of CS, illustrated in Figure 16.

1. Assert WRITE and CS Low. Note that when CS is asserted on successive CCLKs, WRITE must remain either asserted or de-asserted. Otherwise an abort will be initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while CS is Low and WRITE is High. Similarly, while WRITE is High, no more that one CS should be asserted.
3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock.

If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.

4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert CS and WRITE.

A flowchart for the write operation appears in Figure 17.Note that if CCLK is slower than FCCNH, the FPGA never asserts BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

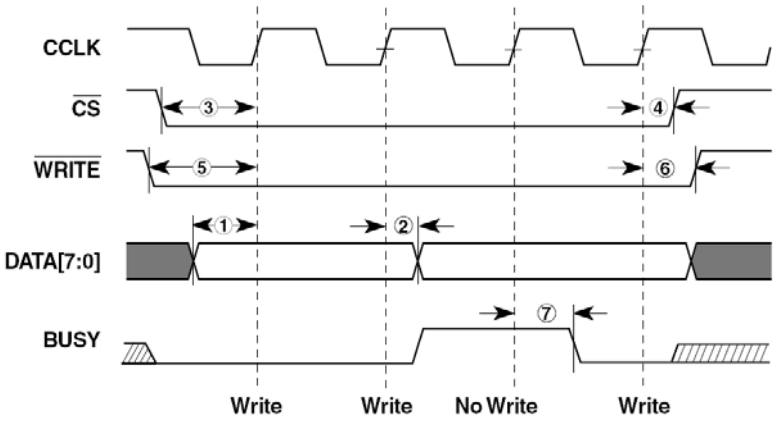


Figure 16: Write Operations

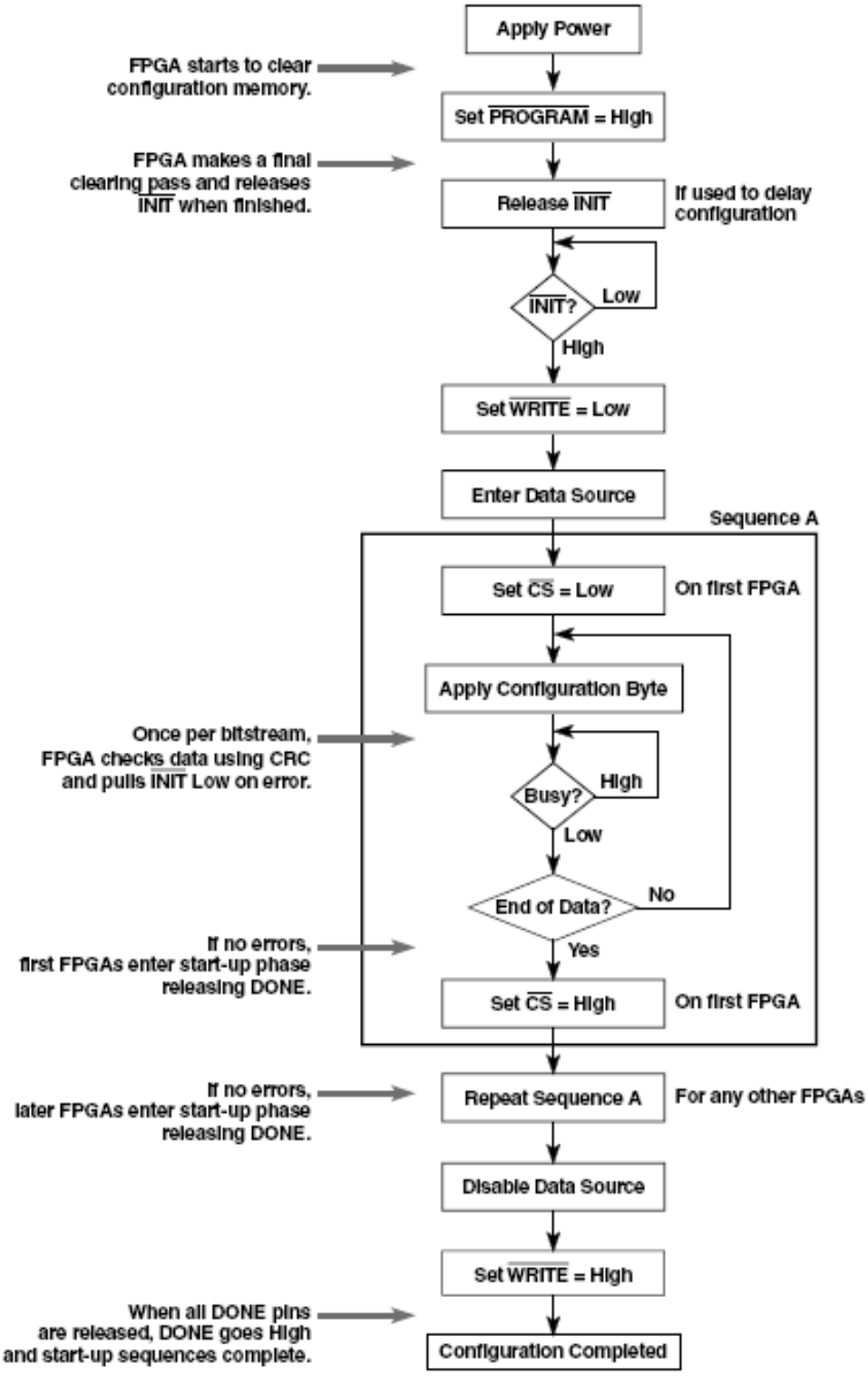


Figure 17: SelectMAP Flowchart for Write Operation

Abort

During a given assertion of CS, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device will remain BUSY until the aborted operation has completed. Following an abort, data

is assumed to be unaligned to word boundaries, and the FPGA requires a new synchronization word prior to accepting any new packets. To initiate an abort during a write operation, de-assert WRITE. At the rising edge of CCLK, an abort is initiated, as shown in Figure 18.

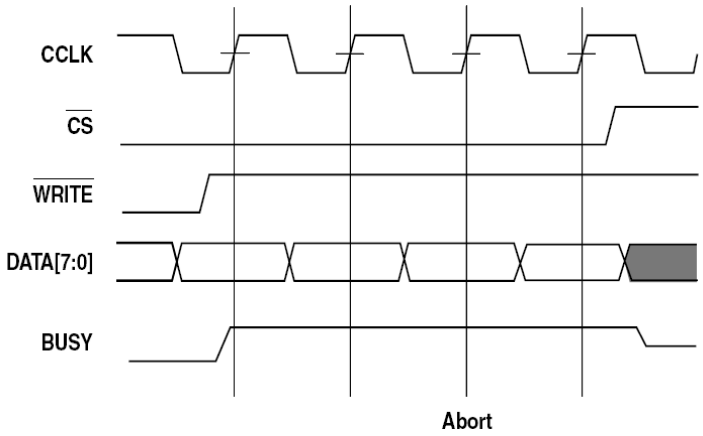


Figure 18: SelectMAP Write Abort Waveforms

4.5Boundary-Scan Mode

In the boundary-scan mode, no non-dedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the startup sequence
8. Return to RTI Configuration and readback via the TAP is always available.

The boundary-scan mode is selected by a <101> or<001> on the mode pins (M2, M1, M0).

4.6Configuration Sequence

The configuration of BQVR300RH devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting PROGRAM. The end of the memory-clearing phase is signalled by INIT going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 19. The corresponding timing characteristics are listed in Table 9 .

4.7Delaying Configuration

INIT can be held Low using an open-drain driver. An open-drain is required since INIT is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

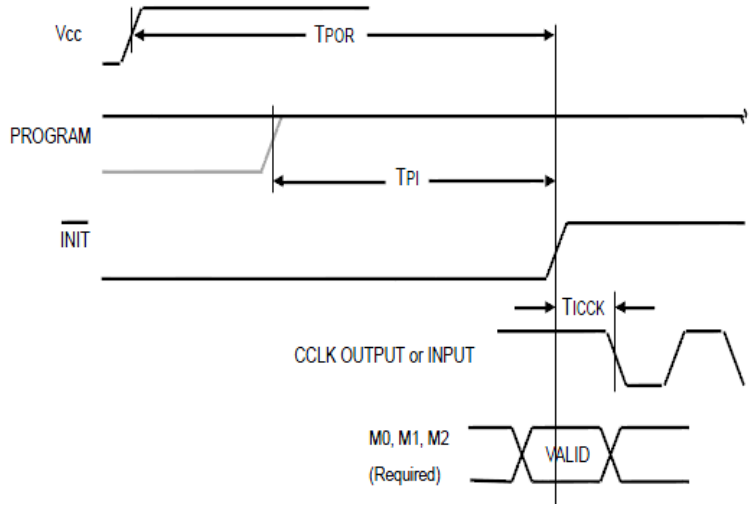


Figure 19: Power-Up Timing Configuration Signals

Table 9: Power-up Timing Characteristics

Description	Symbol	Value	Units
Power-on Reset	TPOR	20.0	ms,max

Description	Symbol	Value	Units
Program Latency	TPL	30.0	us,max
CCLK (output)	TICCK	0.5	us, min
Delay		4.0	us, max
Program Pulse Width	TPROGRAM	300	ns, min

4.8Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed. In addition, the GTS, GSR, and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start in synchronism. The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

5. Electrical Characteristics

5.1DC Characteristics Absolute Maximum Ratings

Table 10: Absolute Maximum Ratings

Symbol	Description(1)		Value	Units
VCCINT	Supply voltage relative to GND(2)		–0.5 to 3.0	V
VCCO	Supply voltage relative to GND(2)		–0.5 to 4.0	V
VREF	Input Reference Voltage		–0.5 to 3.6	V
VIN	Input voltage relative to GND(3)	Using VREF	–0.5 to 3.6	V
		Internal threshold	–0.5 to 5.5	V
VTS	Voltage applied to 3-state output		–0.5 to 5.5	V
VCC	Longest Supply Voltage Rise Time from 1V-2.375V		50	ms
TSTG	Storage temperature (ambient)		–65 to +150	℃
TJ	Junction temperature		+125	℃

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
2. Power supplies can turn on in any order.
3. For protracted periods (e.g., longer than a day), VIN should not exceed VCCO by more than 3.6V.

5.2Recommended Operating Conditions

Table 11: Recommended Operating Conditions

Symbol	Description	Min	Max	Units
VCCINT(1)	Input Supply voltage relative to GND, TJ = -55 ℃ to +125℃	2.5 – 5%	2.5 + 5%	V
VCCO(4)	Supply voltage relative to GND, TJ = -55 ℃ to +125℃	1.4	3.6	V
T_{IN}	Input signal transition time		250	ns

Notes:

1. Correct operation is guaranteed with a minimum VCCINT of 2.375 V (Nominal VCCINT –5%). Below the minimum value, all delay parameters increase by 3% for each 50-mV reduction in VCCINT below the specified range.
2. At junction temperatures above those listed as Operating Conditions, delay parameters do increase.
3. Input and output measurement threshold is ~50% of VCC.
4. Min and Max values for VCCO are I/O Standard dependant.

5.3DC Characteristics Over Recommended Operating Conditions

Table 12: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Max	Units
VDRINT	Data Retention VCCINT Voltage (below which configuration data can be lost)	2.0		V

Symbol	Description	Min	Max	Units
VDRIO	Data Retention VCCO Voltage (below which configuration data can be lost)	1.2		V
ICCINTQ	Quiescent VCCINT supply current(1)		250	mA
ICCOQ	Quiescent VCCO supply current(1)		10	mA
IREF	VREF current per VREF pin		20	μA
IL	Input or output leakage current (2)	–10	+10	μA
C_{IN}	Input capacitance (sample tested)		20	pF
IRPU	Pad pull-up (when selected) @ Vin = 0 V, VCCO = 3.3 V (sample tested)	Note (2)	0.25	mA
IRPD	Pad pull-down (when selected) @ Vin = 3.6 V (sample tested)	Note (2)	0.7	mA

Notes:

1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits. After radiation, IL of GCLK pins and IRPD of some pins may get larger which just has tiny impact in user function.

5.4Power-On Power Supply Requirements

BQVR300RH require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device(1) from 0 V. For more information about power-on requirements see appendix II.

Table 13: Power-On Power Supply Requirements

Product	Description(2)	Current Requirement(1,3)
BQVR300RH	Minimum required current supply	2 A

Notes:

1. Ramp rate used for this specification is from 0 - 2.7 VDC. Peak current occurs on

or near the internal power-on reset threshold and lasts for less than 1 ms at room temperature.

2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents can result if ramp rates are forced to be faster.

5.5DC Input and Output Levels

Values for VIL and VIH are recommended input voltages. Values for IOL and IOH are guaranteed output currents over the recommended operating conditions at the VOL and VOH test points. The selected standards are tested at minimum VCCO for each standard with the respective VOL and VOH voltage levels shown in table14.

Table 14: DC Input and Output Levels

Input/Output		VIL	VIH		VOL	VOH	IOL	IOH
Standard	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL	– 0.5	0.8	2.0	5.5	0.4	2.4	24	–24
LVCMOS2	– 0.5	.7	1.7	5.5	0.4	1.9	12	–12
PCI, 3.3 V	– 0.5	44% VCCINT	60% VCCINT	VCCO + 0.5	10% VCCO	90% VCCO	Note 2	Note 2
PCI, 5.0 V	– 0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	– 0.5	VREF – 0.05	VREF + 0.05	3.6	0.4	n/a	40	n/a
GTL+	– 0.5	VREF – 0.1	VREF + 0.1	3.6	0.6	n/a	36	n/a
HSTL I(3)	– 0.5	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCO – 0.4	8	–8
HSTL III	– 0.5	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCO – 0.4	24	–8
HSTL IV	– 0.5	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCO – 0.4	48	–8
SSTL3 I	– 0.5	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.6	VREF + 0.6	8	–8
SSTL3 II	– 0.5	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.8	VREF + 0.8	16	–16
SSTL2 I	– 0.5	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.61	VREF + 0.61	7.6	–7.6
SSTL2 II	– 0.5	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.80	VREF + 0.80	15.2	–15.2
CTT	– 0.5	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.4	VREF + 0.4	8	–8
AGP	– 0.5	VREF – 0.2	VREF + 0.2	3.6	10% VCCO	90% VCCO	Note 2	Note 2

Notes: 1.Tested according to the relevant specifications.

6. Package Information

6.1Special Pin Definitions

Table 15: Special Purpose Pins

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides header information to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0 - D7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.

Pin Name	Dedicated Pin	Direction	Description
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE 1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
VCCINT	Yes	Input	Power-supply pins for the internal core logic.
VCCO	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
VREF	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

6.2Pinout Information

Table 16: BQVR300RH Pinout Tables (CQFP228)

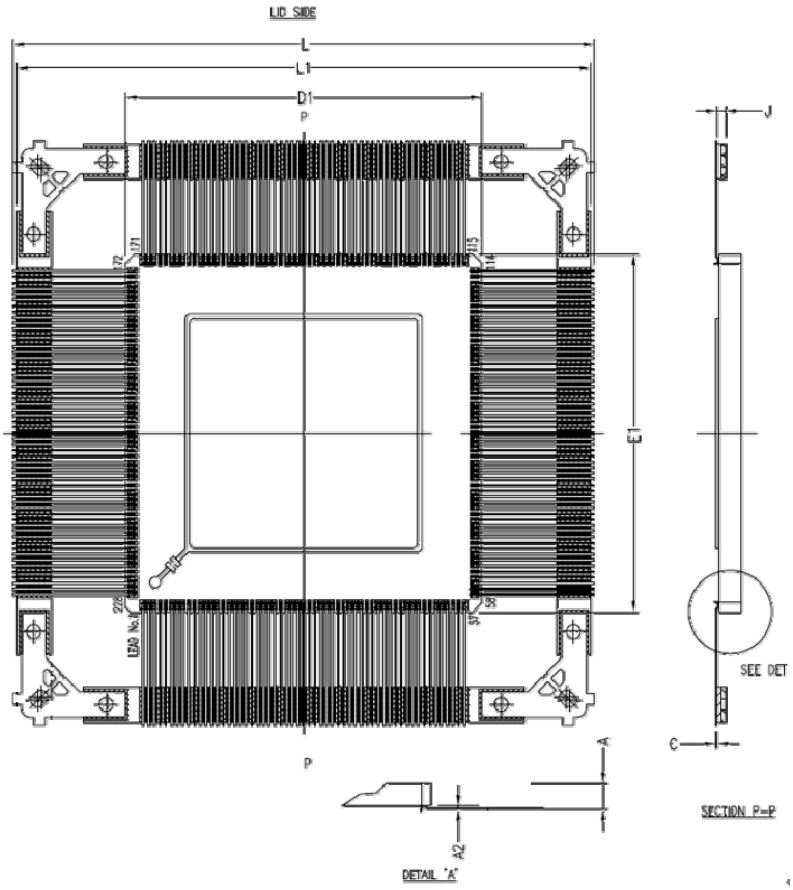
PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name
1	GND	58	VCCO	115	VCCO	172	TDO
2	TMS	59	M2	116	PROGRAM	173	GND
3	I/O	60	I/O	117	I/O_INIT	174	TDI
4	I/O	61	I/O	118	I/O_D7	175	I/O_CS
5	I/O_VREF_7	62	I/O	119	I/O	176	I/O_WRITE
6	I/O	63	I/O_VREF_5	120	I/O_VREF_3	177	I/O
7	I/O	64	I/O	121	I/O	178	I/O_VREF_1
8	GND	65	I/O	122	I/O	179	I/O
9	I/O_VREF_7	66	GND	123	GND	180	GND
10	I/O	67	I/O_VREF_5	124	I/O_VREF_3	181	I/O_VREF_1
11	I/O	68	I/O	125	I/O	182	I/O
12	I/O_VREF_7	69	I/O	126	I/O	183	I/O
13	I/O	70	I/O_VREF_5	127	I/O_VREF_3	184	I/O_VREF_1
14	GND	71	I/O	128	I/O_D6	185	I/O

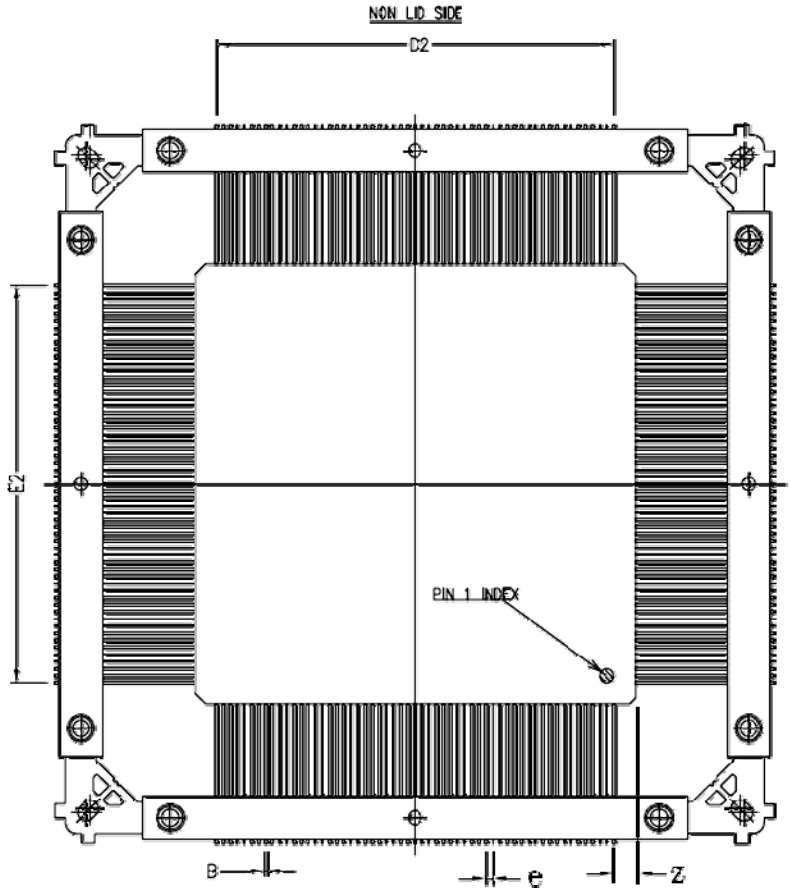
PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name
15	VCCINT	72	GND	129	GND	186	GND
16	I/O	73	VCCINT	130	VCCINT	187	VCCINT
17	I/O	74	I/O	131	I/O_D5	188	I/O
18	VCCO	75	I/O	132	I/O	189	I/O
19	I/O	76	VCCO	133	VCCO	190	I/O
20	I/O	77	I/O	134	I/O	191	VCCO
21	I/O_VREF_7	78	I/O	135	I/O	192	I/O
22	I/O	79	I/O_VREF_5	136	I/O_VREF_3	193	I/O
23	I/O	80	I/O	137	I/O_D4	194	I/O_VREF_1
24	I/O	81	I/O	138	I/O	195	I/O
25	I/O	82	I/O	139	I/O	196	I/O
26	I/O_TRDY	83	VCCINT	140	VCCINT	197	I/O
27	GND	84	GCK1	141	I/O_TRDY	198	I/O
28	VCCO	85	VCCO	142	VCCO	199	GCK2
29	I/O_TRDY	86	GND	143	GND	200	GND
30	VCCINT	87	GCKO	144	I/O_IRDY	201	VCCO
31	I/O	88	I/O	145	I/O	202	GCK3
32	I/O	89	I/O	146	I/O	203	VCCINT
33	I/O	90	I/O	147	I/O	204	I/O
34	I/O_VREF_6	91	I/O	148	I/O_D3	205	I/O
35	I/O	92	I/O_VREF_4	149	I/O_VREF_2	206	I/O
36	I/O	93	I/O	150	I/O	207	I/O_VREF_0
37	VCCO	94	I/O	151	I/O	208	I/O
38	I/O	95	VCCO	152	VCCO	209	I/O
39	I/O	96	I/O	153	I/O	210	VCCO
40	I/O	97	I/O	154	I/O	211	I/O
41	VCCINT	98	I/O	155	I/O_D2	212	I/O

PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name
42	GND	99	VCCINT	156	VCCINT	213	I/O
43	I/O	100	GND	157	GND	214	VCCINT
44	I/O_VREF_6	101	I/O	158	I/O_D1	215	GND
45	I/O	102	I/O_VREF_4	159	I/O_VREF_2	216	I/O
46	I/O	103	I/O	160	I/O	217	I/O_VREF_0
47	I/O_VREF_6	104	I/O	161	I/O	218	I/O
48	GND	105	I/O_VREF_4	162	I/O_VREF_2	219	I/O
49	I/O	106	GND	163	GND	220	I/O_VREF_0
50	I/O	107	I/O	164	I/O	221	GND
51	I/O_VREF_6	108	I/O	165	I/O	222	I/O
52	I/O	109	I/O_VREF_4	166	I/O_VREF_2	223	I/O
53	I/O	110	I/O	167	I/O	224	I/O_VREF_0
54	I/O	111	I/O	168	I/O_DIN_D0	225	I/O
55	M1	112	I/O	169	I/O_DOUT_BUSY	226	I/O
56	GND	113	GND	170	CCLK	227	TCK
57	M0	114	DONE	171	VCCO	228	VCCO

6.3Package Outline

The outline dimensions of BQVR300RH are shown in figure 20:


LID SIDE
L
L1
D1
P
J
E1
SEE DET
C
A
A2
DETAIL "A"
SECTION P-P


NON LID SIDE
D2
E2
PIN 1 INDEX
B
e
Z

Units：mm

Symbol	Value		
	Min	Typical	Max
A	—	—	3.6
A2	—	—	0.8
B	0.17	—	0.30
C	0.10	—	0.23
D1/E1	38.87	—	39.87
D2/E2	—	35.56	—
e	0.62	—	0.65
J	—	0.9	—
L	—	—	65.50
L1	62.99	—	64.26
Z	—	—	2.5

Figure 20: Outline Dimensions of BQVR300RH

Appendix I Electrical performance characteristics

Electrical performance characteristics

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤VCCO ≤ 3.6 V (-55°C≤ TC≤+125°C)	Group A Subgroups	Limits		units
				Min	Max	
Data retention VCCINT voltage below which configuration may be lost	V_{DRINT}		1，2，3	2.0		V
Data retention VCCO voltage below which configuration may be lost	V_{DRIO}			1.2		V
High-level output voltage	V_{OH}	I_{OH}=-24mA，V_{CCO}=3.0V，V_{CCINT}=min，LVTTL		2.4		V
Low-level output voltage	V_{OL}	I_{OL}=24mA，V_{CCO}=3.0V，V_{CCINT}=min，LVTTL			0.4	V
Quiescent VCCINT Supply current	I_{CCINTQ}				250	mA
Quiescent VCCO Supply current	I_{CCOQ}		1，2，3		10	mA
Input or output leakage current[h]	I_L			-10	10	μA

VREF current per VREF pin	I_{REF}				20	μA
Input capacitance	C_{in}/ C_{out}	f =1.0MHz， V_{OUT}=0V Tc=25℃	4		20	pF
Pad pull-up (when selected)	I_{RPU}	V_{IN}=0V， V_{CCINT}=2.5V， V_{CCO}=3.3V, sample test	1，2，3		0.25	mA
Pad pull-down (when selected)	I_{RPD}	V_{IN}=3.6V， V_{CCINT}=2.5V， V_{CCO}=3.3V, sample test			0.15	mA
Functional test	FT	f=10MHz，V_{CCINT}=2.5V， Vcco =3.3V	7，8A，8B			

Electrical performance characteristics - Continued

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤ VCCO ≤3.6 V (-55°C≤ TC ≤ +125°C)	Group A Subgroups	Limits		units
				Min	Max	
lOB Input Switching Characteristics Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "lOB Input Switching Characteristics Standard Adjustments" below this section.						
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	1.0	ns
Pad to I output, with delay	T_{IOPID}			—	1.9	
Pad to output IQ via transparent latch, no delay	T_{IOPLI}			—	2.0	
Pad to output IQ via transparent latch, with delay	T_{IOPLID}			—	5.1	
Sequential Delays						
Clock CLK to output IQ	T_{IOCKIQ}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	0.8	ns
Setup and Hold Times with respect to Clock CLK at IOB input register[b]						
Pad, no	T_{IOPICK}/	2.375V≤V_{CCINT}≤2.625V，	9，10，11	2.0/0	—	ns

delay	T_{IOICKP}	1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃				

Electrical performance characteristics - Continued

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤ VCCO ≤3.6 V (-55°C≤ TC ≤ +125°C)	Group A Subgroups	Limits		Units
				Min	Max	
Setup and Hold Times with respect to Clock CLK at IOB input register[b]						
Pad, with delay	$T_{IOPICKD}$/ $T_{IOICKPD}$	2.375V≤V_{CCINT}≤2.625 V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	5.0/0	—	ns
ICE input	T_{IOCECK}/ $T_{IOCKICE}$			1.0/0	—	
SR Input (IFF,synchronous)	$T_{IOSRCKI}$/ $T_{IOCKISR}$		9，10，11	1.3/0	—	ns
Set / Reset Delays						
SR input to IQ(asynchronous)	T_{IOSRIQ}	2.375V≤V_{CCINT}≤2.625 V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	1.8	ns
GSR to output IQ	T_{GSRQ}		9，10，11	—	12.5	ns
lOB Output Switching Characteristics[a] Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "lOB Output Switching Characteristics Standard Adjustments" below this section.						
Propagation Delays						
O input to Pad	T_{IOOP}	2.375V≤V_{CCINT}≤2.625 V， 1.2V≤V_{CCO}≤3.6V，	9，10，11	—	3.5	ns
O input to Pad via transparent latch	T_{IOOLP}			—	4.0	

		-55℃≤T_A≤125℃				
3-State Delays						
T input to Pad highimpedanc	T_{IOTHZ}	2.375V≤V_{CCINT}≤2.625 V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	—	2.4	ns
T input to valid data on Pad	T_{IOTON}			—	3.7	
T input to Pad highimpedance via transparent latch	$T_{IOTLPHZ}$			—	3.0	
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$			—	4.2	
GTS to Pad high impedance[c]	T_{GTS}			—	6.3	

Electrical performance characteristics - Continued

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤ VCCO ≤3.6 V (-55°C≤ TC ≤ +125°C)	Group A Subgroups	Limits		Units
				Min	Max	
Sequential Delays						
Clock CLK to Pad	T_{IOCKP}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	3.5	ns
Clock CLK to Pad highimpedance (synchronous)[c]	T_{IOCKHZ}			—	2.9	
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}			—	4.1	
Setup and Hold Times before/after Clock CLK[b]						
O input	T_{IOOCK}/ T_{IOCKO}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	1.3/0	—	ns
O OCE input	$T_{IOOCECK}$/ $T_{IOCKOCE}$			1.0/0	—	
SR input (OFF)	$T_{IOSRCKO}$/ $T_{IOCKOSR}$			1.4/0	—	
3-State Setup Times, T input	T_{IOTCK}/ T_{IOCKT}			0.9/0	—	
3-State Setup Times, TCE input	$T_{IOTCECK}$/ $T_{IOCKTCE}$		9，10，11	1.1/0	—	ns
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}$/ $T_{IOCKTSR}$			1.3/0	—	
Set/Reset Delays						
SR input to Pad (asynchronous)	T_{IOSRP}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	4.6	ns
SR input to Pad highimpedance	T_{IOSRHZ}			—	3.9	

(asynchronous)						
SR input to valid data on Pad(asynchronous)	T_{IOSRON}			—	5.1	
Clock Distribution Guidelines **Global Clock Skew**						
Global clock skew between IOB flip-flops[d]	$T_{GSKEWIOB}$	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	0.18	ns

Electrical performance characteristics - Continued

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤ VCCO ≤3.6 V (-55°C≤ TC ≤ +125°C)	Group A Subgroups	Limits		Units
				Min	Max	
Clock Distribution Switching Characteristics GCLK IOB and Buffer						
Global clock pad to output	T_{GPIO}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	0.9	ns
Global Clock Buffer I input to O output	T_{GIO}			—	0.9	
CLB Switching Characteristics[a] Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer. **Combinatorial Delays**						
4-input function: F/G inputs to X/Y outputs	T_{ILO}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	0.8	ns
5-input function: F/G inputs to F5 output	T_{IF5}			—	0.9	
5-input function: F/G inputs to X output	T_{IF5X}			—	1.0	
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}			—	1.2	
6-input function: F5IN input to Y output	T_{F5INY}			—	0.5	
BY input to YB output	T_{BYYB}			—	0.7	
Setup and Hold times before/after Clock CLK[b]						
4-input function: F/G	T_{ICK}/T_{CKI}	2.375V≤V_{CCINT}≤2.625V，	9，10，11	—	1.5/0	ns

Inputs		1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃				
5-input function: *F/G* inputs	T_{IF5CK}/ T_{CKIF5}			—	1.7/0	
6-input function: F5IN input	T_{F5INCK} T_{CKF5IN}			—	1.2/0	
6-input function: F/G inputs via F6 MUX	T_{IF6CK} T_{CKIF6}			—	1.9/0	

Electrical performance characteristics - Continued

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤ VCCO ≤3.6 V (-55°C≤ TC ≤ +125°C)	Group A Subgroups	Limits		Units
				Min	Max	
Setup and Hold times before/after Clock CLK[b]						
BX/BY inputs	T_{DICK}/ T_{CKDI}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	—	0.8/0	ns
CE input	T_{CECK}/ T_{CKCE}			—	1.0/0	
SR/BY inputs (synchronous)	$T_{RCKTCKR}$			—	0.9/0	
CLOCK CLK						
Minimum Pulse Width, High	T_{CH}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	—	2.0	ns
Minimum Pulse Width, Low	T_{CL}			—	2.0	
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T_{RPW}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	—	3.3	ns
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}			—	1.4	
Delay from GSR to XQ/YQ outputs	T_{IOGSRQ}			—	12.5	
CLB Arithmetic Switching Characteristics[a] Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer. **Combinatorial Delays**						

F operand inputs to X via XOR	T_{OPX}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	—	1.0	ns
F operand input to XB output	T_{OPXB}			—	1.4	
F operand input to Y via XOR	T_{OPY}			—	2.0	
F operand input to YB output	T_{OPYB}			—	2.0	
F operand input to COUT output	T_{OPCYF}			—	1.5	
G operand inputs to Y via XOR	T_{OPGY}			—	1.2	
G operand input to YB output	T_{OPGYB}			—	2.1	

Electrical performance characteristics - Continued

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤ VCCO ≤3.6 V (-55°C≤ TC ≤ +125°C)	Group A Subgroups	Limits		Units
				Min	Max	
G operand input to COUT output	T_{OPCYG}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	1.6	ns
BX initialization input to COUT	T_{BXCY}			—	1.1	
CIN input to X output via XOR	T_{CINX}			—	0.6	
ClN input to XB	T_{CINXB}		9，10，11	—	0.1	ns
CIN input to Y via XOR	T_{CINY}			—	0.6	
ClN input to YB	T_{CINYB}			—	0.6	
CIN input to COUT output	T_{BYP}			—	0.2	
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T_{FANDXB}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	0.5	ns
F1/2 operand inputs to YB output via AND	T_{FANDYB}			—	1.1	
F1/2 operand inputs to COUT output via AND	T_{FANDCY}			—	0.6	
G1/2 operand inputs to YB output via AND	T_{GANDYB}			—	0.7	
G1/2 operand inputs to COUT output via AND	T_{GANDCY}			—	0.2	
Setup and Hold Times before/after Clock CLK[b]						
CIN input to FFX	T_{CCKX}/ T_{CKCX}	2.375V≤V_{CCINT}≤2.625V，	9，10，11	—	1.3/0	ns

CIN input to FFY	T_{CCKY}/ T_{CKCY}	1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃		—	1.4/0	

Electrical performance characteristics - Continued

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤ VCCO ≤3.6 V (-55°C≤ TC ≤ +125°C)	Group A Subgroups	Limits		Units
				Min	Max	
CLB SelectRAM Switching Characteristics[a] **Sequential Delays**						
Clock CLK to X/Y outputs(WE active)	T_{SHCKO}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	—	3.0	ns
Clock CLK to X/Y outputs				—	3.0	
Setup and Hold Times before/after Clock CLK[b]						
F/G address inputs	T_{AS}/T_{AH}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	0.7/0	—	ns
BX/BY data inputs (DIN)	T_{DS}/T_{DH}			0.9/0	—	
CE input (WE)	T_{WS}/T_{WH}			1.0/0	—	
Shift Register Mode						
BX/BY data inputs (DIN)	T_{SHDICK}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	0.9	—	ns
CE input (WS)	T_{SHCECK}			1.0	—	
Clock CLK						
Minimum Pulse Width, High	T_{WPH}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	3.1	—	ns
Minimum Pulse Width, Low	T_{WPL}			3.1	—	
Minimum clock period to meet address write cycle time	T_{WC}			6.2	—	
Shift Register Mode						
Minimum Pulse Width, High	T_{SRPH}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，	9，10，11	3.1	—	ns

Minimum Pulse Width, Low	T_{SRPL}	-55℃≤T_A≤125℃		3.1	—	
Block RAM Switching Characteristics[a] **Sequential Delays**						
Clock CLK to DOUT output	T_{BCKO}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	—	4.1	ns

Electrical performance characteristics - Continued

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤ VCCO ≤3.6 V (-55°C≤ TC ≤ +125°C)	Group A Subgroups	Limits		Units
				Min	Max	
Setup and Hold Times before/after Clock CLK[b]						
ADDR inputs	$T_{BACK/BCKA}$	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	1.5/0	—	ns
DIN inputs	$T_{BDCK/BCKD}$			1.5/0	—	
EN input	$T_{BECK/BCKE}$			3.4/0	—	
RST input	$T_{BRCK/BCKR}$			3.2/0	—	
WEN input	$T_{BWCK/BCKW}$			3.0/0	—	
Clock CLK						
Minimum Pulse Width, High	T_{BPWH}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	2.0	—	ns
Minimum Pulse Width, Low	T_{BPWL}			2.0	—	
CLKA CLKB setup time for different ports	T_{BCCS}			4.0	—	
TBUF Switching Characteristics Combinatorial Delays						
IN input to OUT output[a]	T_{IO}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃	9，10，11	0	—	ns
TRI input to OUT output high-impedance[a]	T_{OFF}			0.2	—	
TRI input to valid data on OUT output[a]	T_{ON}			0.2	—	
JTAG Test Access Port Switching Characteristics						
TMS and TDI Setup times before TCK[a]	T_{TAPTCK}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，	9，10，11	4.0	—	ns

TMS and TDI Hold times after TCK[a]	T_{CKTAP}	-55℃≤T_A≤125℃		2.0	—	
Output delay from clock TCK to output TDO[g]	T_{TCKDO}			—	11.0	
Maximum TCK clock frequency[g]	F_{TCK}			—	33	MHz

Electrical performance characteristics - Continued

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤ VCCO ≤3.6 V (-55°C≤ TC ≤ +125°C)	Group A Subgroups	Limits		Units
				Min	Max	
Pin-to-Pin Input Parameter Guidelines **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL**						
LVTTL-F12[g]	$T_{ICKOFDLL}$	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	3.6	ns
LVTTL-F12[g]	T_{ICKOFF}		9，10，11	—	5.9	ns
Minimum Clock to Ou **I/OStandard**				**Minimum**		
				With DLL	**Without DLL**	
LVTTL-S2[a e]	—	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	5.2	6.1	ns
LVTTL-S4[a e]	—			3.5	4.4	
LVTTL-S6[a e]	—			2.8	3.7	
LVTTL-S8[a e]	—			2.2	3.1	
LVTTL-S12[a e]	—			2.0	2.9	
LVTTL-S16[a e]	—			1.9	2.8	
LVTTL-S24[a e]	—			1.8	2.7	
LVTTL-F2[a e]	—			2.9	3.8	
LVTTL-F4[a e]	—			1.7	2.6	
LVTTL-F6[a e]	—			1.2	2.1	
LVTTL-F8[a e]	—			1.1	2.0	
LVTTL-F12[a e]	—			1.0	1.9	
LVTTL-F16[a e]	—			0.9	1.8	
LVTTL-F24[a e]	—			0.9	1.8	

LVCMOS2 [a]	—			1.1	2.0	
PCI33-3 [a]	—			1.5	2.4	
PCI33-5 [a]	—			1.4	2.3	
PCI66-3 [a]	—			1.1	2.0	
GTL [a]	—			1.6	2.5	
GTL+ [a]	—			1.7	2.6	
HSTL Ⅰ [a]	—			1.1	2.0	
HSTL Ⅲ [a]	—			0.9	1.8	
HSTL Ⅳ [a]	—			0.8	1.7	
SSTL2 Ⅰ [a]	—			0.9	1.8	
SSTL2 Ⅱ [a]	—			0.8	1.7	
SSTL3 Ⅰ [a]	—			0.8	1.7	
SSTL3 Ⅱ [a]	—			0.7	1.6	
CTT [a]	—			1.0	1.9	
AGP [a]	—			1.0	1.9	

Electrical performance characteristics - Continued

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤ VCCO ≤3.6 V (-55°C≤ TC ≤ +125°C)	Group A Subgroups	Limits		Units
				Min	Max	
Pin-to-Pin Input Parameter Guidelines[g] **Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL** Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards,adjust the setup time delay by the values shown in Input Delay Adjustments						
No Delay, Global Clock and IFF, with DLL	T_{PSDLL}/T_{PHDLL}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	2.1/-0.4	—	ns
Full Delay, Global Clock and IFF, without DLL	T_{PSFD}/T_{PHFD}			3.1/0.0	—	
DLL Timing Parameters[i]						
Input Clock Frequency (CLKDLLHF)[f]	$F_{CLKINHF}$	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	60	180	MHz
Input Clock Frequency (CLKDLL)[f]	$F_{CLKINLF}$			25	90	
Input Clock Pulse Width(CLKDLLHF)[a]	$T_{DLLPWHF}$			2.4	—	ns
Input Clock Pulse Width (CLKDLL)[a]	$T_{DLLPWLF}$			3.0	—	
CLKDLLHF [a]						
Input Clock Period Tolerance	T_{IPTOL}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	1.0	ns
Input Clock Jitter (Cycle to Cycle)	T_{IJITCC}			—	±150	ps
Time Required for	T_{LOCK}	f_{CLKIN}＞60MHz		—	20	μs

DLL to Acquire Lock						
DLL Output skew (between any DLL output)	T_{SKEW}	2.375V≤V_{CCINT}≤2.625V，1.2V≤V_{CCO}≤3.6V，-55℃≤T_A≤125℃		—	±150	ps
DLL Output long term phase differential	T_{OPHASE}			—	±100	ps
DLL Output jitter cycle to cycle	T_{OJITCC}			—	±60	ps

Electrical performance characteristics - Continued

Test	Symbol	Conditions Limits 2.375 V ≤VCCINT ≤2.625 V 1.2 V ≤ VCCO ≤3.6 V (-55°C≤ TC ≤ +125°C)	Group A Subgroups	Limits		Units
				Min	Max	
CLKDLL [a]						
Input Clock Period Tolerance	T_{IPTOL}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃	9，10，11	—	1.0	ns
Input Clock Jitter (Cycle to Cycle)	T_{IJITCC}			—	±300	ps
Time Required for DLL to Acquire Lock	T_{LOCK}	f_{CLKIN}＞60MHz	9，10，11	—	20	μs
DLL Output skew (between any DLL output)	T_{SKEW}	2.375V≤V_{CCINT}≤2.625V， 1.2V≤V_{CCO}≤3.6V， -55℃≤T_A≤125℃		—	±150	ps
DLL Output long term phase differential	T_{OPHASE}			—	±100	
DLL Output jitter cycle to cycle	T_{OJITCC}			—	±60	

a The parameter is design guaranteed and should not included in qualification test.

b A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", however, if a "0" is listed, there is no positive hold time.

c 3-state turn-off delays should not be adjusted.

d These clock-skew delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

e S= Slow Slew Rate, F= Fast Slew Rate

f The parameter should included in qualification test.

g The parameter isn't test now because current test condition can't meet the accuracy demand, if the test condition is improved and can cover the test accuracy, the parameter should be test.

h Special pins or multifunction pins may not included in qualification test.

i After Total Ionizing Dose test the max lockable frequency may decrease by 5%.

Appendix II Application Notes

- Master CCLK Frequency

In Master Serial configuration mode, the CCLK frequency driven by BQVR300RH is correlated to the OSCFSEL-Specified Master CCLK Frequencies set by the ISE design suit. The actual Master CCLK Frequency is much smaller than the setting value. For example, when the ISE-set Master CCLK frequency is 60MHz, the practical Master CCLK Frequency driven by BQVR300RH is about 24MHz. Because of the structures of the internal oscillators，master CCLK frequency is accurate to ±45%，and so is Xilinx XQVR300. If the configuration time matters for designer, the master CCLK Frequency deviation should be considered, for more information refer to appendix IV.

- Initialization

In the setup process, INIT_B is internally driven Low during initialization, then released after T_{POR}. The release time of Initial depends on the internal oscillators of FPGA. The T_{POR} of BQVR300RH is 10ms – 20ms, which is larger than XQVR300.

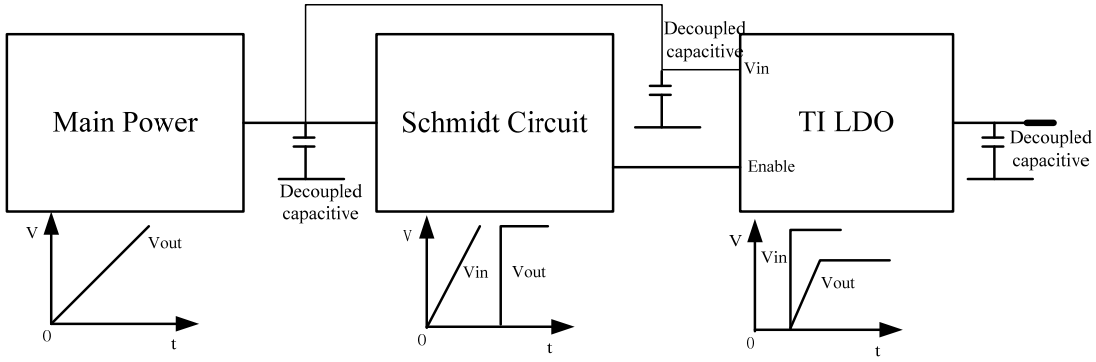
- Power Matching and Power-on Circuit

The Power-On Surge is the current that an SRAM-based FPGA draws upon first applying power. When the FPGA powers up, but before initialization, the RAM cells are briefly in a random state, which results in the POS current draw during power-on. All SRAM-based FPGAs require a minimum supply current to ensure a successful power up. The POS current is very large in size, but only lasts a short period of time (usually on the order of milliseconds). The POS current is related to junction temperatures. As a result, power adaptability tests at whole temperature ranges are required during initial stage of design.

The power-on current can be significant for high performance FPGAs, particularly since they employ extensive buffering for fast signal switching and propagation. During power-up, this buffering creates additional current paths between power and ground. Most FPGA manufactures publish power-on current specifications. The POS specification of BQVR300RH guarantees successful power-on when the following conditions are met: (1) The VCCINT power supply has the ability to continuously output 2A current and should only be used for one FPGA; (2) The VCCINT rise time should be less than 1ms; (3) VCCINT rises steadily from GND to

2.5V (no negative dips in the voltage, no shelf in power-on voltage profile); (4) PCB-level power adaptability tests at whole temperature ranges are required during initial stage of design.

The figure below shows a reference design in which a schmidt circuit is used to delay the LDO enable signal till the LDO's input voltage is enough high. The value of decoupled capacitance should be chosen carefully if the capacitance is too large the VCCINT rise time may exceed the required value.



Appendix III Common Mistakes

- DONE pin

Example：some users once connected a 4.7KΩ pull up resistor to DONE pin, as a result BQVR300RH failed in startup sequence and had no function even the DONE pin was high.

Pull up resistor connected to Done pin must be 330Ω otherwise the device may not startup successfully. If the pull up resistor connected to Done pin is not available in PCB, an alternative solution is to choose “drive done pin high” or “enable internal done pipe” in startup options of ISE.

- CS pin and Write pin

Example：some users thought the CS pin and the Write pin was useless in none-SelectMAP mode, and connected those two pins with uncertain logic state, but the master serial mode configuration was failed for the uncertain state of the CS pin and the Write pin.

Under any configuration mode cs pin and write pin should tied to a constant logic otherwise the configuration may fail. Users may think cs and write are useless if the configuration mode isn’t SelectMAP mode. Be attention that even if not in SelectMAP mode the logic changes in cs pin and write pin may cause the device shut down during the configuration.

- DLL reset and locked signal

Example: some users didn’t wait for the DLL being locked, as a result the initial disordered clocks made their function abnormal.

The RST pin, active High, must either connect to a dynamic signal or tied to ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer de-skew with respect to one another. For these reasons, rarely use the reset pin unless reconfiguring the device or changing the input frequency.

In order to achieve lock, the DLL may need to sample several thousand clock cycles. Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not

valid and can exhibit glitches, spikes, or other spurious movement.

- Initializing reset

Example: some users reset their BQVR300RH function after power on, but the reset signal was disabled before the DONE pin went high, as a result the function was not really reset.

Configuration costs a period of time, during the process BQVR300RH has no function. If the design need a initializing reset, please make sure the reset is active after the DONE pin goes high which indicates that the configuration is finished.

Appendix IV Master CCLK Frequency for Reference Only

OSCFSEL	ISE-set Master CCLK frequency (MHz)	practical Master CCLK Frequency (MHz)
101101	60	24.4
110100	55	17.9
101010	51	19.6
110011	45	14.1
100111	41	14.3
110010	34	10.3
011101	30	12.2
011010	26	9.7
010111	20	7.1
001101	15	6
001010	13	4.85
000111	10	3.58
000110	9.2	3.15
000101	8.1	2.69
000100	6.9	2.23
010001	5.4	1.56
000010	4	1.28
000000	2.5	0.778

Service and Support：

Address： No.2 Siyingmen N. Road. Donggaodi. Fengtai District.Beijing.China.
Department： Department of international cooperation
telephone：010-67968115-7178
Fax：010-68757706
Zip code：100076