Datasheet

600V High Voltage 3 Phase Bridge Driver

BS2130F-G

General Description

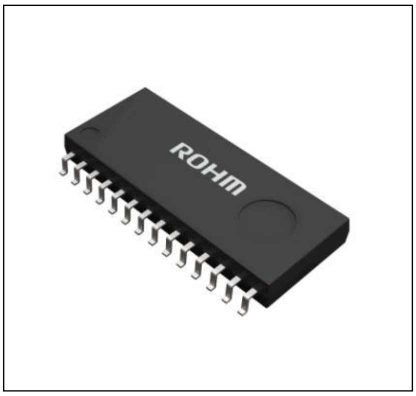
The BS2130F is a monolithic bridge driver IC, which can drive N-channel power MOSFET and IGBT driver in 3 phase systems with bootstrap operations.
The floating channel can be used to driven an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600V.
The logic inputs can be used 3.3V and 5.0V.
To provide a protection circuit, the device Includes an Under Voltage Lockout (UVLO) circuit and an Over Current Protection (OCP) circuit.
The UVLO circuit prevents malfunction when VCC and VBS are lower than the specified threshold voltage.

Key Specifications

■ High-side floating supply voltage:	600V
■ Output voltage range:	11.5 ~ 20V
■ Min Output Current Io+/Io-:	200mA/350mA(Typ)
■ OCP detect voltage	0.46V(Typ)
■ OCP blanking time	150ns(Typ)
■ Turn On/Turn Off:	630/580ns(Typ)
■ Offset supply leakage current:	50µA (Max)
■ Operating temperature range:	-40°C ~+125°C

Package

	W(Typ) x D(Typ) x H(Max)
SOP-28	18.50mm x 9.90mm x 2.41mm



Features

- ■ Floating Channels for Bootstrap Operation to +600V
- ■ Gate drive supply range from 11.5V to 20V
- ■ Built-in Under Voltage Lockout for Both Channels
- ■ The device includes an Over Current Protection circuit
- ■ Built-in Enable Channel (EN) which enable I/O functionality
- ■ Built-in FAULT Channel (/FAULT) which indicates over current and under voltage
- ■ RCIN Channel can determine the OCP holding time by external resistance and capacitance
- ■ 3.3V and 5.0V input logic compatible
- ■ Output in phase with input

Applications

- ■ MOSFET and IGBT high side driver applications

Typical Application Circuit

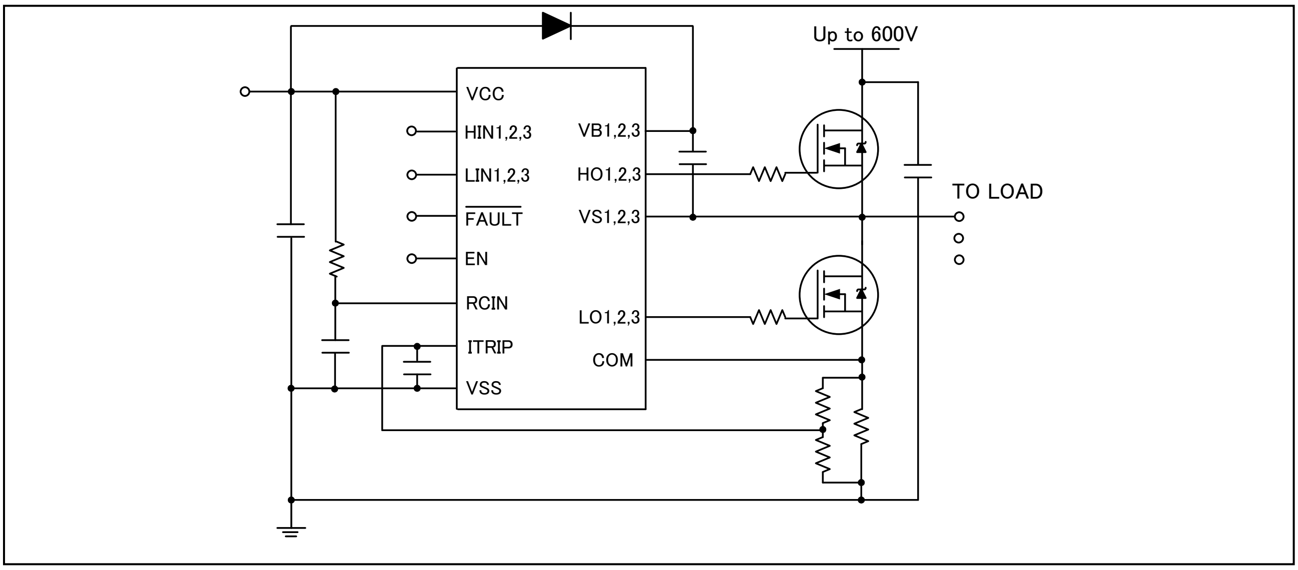


Figure 1. Typical Application Circuit

○Product structures : Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays

Pin Configuration

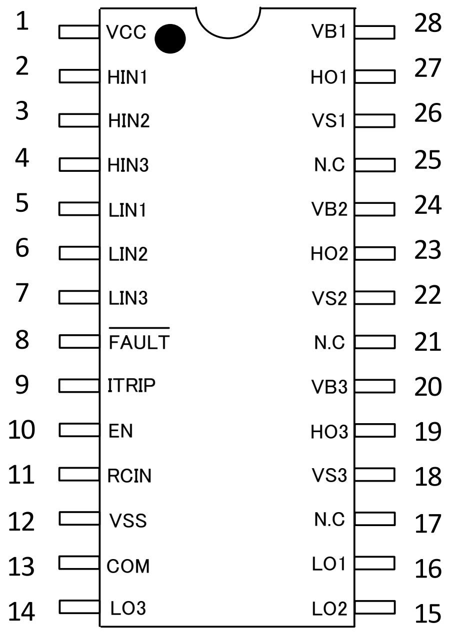


Figure 2. Pin Configuration

Pin Description

Pin No.	Symbol	Function
1	VCC	Low side supply voltage
2,3,4	HIN1,2,3	Logic input for high side gate driver outputs (HO1,2,3), in phase
5,6,7	LIN1,2,3	Logic input for low side gate driver outputs (LO1,2,3), in phase
8	/FAULT	Indicates over current or low side undervoltage (negative logic, open-drain output)
9	ITRIP	Analog input for over-current shutdown, activates FAULT and RCIN to VSS
10	EN	Logic input to enable I/O functionality (positive logic)
11	RCIN	External RC-network to define FAULT clear delay after the t_{HOLD}
12	VSS	Logic Ground
13	COM	Power Ground
14,15,16	LO1,2,3	Low side gate drive outputs
18,22,26	VS1,2,3,	High side floating supply return
19,23,27	HO1,2,3	High side gate drive outputs
20,24,28	VB1,2,3	High side floating supply
17,21,25	N.C	Non-Connection

Block Diagram

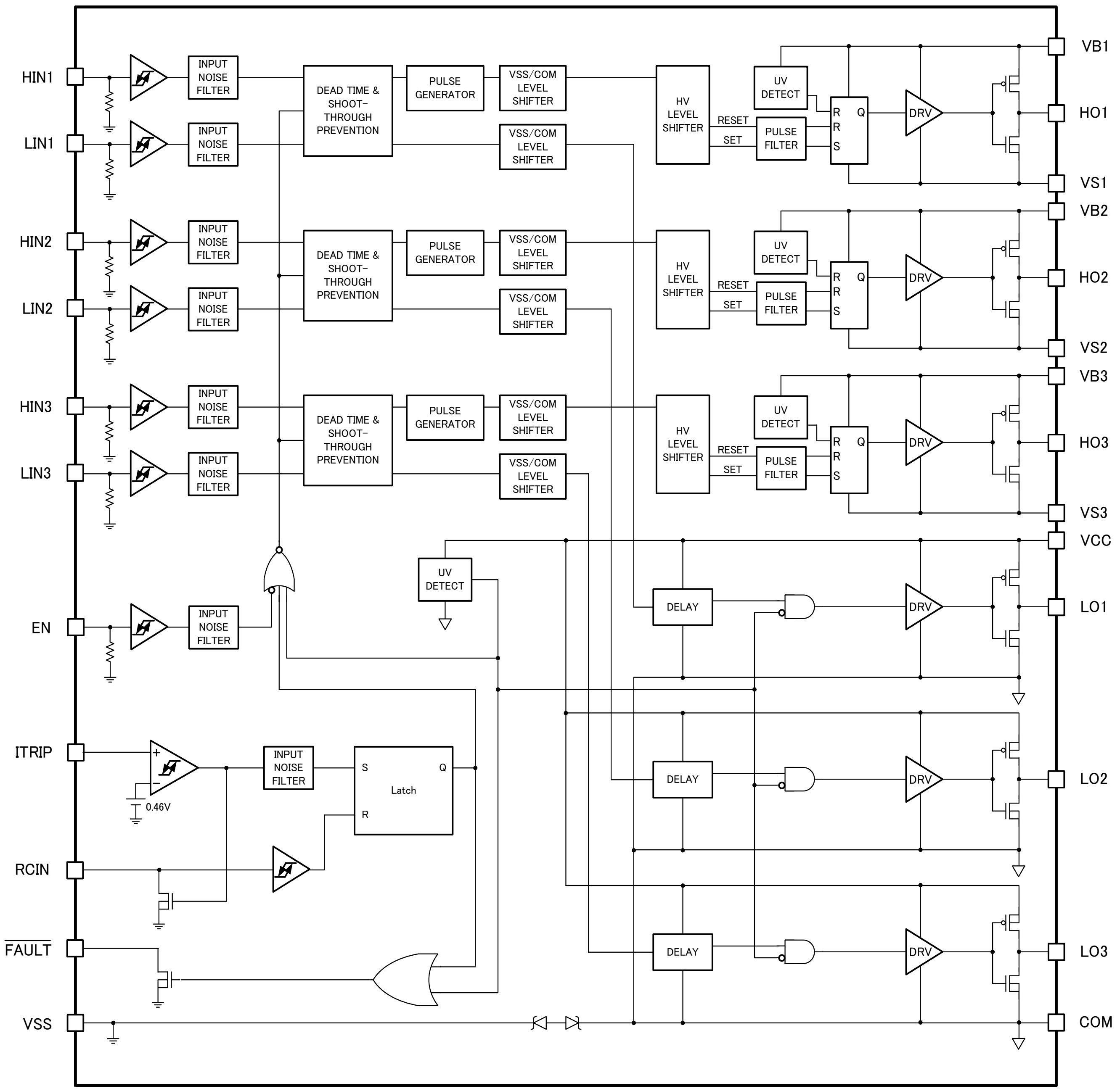


Figure 3. Functional Block Diagram

Absolute Maximum Ratings

(Unless otherwise specified: All voltages are absolute voltages referenced to VSS. VSS=0V, Ta=25˚C)

Parameter	Symbol	Min	Max	Unit
High side offset voltage	V_S	V_B-25	V_B+0.3	V
High side floating supply voltage	V_B	V_{COM}-0.3	V_{COM}+625	V
High side floating output voltage HO (HO vs. VS)	V_{HO}	-0.3	V_B+0.3	V
Low side and logic fixed supply voltage (VCC vs. VSS)	V_{CC}	-0.3	+25	V
Low side and logic fixed supply voltage (VCC vs. COM)	V_{CCCOM}	-0.3	+25	V
Low side output voltage LO (LO vs. COM)	V_{LO}	-0.3	V_{CCCOM}+0.3	V
Logic input voltage HIN, LIN, EN	V_{IN}	-0.3	V_{CC}+0.3	V
FAULT output voltage	V_{FLT}	-0.3	V_{CC}+0.3	V
RCIN input voltage	V_{RCIN}	-0.3	V_{CC}+0.3	V
ITRIP input voltage	V_{ITRIP}	-0.3	V_{CC}+0.3	V
Power ground	V_{COM}	-5.5	+5.5	V
Allowable offset voltage SLEW RATE	dV_S/dt	-	50	V/ns
Junction temperature	Tjmax	-	150	°C
Storage temperature	Tstg	-55	+150	°C

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
SOP28				
Junction to Ambient	θ_{JA}	136.9	88.6	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	19	15	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air)

*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

*(Note 3)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70μm

*(Note 4)*Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2mm x 74.2mm	35μm	74.2mm x 74.2mm	70μm

Recommended Operating Ratings

(Unless otherwise specified: All voltages are absolute voltages referenced to VSS. VSS=0V)

Parameter	Symbol	Min	Max	Unit
High side floating supply offset voltage (VS vs. COM)	V_S	-	600	V
High side floating supply voltage (VB vs. VS)	V_B	11.5	20	V
High side floating output voltage (HO vs. VS)	V_{HO}	0	V_B	V
Low side supply voltage (VCC vs. VSS)	V_{CC}	11.5	20	V
Low side supply voltage (VCC vs. COM)	V_{CCCOM}	11.5	20	V
Low side output voltage LO (LO vs. COM)	V_{LO}	0	V_{CCCOM}	V
Logic input voltage HIN, LIN, EN	V_{IN}	0	V_{CC}	V
FAULT output voltage	V_{FLT}	0	V_{CC}	V
RCIN input voltage	V_{RCIN}	0	V_{CC}	V
ITRIP input voltage	V_{ITRIP}	0	V_{CC}	V
Power ground	V_{COM}	-2.5	+2.5	V
Ambient temperature	T_A	-40	+125	°C

Static Logic Function Table

VCC	VBS	RCIN	ITRIP	EN	FAULT	HO1,2,3	LO1,2,3
<VCCUV-	X	X	X	X	0	0	0
15V	<VBSUV-	X	0V	5V	High-Z	0	LIN1,2,3
15V	15V	X	>$V_{IT,TH+}$	5V	0	0	0
15V	15V	<V_{RCIN+}	0V	5V	0 *(Note 1)*	0 *(Note 1)*	0 *(Note 1)*
15V	15V	>V_{RCIN+}	0V	5V	High-Z	HIN1,2,3	LIN1,2,3
15V	15V	>V_{RCIN+}	0V	0V	High-Z	0	0

(Note 1) State after the OCP. Because the latch circuit is not reset, the OCP state is maintained.

DC Operation Electrical Characteristics

(Unless otherwise specified: Ta=25°C, V_{CC}=15V, V_{BS}=15V, V_S=V_{SS}=V_{COM}, C_L=1000pF)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
V_{CC} and V_{BS} supply undervoltage positive going threshold	V_{CCUV+} V_{BSUV+}	9.6	10.4	11.2	V	
V_{CC} and V_{BS} supply undervoltage negative going threshold	V_{CCUV-} V_{BSUV-}	8.6	9.4	10.2	V	
V_{CC} supply undervoltage lockout hysteresis	V_{CCUVH} V_{BSUVH}	-	1.0	-	V	
Offset supply leakage current	I_{LK}	-	-	50	µA	V_B = V_S = 600V
Quiescent V_{BS} supply current	I_{QBS}	-	60	120	µA	V_{IN} = 0V or 5V
Quiescent V_{CC} supply current	I_{QCC}	-	0.7	1.3	mA	V_{IN} = 0V or 5V
Logic "1" input voltage	V_{IH}	2.6	-	-	V	
Logic "0" input voltage	V_{IL}	-	-	0.8	V	
EN positive going threshold	V_{EN+}	-	-	2.6	V	
EN negative going threshold	V_{EN-}	0.8	-	-	V	
RCIN positive going threshold	V_{RCIN+}	-	8	-	V	
RCIN hysteresis	$V_{RCIN,HYS}$	-	3	-	V	
ITRIP positive going threshold	$V_{IT,TH+}$	0.437	0.46	0.483	V	
ITRIP hysteresis	$V_{IT,HYS}$	-	0.07	-	V	
High level output voltage, V_{CC} (V_{BS}) - V_O	V_{OH}	-	-	1.4	V	I_O = 20mA
Low level output voltage, V_O	V_{OL}	-	-	0.6	V	I_O = 20mA
Logic "1" input bias current	I_{IN+}	-	100	150	µA	V_{IN} = 3.3V
Logic "0" input bias current	I_{IN-}	-	-	1.0	µA	V_{IN} = 0V
ITRIP input bias current	I_{ITRIP}	-	1	2	µA	V_{ITRIP} = 0V or 3.3V
Output high short circuit pulse current	I_{O+}	120	200	-	mA	V_O = 0V Pulse Width ≦10µs
Output low short circuit pulsed current	I_{O-}	250	350	-	mA	V_O = 15V Pulse Width ≦10µs
RCIN input bias current	I_{RCIN}	-	-	1	µA	
RCIN low on resistance	R_{ON_RCIN}	-	50	100	Ω	V_{RCIN} = 0.5V
FAULT low on resistance	R_{ON_FAULT}	-	50	100	Ω	V_{FAULT} = 0.5V

AC Operation Electrical Characteristics
(Unless otherwise specified: Ta=25°C, V_{CC}=15V, V_{BS}=15V, V_S=V_{SS}=V_{COM}, C_L=1000pF)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Turn-on propagation delay	t_{on}	480	630	780	ns	V_S = 0V, V_{IN} = 0V & 5V
Turn-off propagation delay	t_{off}	430	580	730	ns	V_S = 0V or 600V, V_{IN} =0V&5V
Turn-on rise time	t_r	-	125	190	ns	V_{IN} = 0V & 5V
Turn-off fall time	t_f	-	50	75	ns	V_{IN} = 0V & 5V
EN low to output shutdown propagation delay	t_{EN}	430	580	730	ns	V_{IN} ,V_{IN} = 0V & 5V
ITRIP to output shutdown propagation delay	t_{ITRIP}	500	750	1000	ns	V_{ITRIP} = 5V
ITRIP blanking time	t_{bl}	100	150	-	ns	V_{ITRIP} = 5V
ITRIP to FAULT propagation delay	t_{FLT}	400	600	800	ns	V_{ITRIP} = 5V
Input filter time (HIN,LIN)	t_{FILIN}	100	200	-	ns	V_{IN} = 0V & 5V
Enable input filter time	t_{FLTEN}	100	200	-	ns	V_{IN} = 0V & 5V
Dead time	DT	250	300	450	ns	V_{IN} = 0V & 5V
Delay matching, HS & LS turn-on/off	MT	-	-	150	ns	
FAULT clear time	t_{FLTCLR}	1.3	1.65	2.0	ms	RCIN : R = 2MΩ, C = 1nF

Typical Performance Curves
(Unless otherwise specified: Ta=25°C, V_{CC}=15V, V_{BS}=15V, V_S=V_{PGND}=V_{GND}, C_L=1000pF)

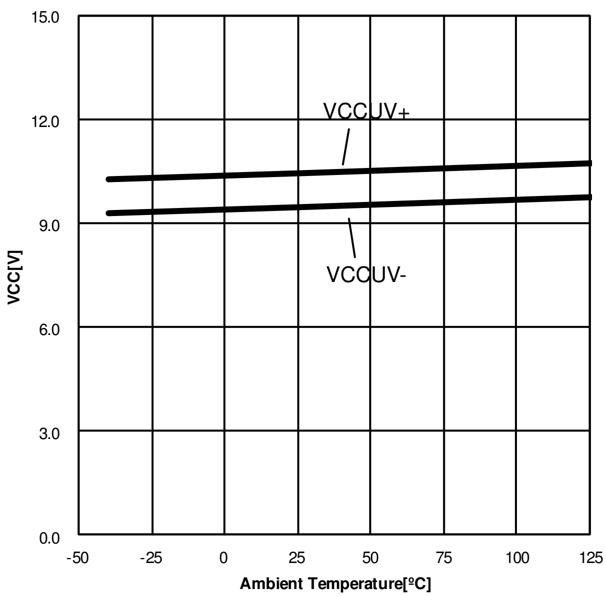


Figure 4. V_{CC} UVLO - Ta

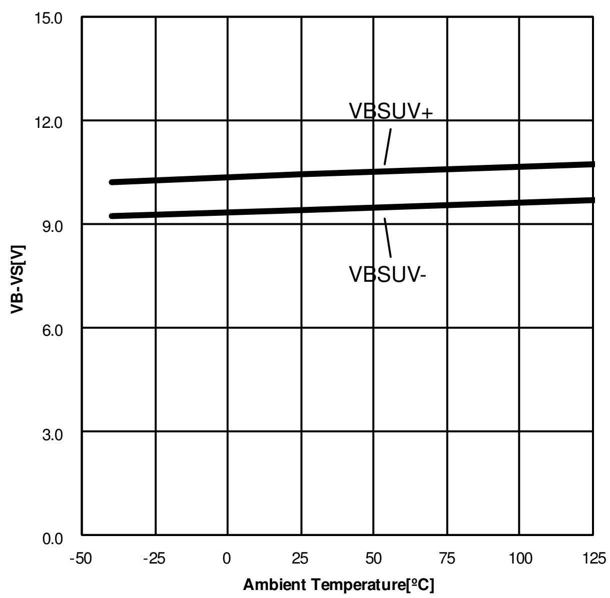


Figure 5. V_{BS} UVLO - Ta

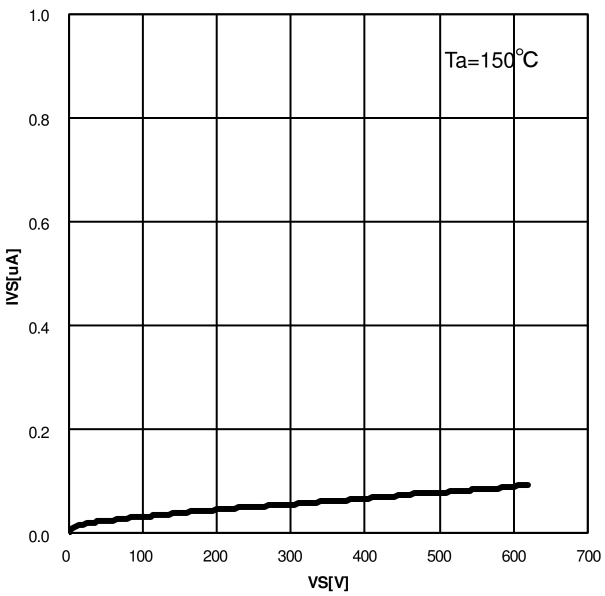


Figure 6. Offset supply leakage current - V_S
(V_B=V_S)

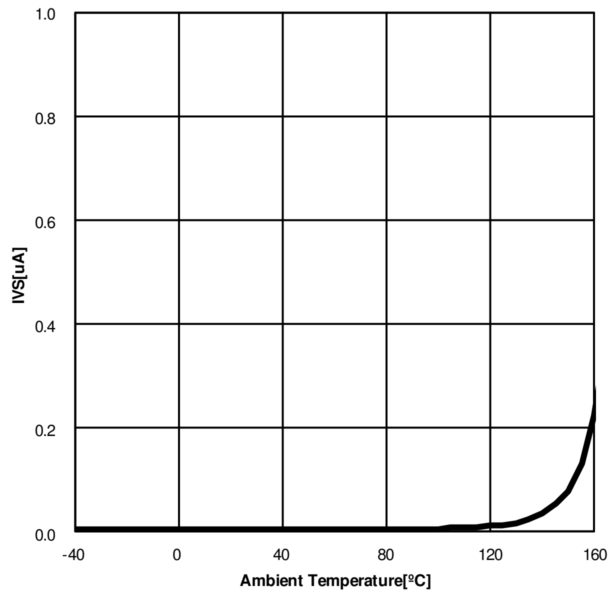


Figure 7. Offset supply leakage current – Ta
(V_B=V_S=600V)

Typical Performance Curves

(Unless otherwise specified: Ta=25°C, V_{CC}=15V, V_{BS}=15V, V_S=V_{PGND}=V_{GND}, C_L=1000pF)

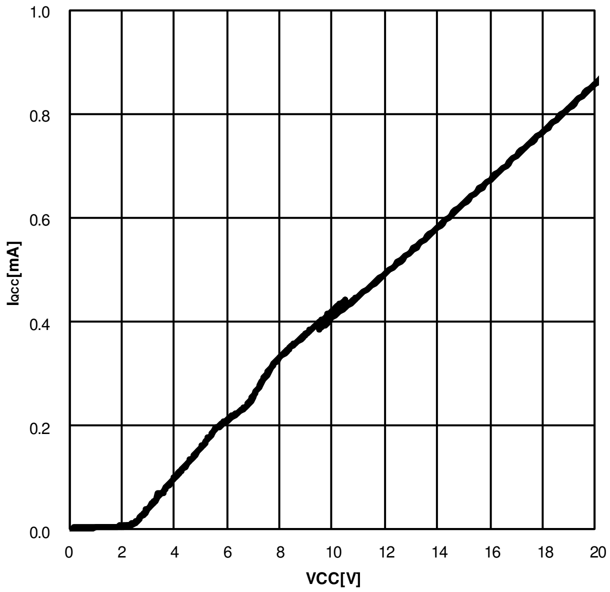


Figure 8. Quiescent V_{CC} supply current - V_{CC}

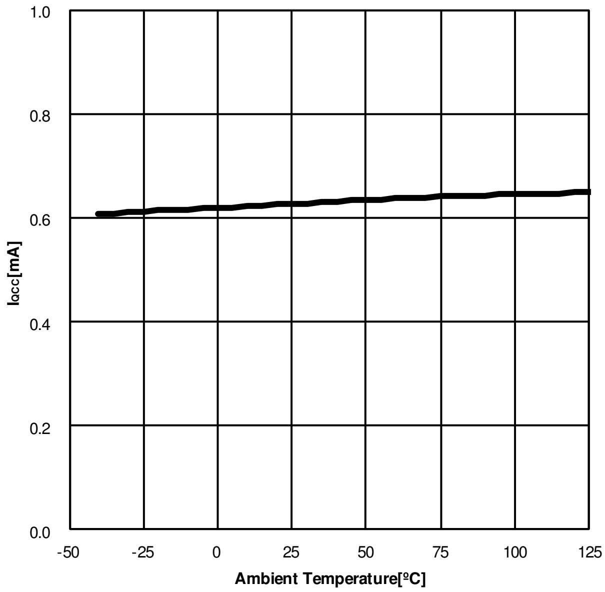


Figure 9. Quiescent V_{CC} supply current – Ta (V_{CC}=15V)

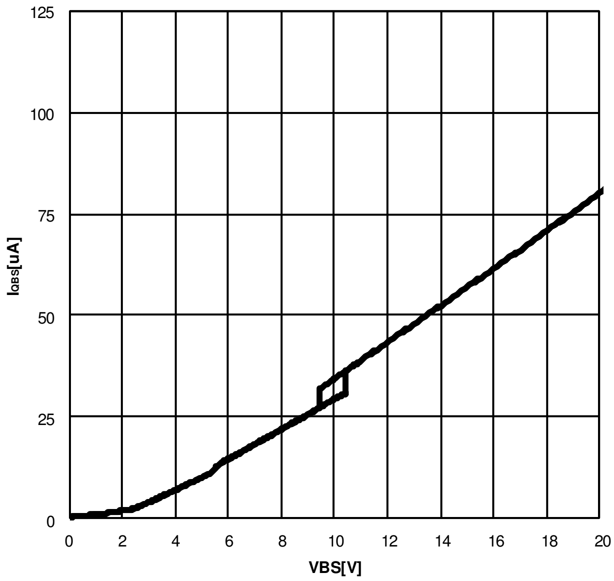


Figure 10. Quiescent V_{BS} supply current - V_{BS}

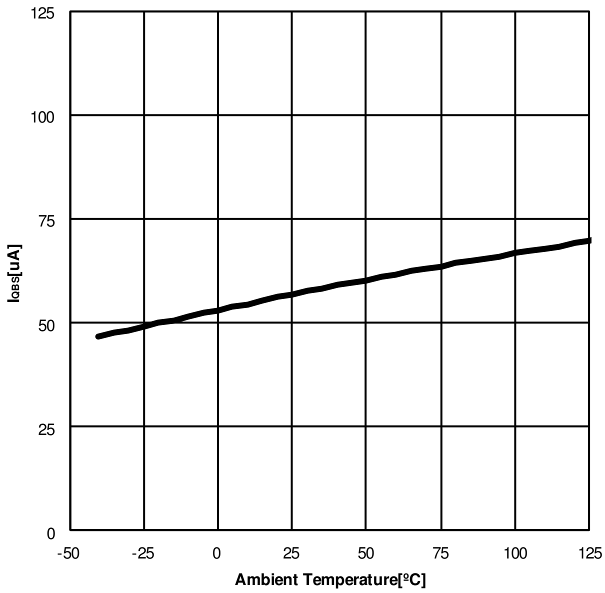


Figure 11. Quiescent V_{BS} supply current – Ta (V_{BS}=15V)

Typical Performance Curves

(Unless otherwise specified: Ta=25°C, V_{CC}=15V, V_{BS}=15V, V_S=V_{PGND}=V_{GND}, C_L=1000pF)

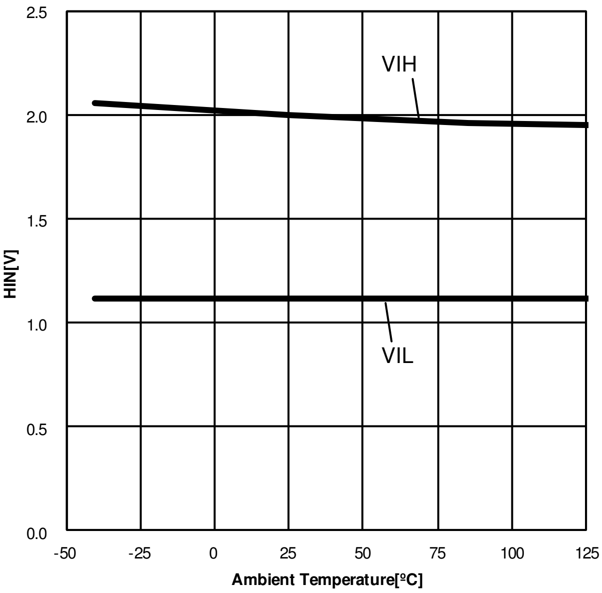


Figure 12. Logic "1"/"0" Input Voltage HIN - Ta

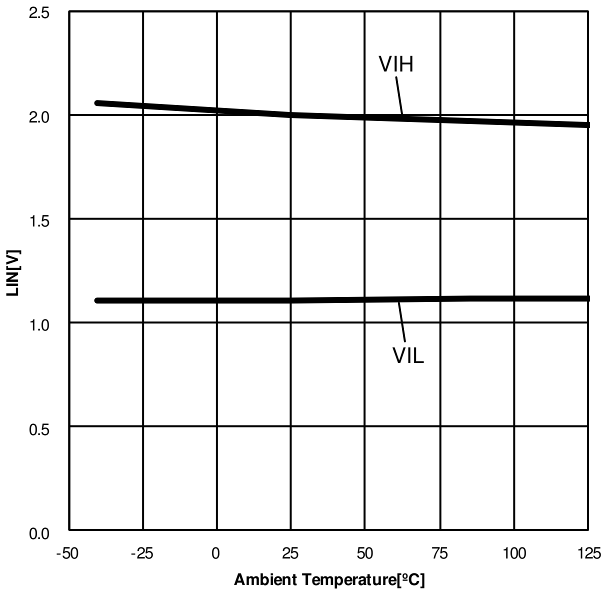


Figure 13. Logic "1"/"0" Input Voltage LIN - Ta

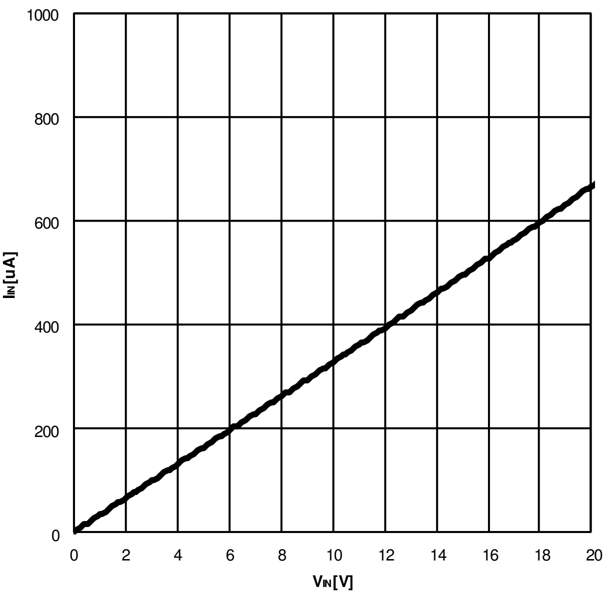


Figure 14. Logic "1" Input bias current - VIN

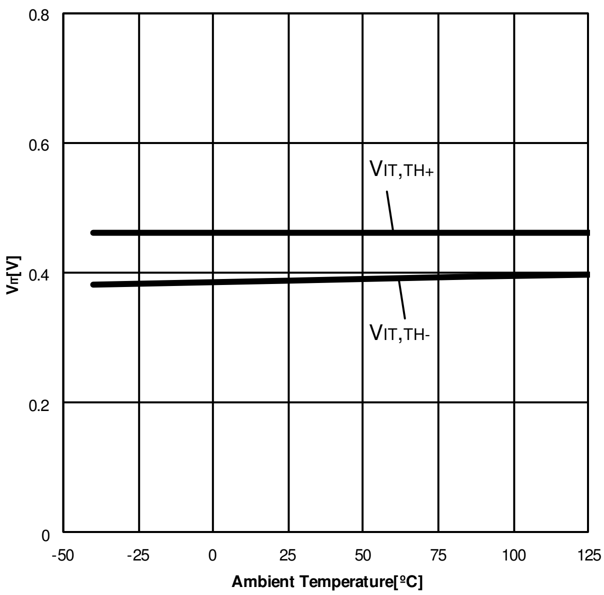


Figure 15. ITRIP threshold Voltage - Ta

Typical Performance Curves

(Unless otherwise specified: Ta=25°C, V_{CC}=15V, V_{BS}=15V, V_S=V_{PGND}=V_{GND}, C_L=1000pF)

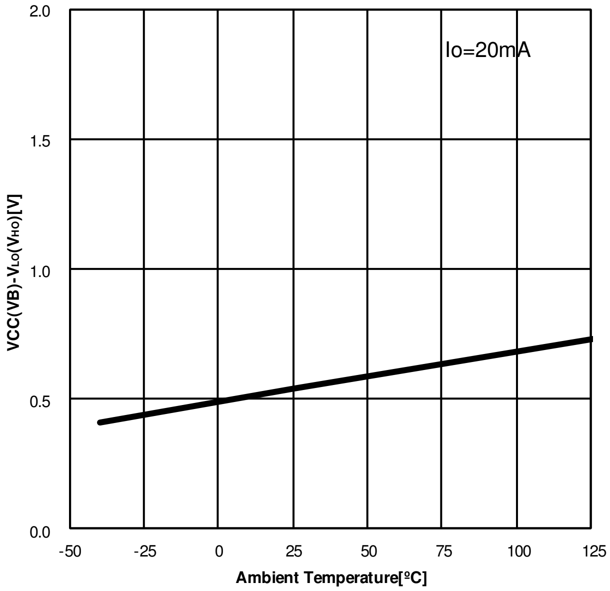


Figure 16. High Level Output Voltage - Ta

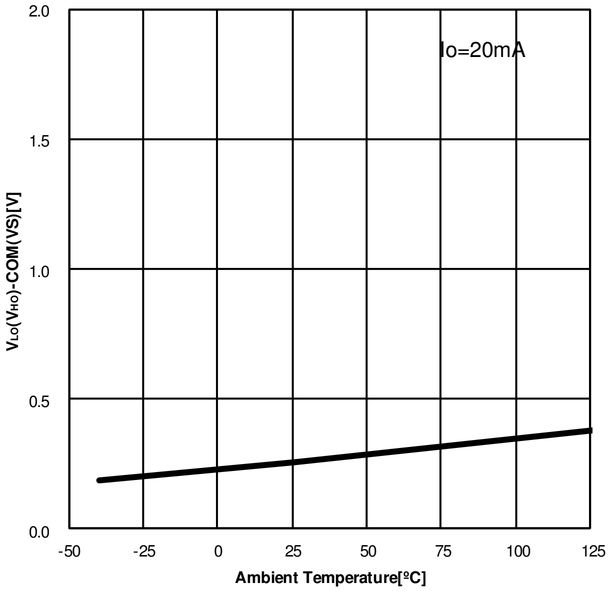


Figure 17. Low Level Output Voltage - Ta

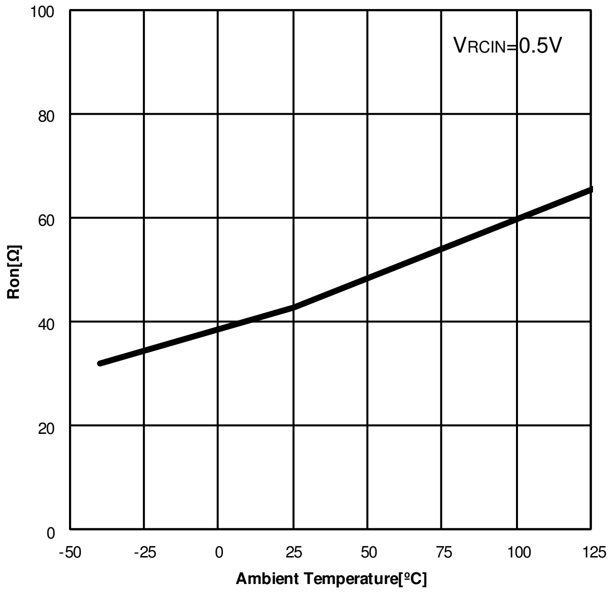


Figure 18. RCIN low on Resistance - Ta

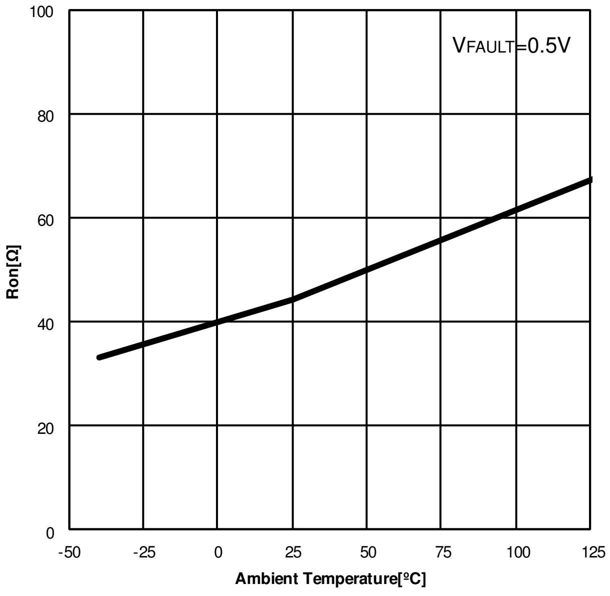


Figure 19. FAULT low on Resistance - Ta

Typical Performance Curves

(Unless otherwise specified: Ta=25°C, V_{CC}=15V, V_{BS}=15V, V_S=V_{PGND}=V_{GND}, C_L=1000pF)

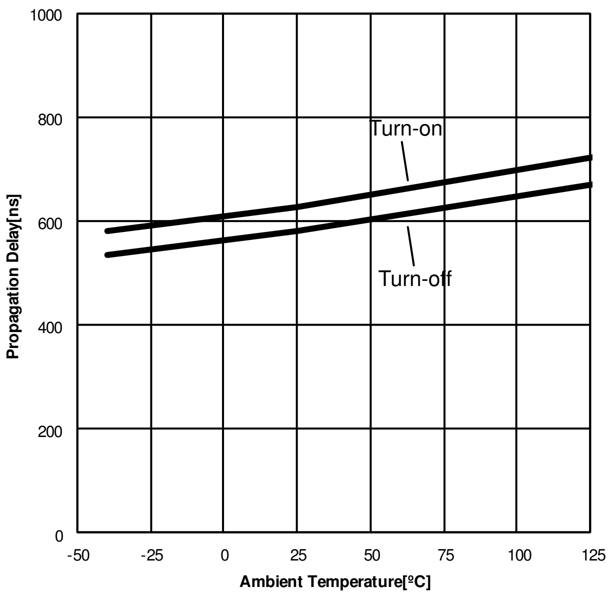


Figure 20. HO Turn on/off Propagation Delay - Ta

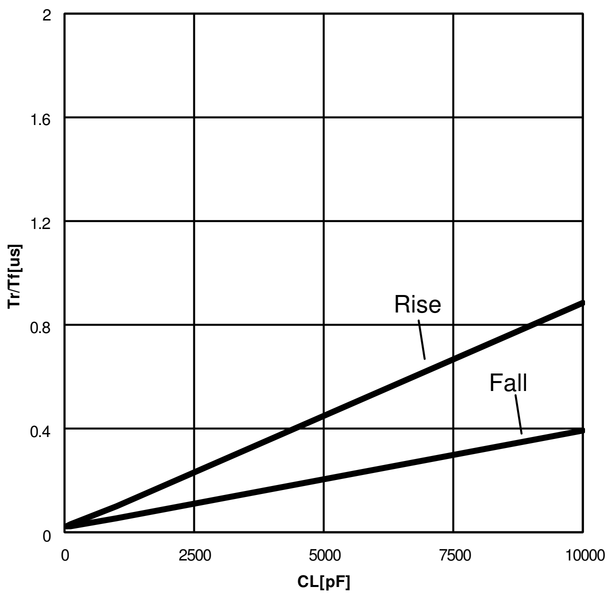


Figure 21. HO Rise/Fall Time – Load Capacitance

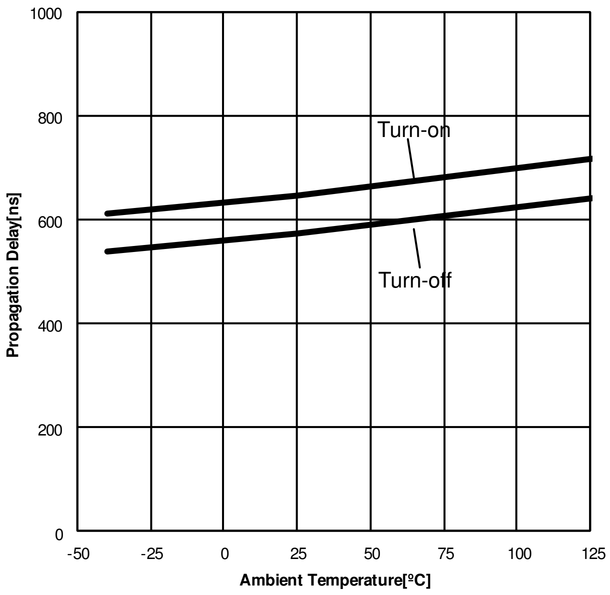


Figure 22. LO Turn on/off Propagation Delay - Ta

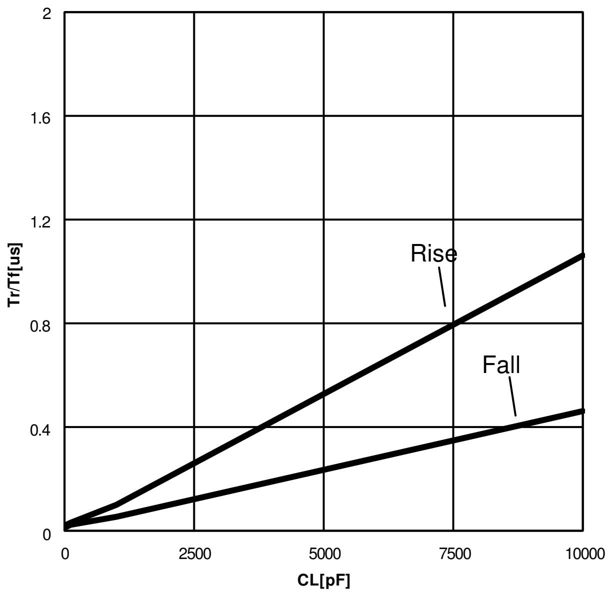


Figure 23. LO Rise/Fall Time – Load Capacitance

Typical Performance Curves
(Unless otherwise specified: Ta=25°C, V_{CC}=15V, V_{BS}=15V, V_S=V_{PGND}=V_{GND}, C_L=1000pF)

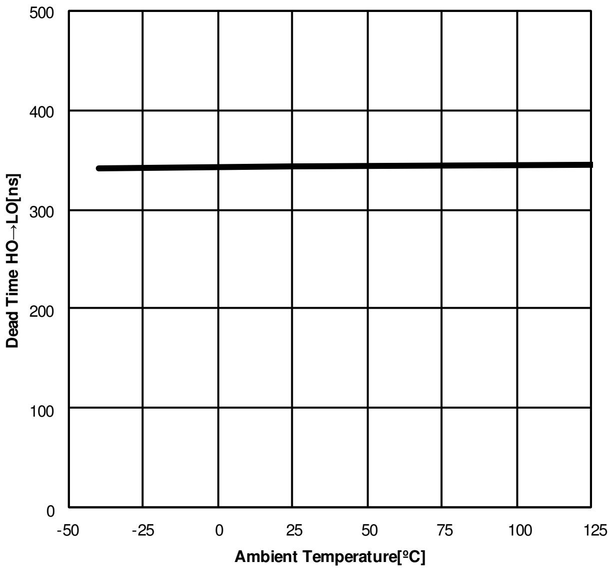


Figure 24. Dead time – Ta (HO off – LO on)

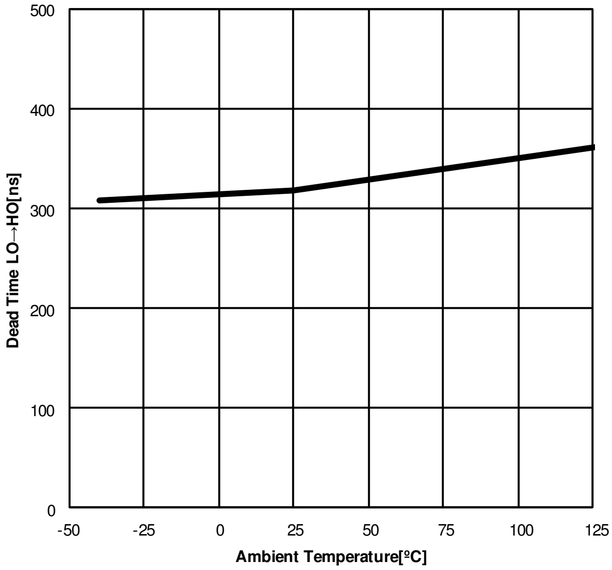


Figure 25. Dead time – Ta (LO off – HO on)

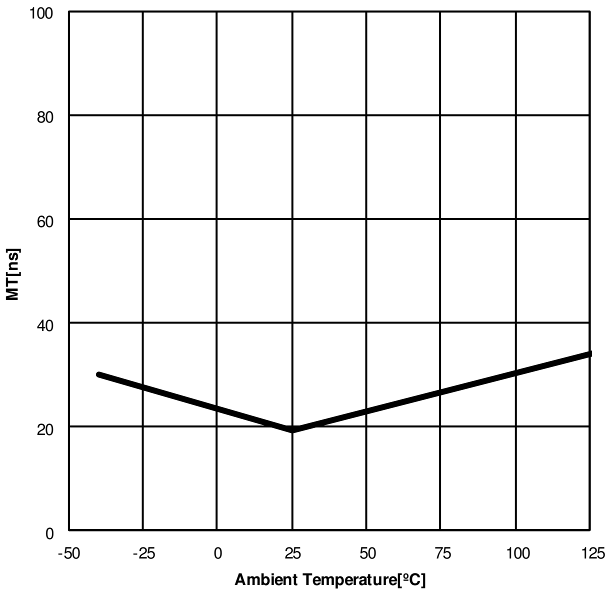


Figure 26. Delay matching Turn on/off - Ta

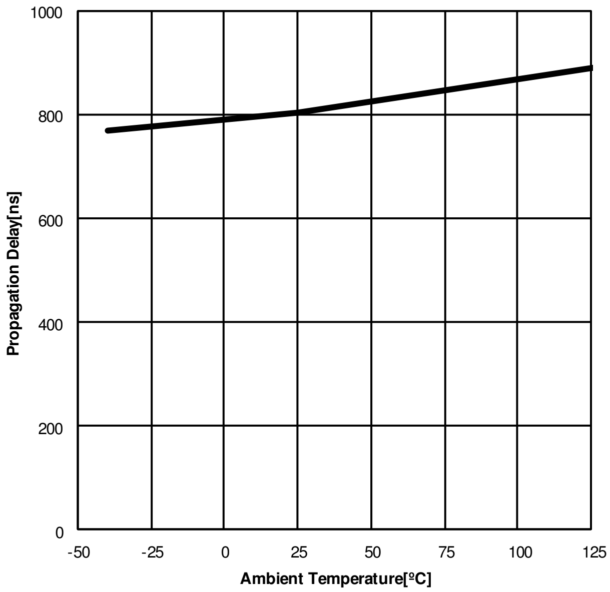


Figure 27. ITRIP to Output Shutdown Propagation Delay - Ta

Typical Performance Curves

(Unless otherwise specified: Ta=25°C, V_{CC}=15V, V_{BS}=15V, V_S=V_{PGND}=V_{GND}, C_L=1000pF)

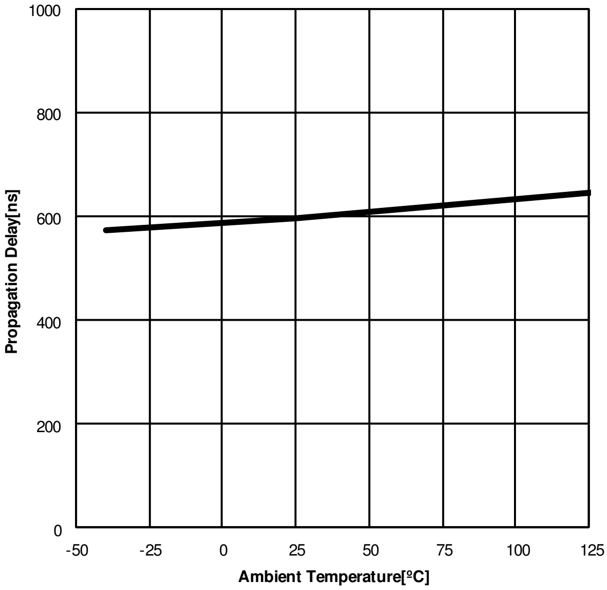


Figure 28. ITRIP to FAULT Propagation Delay - Ta

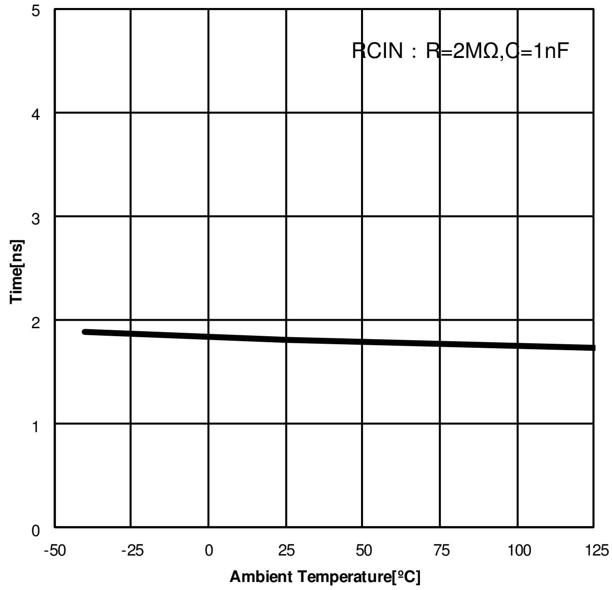
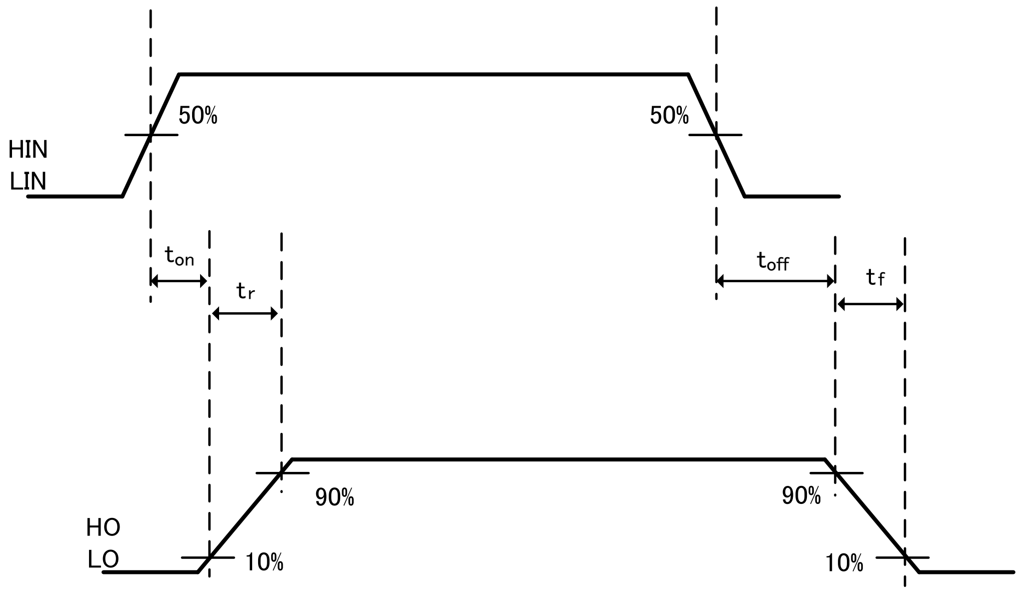
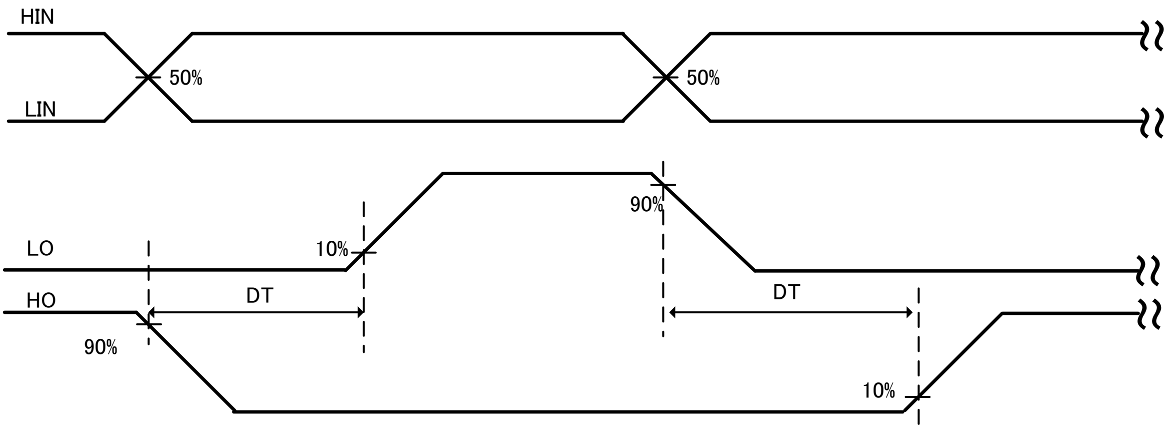


Figure 29. FAULT clear time - Ta

Timing Chart



(a) Propagation Delay



(b) Dead time

Figure 30. Timing Chart

Timing Chart

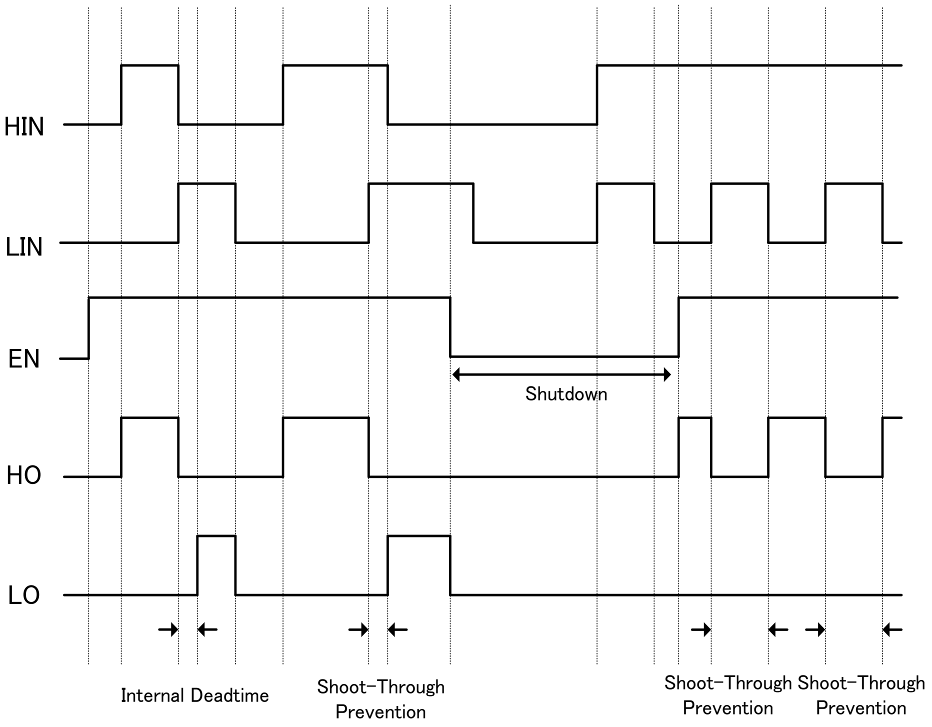


Figure 31. Timing Chart

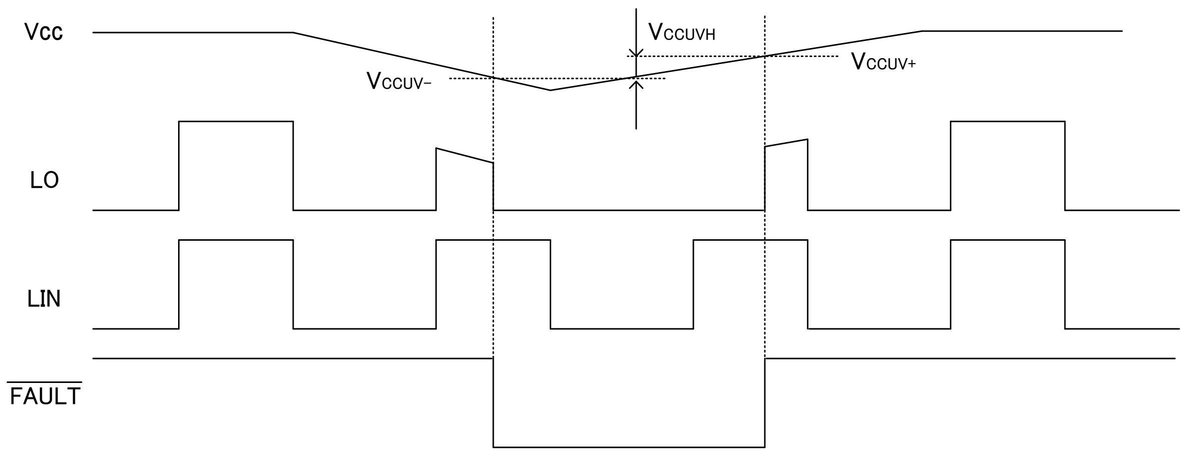


Figure 32. VCCUVLO Timing Chart

Over Current Protection

As soon as ITRIP voltage is exceeded the threshold voltage 0.46V (typ), impedance of the /FAULT pin is lowered and the RCIN pin turns off.
ITRIP blanking time 150ns (typ) prevents the driver to detect false over-current events which caused by noise. However, it is recommended to add a ceramic capacitor near the ITRIP pin.
FAULT clear time is determined by external resistance and capacitance. As soon as RCIN voltage exceeds the rising threshold voltage 8V (typ), the FAULT condition releases. Also, RCIN voltage operates in the voltage less than V_{RCIN+}. However, it is not returned with stopping when ITRIP voltage goes over threshold voltage $V_{IT,TH+}$ once. RCIN voltage to recommend at the normal operation is more than V_{RCIN+}.

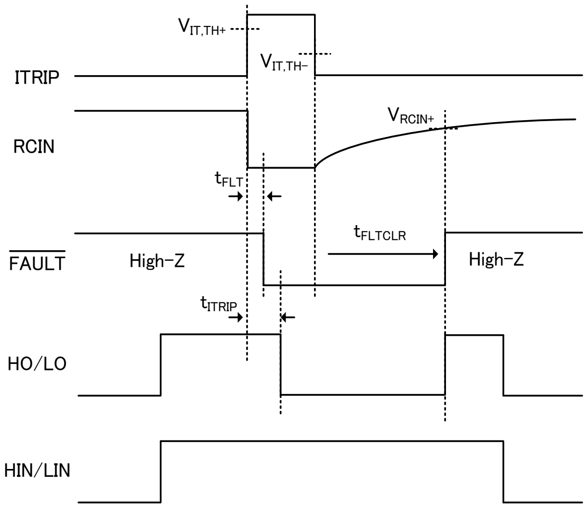


Figure 33. OCP Detection Timing Chart

The over current detection value is determined by R1, R2, and RS, which are connected to ITRIP pin as Figure 34.
The over current detection value is determined by the following equation.

$$Iocp = \frac{R_1+R_2}{R_2} \times \frac{V_{IT,TH+}}{R_S}$$

Iocp : over current detection value
$V_{IT,TH+}$: OCP threshold voltage 0.46V(typ)
Rs : Shunt resistor

The reset time of FAULT is determined by the following equation.

$$t_{FLTCLR} = -(R_{RCIN} \times C_{RCIN}) \times \ln(1- \frac{V_{RCIN,TH+}}{V_{CC}})$$

V_{RCIN+} : RCIN threshold voltage 8V(typ)

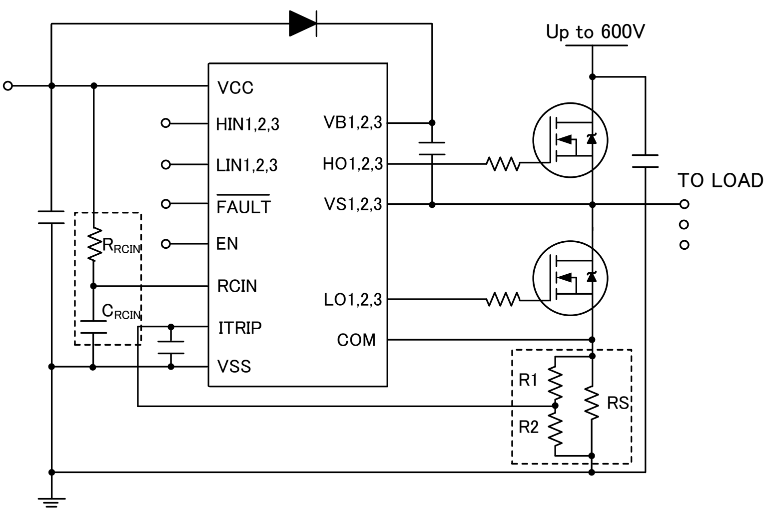


Figure 34. OCP Detection Schematic

Application Components Selection Method

(1) Gate Resistor

The gate resistor $R_{G(on/off)}$ is selected to control the switching speed of the output transistor. The switching time (t_{SW}) is defined as the time spent to reach the end of the plateau voltage, so the turn on gate resistor $R_{G(on)}$ can be calculated using the following formulas.

$$I_g = \frac{Q_{gs}+Q_{gd}}{t_{SW}} \quad (1)$$

$$R_{TOTAL(on)} = R_{pon} + R_{G(on)} = \frac{V_{BS}-V_{gs(th)}}{I_g} \quad (2)$$

$$t_{sw} = \frac{Q_{gs}+Q_{gd}}{I_g} = \frac{(Q_{gs}+Q_{gd})(R_{pon}+R_{G(on)})}{(V_{BS}-V_{gs(th)})} \quad (3)$$

Turn on gate resistor value can be changed to control output slope (dVs/dt). While the output voltage is non-linear, the maximum output slope should have a value near that of the following formula:

$$\frac{\mathrm{dVs}}{\mathrm{dt}} = \frac{I_g}{C_{rss}} \quad (4)$$

where:
C_{rss} is the feedback capacitance.

Substituting the value of I_g from equation (2) into equation (4) yields the following formulas.

$$R_{TOTAL(on)} = R_{pon} + R_{G(on)} = \frac{V_{BS}-V_{gs(th)}}{C_{rss}\cdot\frac{dVs}{dt}} \quad (5)$$

$$R_{G(on)} = \frac{V_{BS}-V_{gs(th)}}{C_{rss}\cdot\frac{dVs}{dt}} - R_{pon} \quad (6)$$

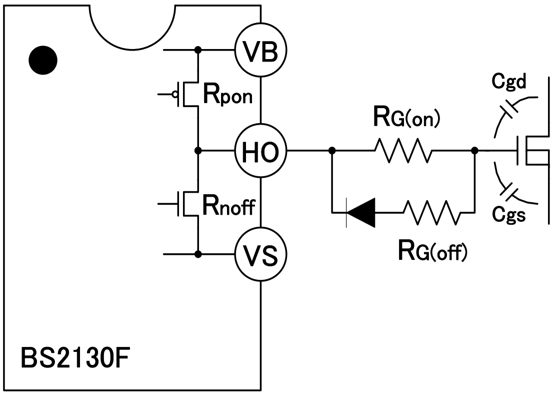


Figure 35. Gate Driver Equivalent Circuit

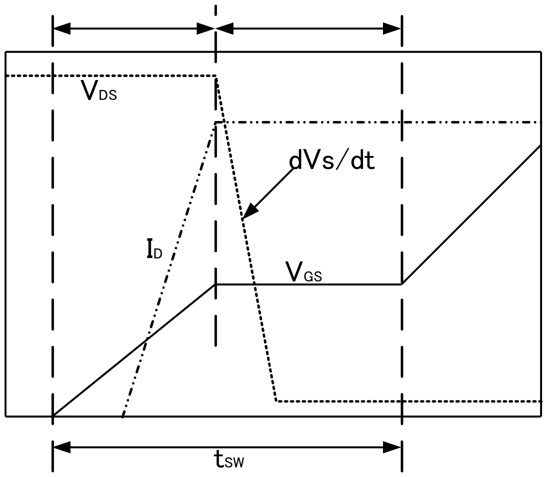


Figure 36. Gate Charge Transfer Characteristics

When the gate driver output is in off state, other dVs/dt may induce a drop in the gate voltage of the MOSFET, causing self-turn-on. To prevent this, please set up the turn off resistor ($R_{G(off)}$) that satisfies the following formulas.

$$V_{gs(th)} \geq (R_{noff}+R_{G(off)})\cdot I_g = (R_{noff}+R_{G(off)})\cdot C_{gd}\frac{dVs}{dt} \quad (7)$$

$$R_{G(off)} \leq \frac{V_{gs(th)}}{C_{gd}\frac{dVs}{dt}} - R_{noff} \quad (8)$$

(2) Bootstrap Capacitor C_{BS}
To reduce ripple voltage, ceramic capacitors with low ESR value are recommended for use in the bootstrap circuit.
The maximum voltage drop (ΔV_{BS}) that we have to guarantee when the high-side switch is in on state must be:

$$\Delta V_{BS} \leq VCC - VF - V_{GSMIN} \quad (9)$$

where:
VCC is the gate driver supply voltage,
VF is the bootstrap diode forward voltage drop, and
V_{GSMIN} is the minimum gate-source voltage.

The total charge supplied (Q_{Total}) by the bootstrap capacitor should have a value near the following formulas.

$$Q_{Total} = Q_G + (I_{LKGS} + I_{LK} + I_{LKDIO} + I_{QBS}) \cdot T_{HON} \quad (10)$$

where:
Q_G is the total gate charge,
I_{LKGS} is the switch gate-source leakage current,
I_{LKDIO} is the bootstrap diode leakage current,
I_{LK} is the level shifter circuit leakage current,
I_{QBS} is the quiescent current, and
T_{HON} is the high-side switch on time.

The bootstrap capacitor value should satisfy the following formula.

$$C_{BS} \geq \frac{Q_{Total}}{\Delta V_{BS}} \quad (11)$$

However, BS2130F has a BSTUVLO function to prevent malfunction at low voltage between VB and VS.
Please ensure sufficient capacitor margin to prevent BSTUVLO malfunction.
It is not able to keep turning-on the same way as the high side switch driver because of the specifications of the bootstrap circuits.
In addition, it is recommended to insert a 1 µF ceramic capacitor between VB and VS. This capacitor should be placed as close as possible to these pins for noise reduction.

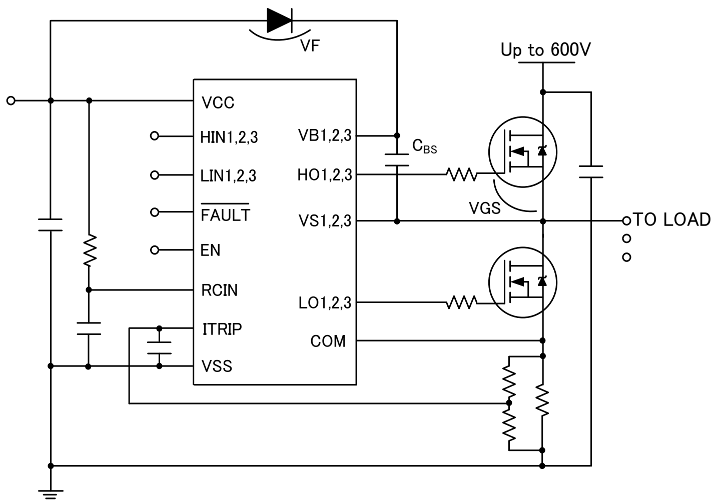


Figure 37. Bootstrap Power Supply Circuit

(3) Input Capacitor
Mount a low-ESR ceramic input capacitor near the VCC pin to reduce input ripple.
For BS2130F, it is recommended to use a capacitor value two times larger than that of the bootstrap capacitor or more.

(4) Input Signals Differential Δt_{IN}

The minimum differential of input signals ($\Delta t_{IN(min)}$) to prevent shoot-through of the MOSFETs can be calculated using the following formula.

$$t_{dead} \approx (t_{on} + \Delta t_{IN}) - (t_{off} + t_f) \quad (12)$$

$$t_f = -\tau \times (\ln 0.1 - \ln 0.9) \quad (13)$$

$$\tau = (R_{non} + R_G) \times C_L \quad (14)$$

t_{on} : Turn-on propagation delay
t_{off} : Turn-off propagation delay
t_f : Turn-off fall time
R_{non} : On-resistance of Nch MOSFET constituting the final stage inverter
R_G : Gate resistor
C_L : Load capacitor

Please set up Δt_{IN} that satisfies the following formulas.

$$t_{dead} > 0 \quad (15)$$

$$(t_{on} + \Delta t_{IN}) - (t_{off} + t_f) > 0 \quad (16)$$

$$\Delta t_{IN} > (t_{off} - t_{ON}) + t_f \quad (17)$$

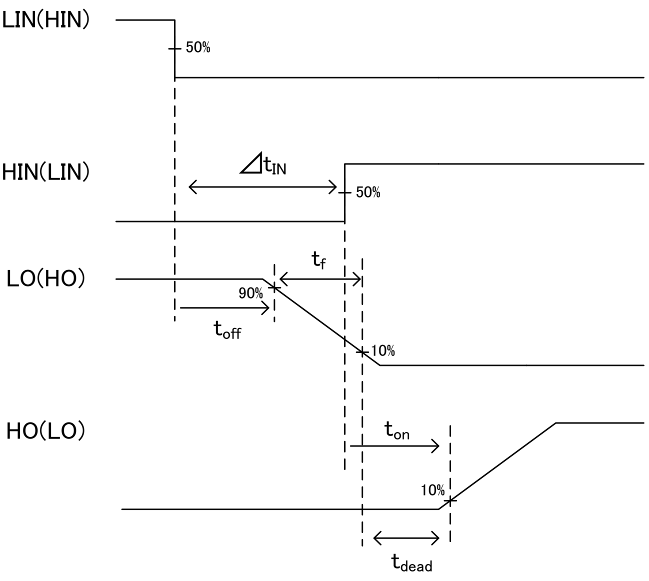


Figure 38. Shoot-Through Prevention Timing Chart

$$\Delta t_{IN(\min)} > (t_{off(\max)} - t_{on(\min)}) - (R_{non(\max)} + R_G) \times C_L \times (\ln 0.1 - \ln 0.9) \quad (18)$$

Overshoot / Undershoot of Output Terminal

The occurrence of overshoot / undershoot may be detected by the parasitic inductance of the bonding wire and the PCB. The mechanism of overshoot in the switching off is Figure 40.
(1) After PchFET is turn-off, current flows from HO to VB through capacitance between G-D and G-S.
(2) The current flows from HO to VB through parasitic diode of PchFET. Forward voltage Vf of the parasitic diode is increased, and HO voltage becomes VB+Vf. NchFET is turn-on and it is discharged to VS.
The undershoot of the switching on may be caused by the same mechanism, too.
In addition, it may be caused in low side output LO because the circuit structure is the same. The overshoot / undershoot voltage changes by the current of the parasitic diode.
When the overshoot / undershoot voltage is large, please adjust the gate resistance to slow in order to the switching speed and connect to reduce the parasitic inductance.

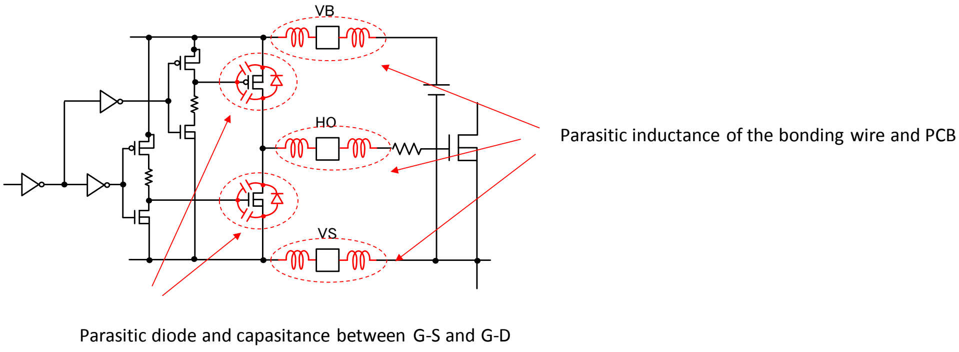


Figure 39. Schematic with Parasitic Inductance

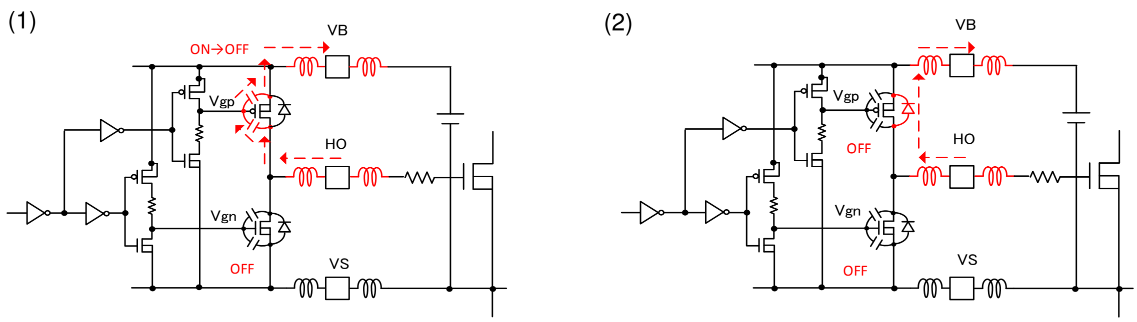


Figure 40. Mechanism of Overshoot

Figure 41. Overshoot Wave

Power Dissipation

It is shown below reducing characteristics of power dissipation to mount 114.3mm × 76.2mm.
Junction temperature must be designed not to exceed 150°C.

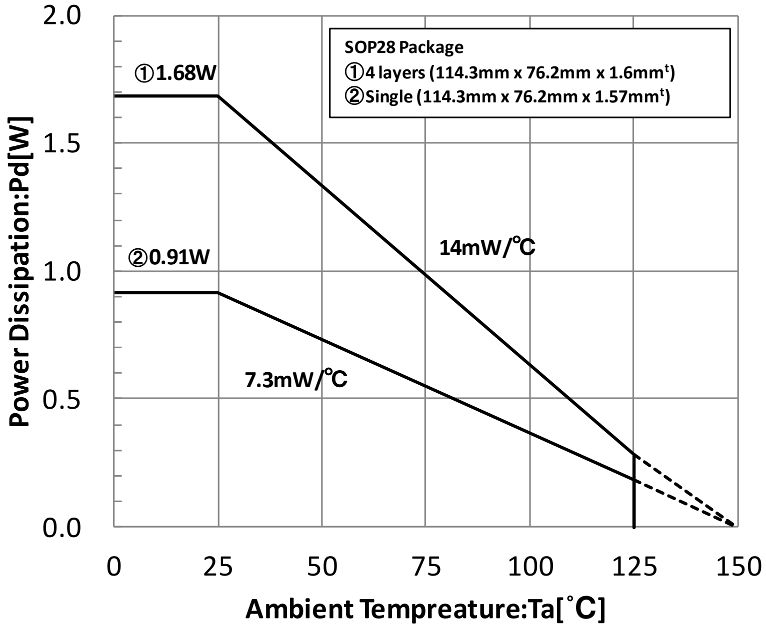


Figure 42. Power Dissipation

PCB Layout

1. Power GND and Logic GND
   Surge voltage is caused by current of Power GND and parasitic inductance of the wire. It may cause malfunction by GND fluctuation. It is recommended to connect Power GND and Logic GND at only a point.

2. Shunt Resistor
   It is recommended to locate a shunt resistor near the external power MOSFET of low side. If the wiring is long, surge voltage is caused by parasitic inductance. The wiring to the ITRIP should be divided near the shunt resistor.

3. ITRIP Filter Capacitor
   To prevent a malfunction, it is recommended to locate a ceramic capacitor near ITRIP pin. GND of the capacitor should be connected to Logic GND.

4. Input Capacitor and Zener Diode
   An input capaciter and a zener diode, a bootstrap capacitor should be located near the pin. It is recommended to select a low ESR capacitor such as a ceramic-type.

I/O Equivalence Circuits

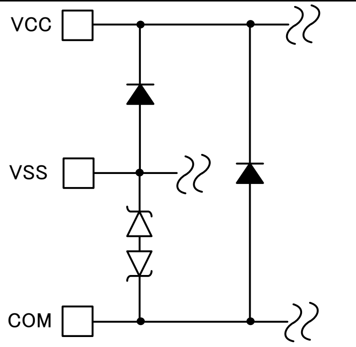
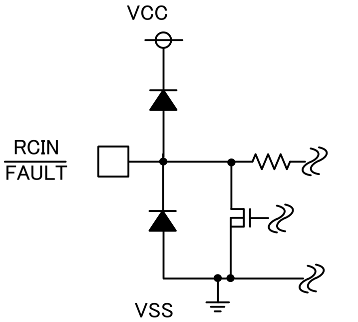
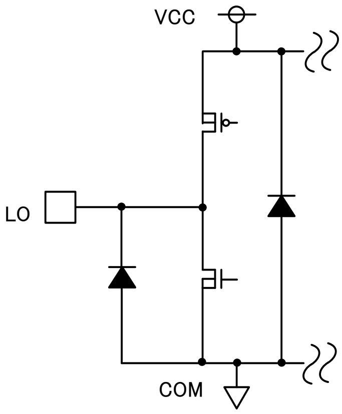
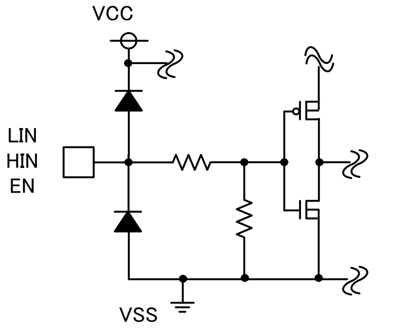
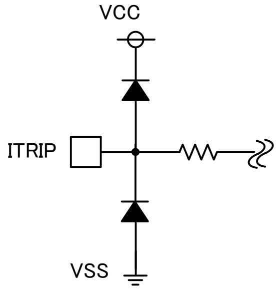
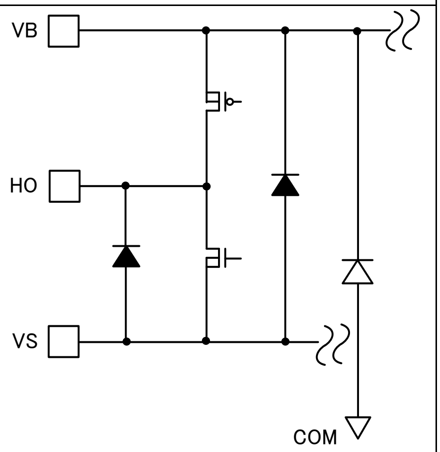
Pin.No	Pin Name	Pin Equivalent Circuit
1 12 13	VCC VSS COM	
8 11	/FAULT RCIN	
14,15,16	LO1,2,3	
2,3,4 5,6,7 10	HIN1,2,3 LIN1,2,3 EN	
9	ITRIP	
18,22,26 19,23,27 20,24,28	VS1,2,3 HO1,2,3 VB1,2,3	

Figure 43. I/O Equivalent Circuits

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Ceramic Capacitor**
    When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

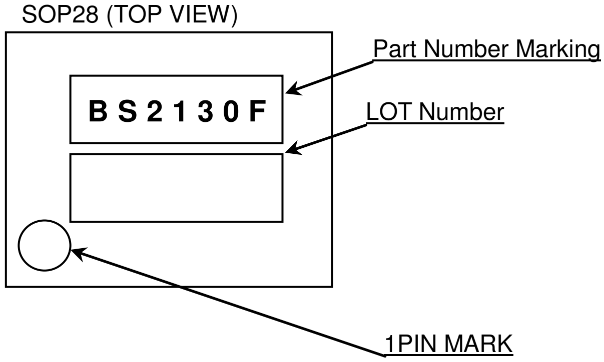
13. **Area of Safe Operation (ASO)**
    Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

Ordering Information

B S 2 1 3 0 F - GE 2

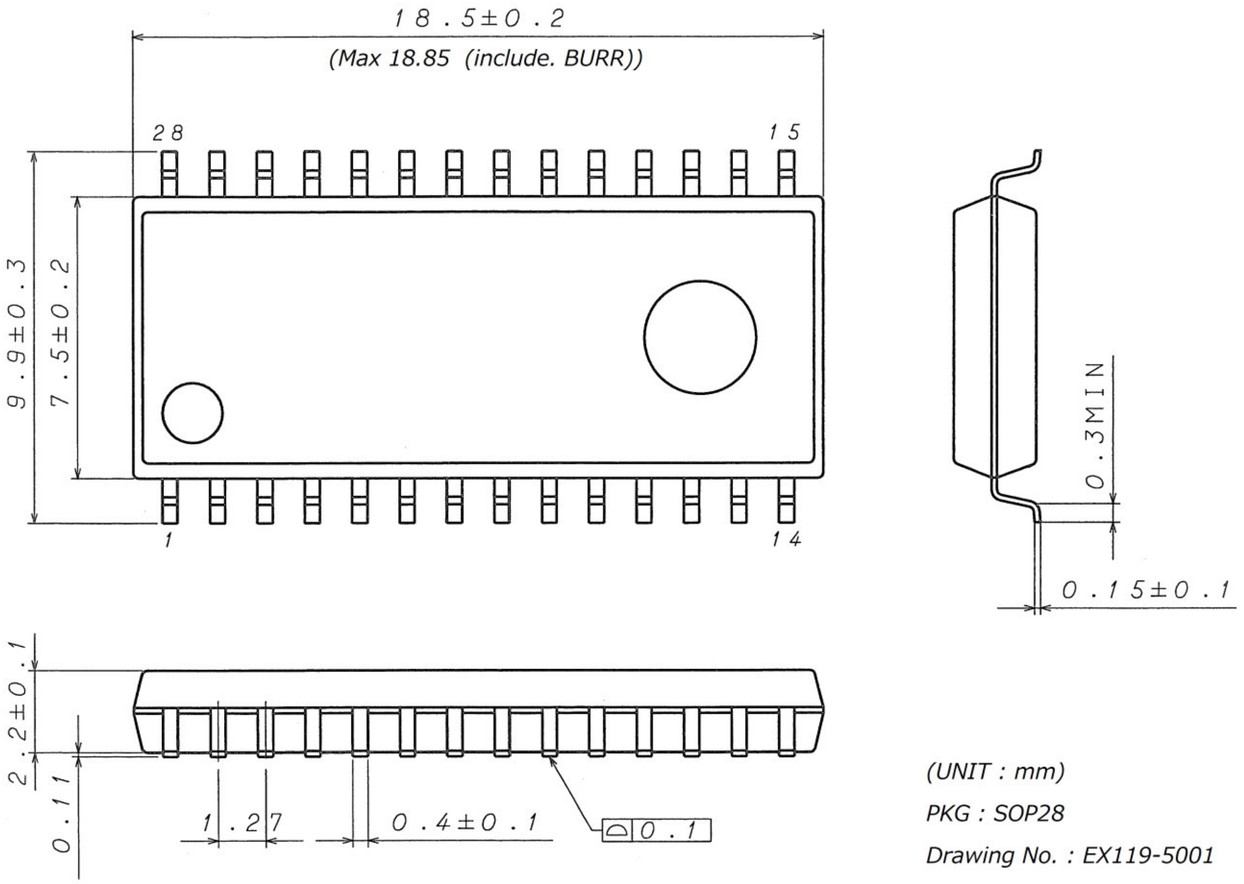
- Part Number
- Package
  F: SOP-28
- Package Material
  G: Halogen Free type
- Packaging and forming specification
  E2: Embossed tape and reel

Marking Diagram



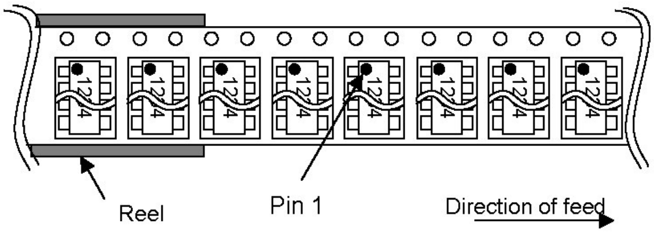
Physical Dimension, Tape and Reel Information

Package Name	SOP28



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
26.Feb.2016	001	New Release
31.May.2016	002	Addition P.21 Overshoot / Undershoot of Output Terminal Correction of errors P.4, P23

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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   [c] the Products are exposed to direct sunshine or condensation
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2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BS2130F-G - Web Page

Part Number	BS2130F-G
Package	SOP-28
Unit Quantity	1500
Minimum Package Quantity	1500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes