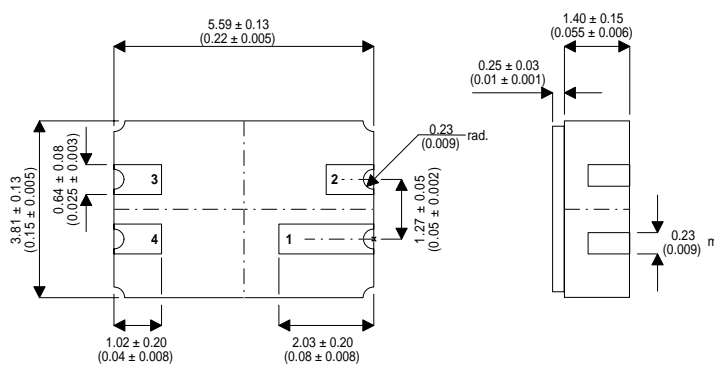


P-CHANNEL ENHANCEMENT MODE IN A CERAMIC SURFACE MOUNT PACKAGE FOR HIGH REL APPLICATIONS

MECHANICAL DATA

Dimensions in mm (inches)


FEATURES

- $V_{DSS} = 45V$
- $I_D = 0.18A$
- $r_{dson} = 14$ ohms
- Hermetic Surface Mount Package
- Screening Option Available

**LCC3 PACKAGE
Underside View**

PAD 1 - Drain **PAD 3 - Source**
PAD 2 - N/C **PAD 4 - Gate**

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise stated)

V_{DS}	Drain – Source Voltage		45V
V_{GS}	Gate – Source Voltage		$\pm 30V$
I_D	Continuous Drain Current	@ $T_A = 25^\circ C$	0.15A
		@ $T_A = 100^\circ C$	0.095A
I_{DM}	Pulsed Drain Current		0.69A
P_D	Power Dissipation	@ $T_A = 25^\circ C$	0.83W
		@ $T_A = 100^\circ C$	0.32W
T_{STG}, T_J	Maximum Junction and Storage Temperature Range		$150^\circ C$

ELECTRICAL RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
STATIC CHARACTERISTICS					
$V_{(BR)DSS}$ Drain – Source Breakdown Voltage	$V_{GS} = 0V$ $I_D = 100\mu A$	45	60		V
$V_{GS(TH)}$ Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 1mA$	1	2.7	3.5	
I_{GSS} Gate – Body Leakage	$V_{GS} = \pm 15V$ $V_{DS} = 0V$		± 1	± 20	nA
I_{DSS} Zero Gate Voltage Drain Current	$V_{DS} = 36V$ $V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			0.5	μA
				2000	
$I_{D(ON)}$ On State Drain Current ¹	$V_{DS} = 10V$ $V_{GS} = 10V$	0.2			A
$R_{DS(ON)}$ Drain – Source On-State Resistance ¹	$V_{GS} = 10V$ $I_D = 0.2A$ $T_J = 125^\circ\text{C}$			14	Ω
				28	
g_{fs} Forward Transconductance ¹	$V_{DS} = -10V$ $I_D = 0.2A$	100			mS
g_{os} Common Source Output Conductance	$V_{DS} = -7.5V$ $I_D = -0.1A$		600		μS
C_{iss} Input capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1MHz$		25	60	pF
C_{oss} Output capacitance			15	25	
C_{rss} Reverse transfer capacitance			4	8	
t_{on} Turn-on Time	$V_{DD} = 25V$ $R_L = 120\Omega$ $I_D = 200mA$ $R_G = 25\Omega$		16		ns
t_{off} Turn-off Time	$V_{GEN} = 10V$ (Switching time is essentially independent of operating temp.)		15		

NOTES:

1) Pulse Test: Pulse Width = $300\mu s$, Duty Cycle $\leq 2\%$