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DEVICE SPECIFICATION for
DIGITAL DBS TUNER with LINK

MODEL NO. BS2F7HZ0194

☐ CUSTOMER'S APPROVAL

DATE

BY

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DESCRIPTION: This specification covers DBS tuner intended for use in Digital Broadcasting Satellites. This tuner incorporates "LINK" section that is composed of DVB standard QPSK demodulation circuit and FEC(Forward Error Correction) circuit. This tuner has 8-bit transport stream output.

[1] GENERAL SPECIFICATIONS

1-1	Receiving frequency range		950MHz to 2150MHz
1-2	Input level		-65dBm to -25dBm
1-3	Input structure		F type Female
1-4	Nominal input impedance		75Ω
1-5	Channel selection system		PLL synthesizer(Clock 4.0MHz)
1-6	Step frequency		500kHz
1-7	I/Q output LPF cut off frequency(-3dB)		10MHz to 30MHz,variable(2MHz step)
1-8	Symbol rate		2Msps to 45Msps
1-9	Roll-off Factor		35% (root-raised cosine)
1-10	LINK IC		STV0299B(Clock:4MHz,Address:D0(HEX))
1-11	FEC	Inner decoder:	Viterbi soft decoder ,Constraint length M=7 Punctured codes 1/2,2/3,3/4,5/6,7/8 Automatic or manual rate and Phase recognition deinterleaver Word synchro extraction Convolutive deinterleaver
		Outer decoder:	Reed-solomon decoder ,for 16 parity bytes block lengths 204byte energy dispersal descrambler
1-12	Operating voltage		
	LNB voltage	(B1A)	25V, 400mA max.
	Supply voltage	(B2)	3.3V ± 0.165V DC
		(B3)	3.3V ± 0.165V DC
		(B4)	3.3V ± 0.165V DC
		(VDD)	2.5V ± 0.125V DC
1-13	Circuit block diagram		Fig.1
1-14	Connection diagram		Fig.2
1-15	Attention item:		This unit contains components that can be damaged by electro-static discharge. Before handling this unit, ground your hands, tools, working desks and equipment to protect the unit from Electronic Static Destroy.

[2]MECHANICAL SPECIFICATION

2-1	Dimension and mounting details	Fig.3
2-2	Strength of F-connector	No severe transform or distortion at bending moment, 98N·cm. To be connected electrically.
2-3	Clamp Torque of F-connector	No severe transform or distortion on the connection with F-connector at bending moment, 98N·cm. To be connected electrically.

[3] ENVIRONMENTAL SPECIFICATION

3-1	Temperature	Operating	0℃ to 60℃
		Storage	-20℃ to 85℃
3-2	Humidity	Operating	Less than 85%
		Storage	Less than 95%

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[4] TESTING CONDITION

4-1	Supply voltage	(B2)	3.3V ± 0.05V
		(B3)	3.3V ± 0.05V
		(B4)	3.3V ± 0.05V
		(VDD)	2.5V ± 0.05V
4-2	Ambient temperature		25℃ ± 5℃
4-3	Ambient humidity		65% ± 10%

[5]ELECTRICAL SPECIFICATION (Unless otherwise stated testing condition 4-1～4-3.)

No.	Item		Specification MIN.	TYP.	MAX.	UNIT	Condition
5-1	RF input VSWR			2.0	2.5		950MHz to 2150MHz
5-2	Noise figure(at max. gain)			8	12	dB	950MHz to 2150MHz
5-3	Intermodulation rejection Desired signal Fo Undesired signal (2 signals) (Fo+29.5MHz,Fo+59MHz) or (Fo-29.5MHz,Fo-59MHz)		40	60		dB	Input level:-25dBm I/Q Output level: $0.6V_{P-P}$(1kΩload) BBLPF Fc=20MHz
5-4	L.O. leak at input terminal			-68	-63	dBm	950MHz to 2150MHz
5-5	Eb/No for BER = 2 × 10^{-4} at viterbi output	PC= 1/2		3.7	4.5	dB	4≦Fs≦45[Msps] (Fs :symbol rate)
		PC= 2/3		4.2	5.0		
		PC= 3/4		4.7	5.5		
		PC= 5/6		5.3	6.0		
		PC= 7/8		5.7	6.4		
		PC= 1/2		4.8	5.5	dB	2≦Fs＜4[Msps]
		PC= 3/4		5.0	6.0		
		PC= 5/6		5.5	6.5		
		PC= 7/8		6.2	7.0		
				6.8	7.4		
5-6	PLL lock up time (C1,C0)=(1,1)			6	50	ms	
5-7	PLL phase noise (C1,C0)=(1,1)			-78	-70	dBc/Hz	10kHz offset
				-85	-80	dBc/Hz	100kHz offset
5-8	PLL reference leak			-40	-30	dBc	500kHz
5-9	RF output VSWR			2.0	2.5		950MHz to 2150MHz
5-10	RF output gain		-5	0	+5	dB	measured at RF out
5-11	Current consumption	B2		90	135	mA	B2=3.3V
		B3		5	15	mA	B3=3.3V
		B4		25	40	mA	B4=3.3V
		VDD		250	350	mA	VDD=2.5V

[6] PLL FUNCTION DESCRIPTION

PLL and VCO are promptly set up without fail when the user correctly program the data with the prompt I^2C access sequence as long as the following are also applied;

a) Follow the I^2C standard specification
b) Leave RTS to 0

6-1. I^2C-BUS DATA FORMATS

Table 1 ; Write data format (MSB is transmitted first)

MSB							LSB		
1	1	0	0	0	0(MA1)	0(MA0)	0	A	Byte1
0	N10	N9	N8	N7	N6	N5	N4	A	Byte2
N3	N2	N1	A5	A4	A3	A2	A1	A	Byte3
1	1(C1)	1(C0)	PD5	PD4	TM	0(R1)	1(R0)	A	Byte4
BA2	BA1	BA0	0(RTS)	PD3	PD2/TS2	DIV/TS1	PD0/TS0	A	Byte5

* A	; Acknowledge bit	
* N10 to N1	; Programmable division ratio control bits	(see Table 3)
* A5 to A1	; Swallow division ratio setting bits	(see Table 4)
* R1,R0	; Reference division ratio setting bits	(see Table 5)
* MA1,MA0	; Address setting bits	(see Table 6)
* PD0	; P0 control bit	(see Table 7)
* BA2,BA1,BA0	; Local oscillator select	(see Table 8)
* DIV	; Local oscillator divided ratio setting	
* PD5 to PD2	; BB LPF cut-off frequency setting	(see Table 9)
* RTS	; Test mode control bit	(see Table 10)
* TS2,TS1,TS0	; Test mode setting bits (when RTS=1)	
* C1,C0	; Charge pump current setting bits	(see Table 11)
* TM	; VCO/LPF adjustment mode setting bits	(see 8-2)

Write PLL register data to set one among the following I^2C access sequence as #a) to h).
It is available to skip the bytes which does not require for renewal or change the sequence of the bytes to choose one of the following.

I^2C start ->1st byte ->2nd byte ->3rd byte ->4th byte ->5th byte

a) I^2C start -> byte1 -> byte2 -> byte3 -> byte4 -> byte5 * byte1: I^2C address byte
b) I^2C start -> byte1 -> byte4 -> byte5 -> byte2 -> byte3 *
c) I^2C start -> byte1 -> byte2 -> byte3 -> byte4 -> either I^2C stop or (another) start
d) I^2C start -> byte1 -> byte4 -> byte5 -> byte2 -> either I^2C stop or (another) start
e) I^2C start -> byte1 -> byte2 -> byte3 -> either I^2C stop or (another) start
f) I^2C start -> byte1 -> byte4 -> byte5 -> either I^2C stop or (another) start
g) I^2C start -> byte1 -> byte2 -> either I^2C stop or (another) start
h) I^2C start -> byte1 -> byte4 -> either I^2C stop or (another) start

*: either I2C stop or (another) start is available to follow after the 5th byte, but not mandatory

(CAUTION) During receiving signals, don't access I^2C bus to satisfy the phase noise character specification.

(NOTE) PLL set up rule for PLL synthesizer

The following conditions are required to program the I^2C access sequence.
According to a required renewal data on each byte, one of the access sequence shown above as a) to h) should be chosen.

1) Write byte1 on the 1st byte after I^2C start.
2) Write either byte2 or byte4 on the 2nd byte. When the MSB header is 0 on the 2nd byte, the 2nd byte is recognized as byte2 or When the MSB header is 1 on the 2nd byte, the 2nd byte is recognized as byte4
3) The following byte after byte2 or byte4 should be the sequent # of the last byte as; The byte3 should be followed after byte2 or The byte5 should be followed after byte4.
4) The number of byte to write in one access sequence as from a start to a stop (or another start) state should be

two bytes at least. Review #g) and #h). Maximum bytes is five as write all byte 1 to byte5 data in one access sequence. Review #a) and #b)

5) The renewal of the register data is only available when it becomes a I2C stop or another start state after all the bytes to write in case of #c) to h). Only in the case when the renewal of the register data all from byte2 to byte5 in one access sequence as #a) and #b), a stop state or another start state is not mandatorily required for data renewal.

6) The data already registered and not to write for renewal has kept as it is as the last state.

7) Every time when the power is on, write all the register data on byte 2 to byte5 in one sequence for the purpose of the initial default set up to follow either #a) or #b). Because the initial values on byte 2 to byte5 are not fixed before the initialization.

Table 2 ; Read data format

MSB							LSB		
1	1	0	0	0	MA1	MA0	1	A	Byte1
POR	FL	X	x	x	x	x	x	A	Byte2

* POR ; Power on reset indicator (see table 12)
* FL ; Phase lock detect flag (see table 13)
* x ; don't care
* All data of byte2 will be "H", when "Power on reset" operates under the condition of a pulled up SDA.
* "Read mode" will change to "Write mode" after completing to output the byte2.

6-2. PROGRAMING

6-2-1 Programmable divider bits data

Please set P, N, A, R as follows.

$$fvco=[(P*N)+A]*fosc/R$$

fvco : Receiving frequency
P : Dividing factor of prescaler (32)
N : Programmable division ratio (5 to 1023)
A : Swallow division ratio (0 to 31 and A<N)
fosc : Reference oscillation frequency (4MHz)
R : Reference division ratio (see table5)

6-2-2 Data setting

Table 3 ; Programmable division ratio control (Binary:10bits)

Dividing factor(N)	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.
1023	1	1	1	1	1	1	1	1	1	1

Table 4 ; Swallow division ratio setting (Binary:5bits)

Dividing factor(A)	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0
1	0	0	0	0	1
.	.	.	.	.	.
31	1	1	1	1	1

* The using 4 or smaller of dividing factors is inhibited.
* The dividing factor is set by the data of N10 to N1 and A5 to A1 in byte 2,3,4 on I^2C write data. (table 1)

Table 5 ; Reference division ratio setting

(Binary:2bits)

R 1	R 0	dividing factor(R)	Compare frequency
0	0	4	1 MHz
0	1	8	500 KHz
1	0	16	250 KHz

The dividing factor is set by the data of R1and R0 in byte 4 on I^2C write data.

CAUTION:

Only use (R1, R0) = (0,1)

Other settings can't be assured

Table 6 ; Address selection

MA1	MA0	ADR input voltage
0	0	0V ~ 0.1VCC3
0	1	open
1	0	0.4VCC3 ~ 0.6VCC3
1	1	0.9VCC3 ~ VCC3

Table 7 ; P0 control

Input data (PD0)	Output of P0		
	Normal	Power on reset	Power on
1	L	Hi-Z	Hi-Z
0	Hi-Z	Hi-Z	

Hi-Z : High impedance

Table 8 ; Local oscillator select

BAND	DIV	BA2	BA1	BA0	Local frequency (Receiving frquency)	Divider ratio
1	1	1	1	0	950MHz to 1065MHz	1/4
2	1	1	1	1	1065MHz to 1170MHz	1/4
3	0	0	0	1	1170MHz to 1300MHz	1/2
4	0	0	1	0	1300MHz to 1445MHz	1/2
5	0	0	1	1	1445MHz to 1607MHz	1/2
6	0	1	0	0	1607MHz to 1778MHz	1/2
7	0	1	0	1	1778MHz to 1942MHz	1/2
8	0	1	1	0	1942MHz to 2150MHz	1/2

Table 9 ; Baseband LPF cut-off frequency setting

PD2	PD3	PD4	PD5	LPF cut-off Frequency
0	0	1	1	10.0 MHz
0	1	0	0	12.0 MHz
0	1	0	1	14.0 MHz
0	1	1	0	16.0 MHz
0	1	1	1	18.0 MHz
1	0	0	0	20.0 MHz
1	0	0	1	22.0 MHz
1	0	1	0	24.0 MHz
1	0	1	1	26.0 MHz
1	1	0	0	28.0 MHz
1	1	0	1	30.0 MHz

Table 10 ; Test mode setting

RTS	TS2	TS1	TS0	Test mode
0	X	X	X	Normal operation
1	0	0	0	Charge pump sink (FL=1)
1	0	0	1	Charge pump source (FL=0)
1	0	1	0	Charge pump disable (FL=0)
1	0	1	1	Output fp/2 at port terminal PO
1	1	0	0	Output fr/2 at port terminal PO

X :don't care

* When RTS=1 on "I^2C write data (table 1)", it changes to test mode.

Table 11 ; Charge pump output current selection

C1	C0	Charge pump output current [micro A]		
		min	typ	max
0	0	+/- 90	+/- 120	+/- 150
0	1	+/- 195	+/- 260	+/- 325
1	0	+/- 416	+/- 555	+/- 694
1	1	+/- 900	+/- 1200	+/- 1500

Table 12 ; POR bit polarity

	VCC3 > 2.2V	VCC3 < 2.2V
POR bit	L	H

Table 13 ; FL bit polarity

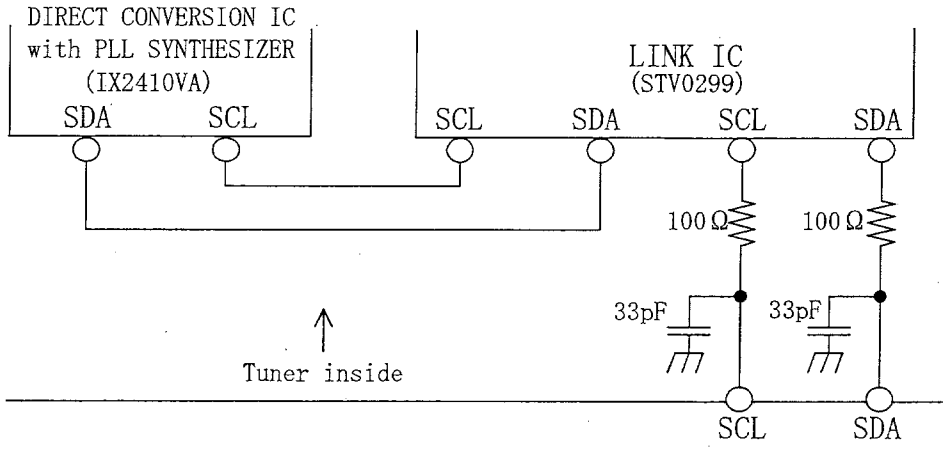
	lock	unlock
FL bit	H	L

* SDA has to be pulled up.

6-3.INTERFACE CIRCUITS

The interface of this tuner is as following table.

Tuner pin No.	I^2C port	Note
8	SDA	Refer to following figure
9	SCL	



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[7] CONFIGURATION REGISTERS

Table 7-1:STV0299's Test Register Value

Name	Address	Test Value	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Comment
ID	00(r/w)	A1	Chip identification number			Release number					
RCR	01(w)	15	K(1:0)		dirclk	M(4:0)					
MCR	02(w)	30	stdby	VCO off	1	1	serclock	P(2:0)			4MHz at CK-IN, VCO=352MHz
ACR	03(w)	2A	prescaler			divider					Note1, MCLK=88MHz
F22FR	04(w)	7D	frequency register f_reg(7:0)								Note1
I2CRPT	05(w)	05	I2CT	0	0	0	0	SCLT value		SDAT value	
DACR1	06(w)	A2	DAC mode				DAC(11:8)				Note1
DACR2	07(w)	00	DAC(7:0)								Note1
DiSEqC	08(w)	60	LOCK output		LOCK conf	0	0	DiSEqC	DiSEqC mode		Note1,Note3
DiSEqC FIFO	09(w)	00	DiSEqc FIFO(7:0)								
DiSEqC Status	0A(r)	-	IP	SDAT input status					FE	FF	Note1
IOCFG	0C(w)	F1	OP1_ opdrain	OP1_1	OP0_ opdrain	OP0_1	0	Niquist filter		I/Q conv	Note1
AGC1C	0D(w)	81	Dcadj					bata_agc1(2:0)			
RTC	0E(w)	23		alpha_tmg(2:0)				beta_tmg(2:0)			
AGC1R	0F(w)	19	Iagc		Reference Vallue						Note1
AGC20	10(w)	3F	AGC2_coef			AGC2_Ref					
TLSR	11(w)	84	step_minus(3:0)			step_plus(3:0)					
CFD	12(w)	F7	FD on/off	beta_fd		FDTC		LDL			Note4
ACLC	13(w)	98	derot on/off	0	noise_TC	alpha_car					
BCLC	14(w)	*	Ph_detect_algo	beta_car							Note2
CLDT	15(w)	14	Lock_Detector_Threshold								Note4
AGC1I	16(r/w)	-	AGC Integrator Value								
TL1R	17(r)	-	Timing lock indicator(7:0)								
AGC2I1	18(r/w)	-	AGC2 integrator MSB								
AGC2I2	19(r/w)	-	AGC3 integrator LSB								
RTF	1A(r/w)	-	Timing Loop Frequency(7:0)								
VSTATUS	1B(r)	-	CF			PRF	LK	PR(2:0)			
CLDI	1C(r)	-	Lock Detector Integrator								
ERRCNT-HIGH	1D(r)	-	Error Count MSBs								
ERRCNT-LOW	1E(r)	-	Error Count LSBs								
SFRH	1F(w)	*	Symb_freq(19:12)								Depend on requested symbol rate
SFRM	20(w)	*	Symb_freq(11:4)								
SFRL	21(w)	*	Symb_freq(3:0)				0	0	0	0	Note5
CFRM	22(r/w)	-	Carrier Frequency Register MSB								
CFRL	23(r/w)	-	Carrier Frequency Register LSB								
NIRG	24(r)	-	Noise Indicator MSBs								
NIRL	25(r)	-	Noise Indicator LSBs								
VERROR	26(r)	-	Error Value								
MSTATUS	27(r)	-	ARESET	INIT	STOP	MWAIT	DMAACK	CCI	error	mstatus_0	
FECM	28(w)	0	FEC mode				0	0	out type	out imp	Note1
VTH0	29(w)	1E	t0(6:0)								Note4
VTH1	2A(w)	14	t1(6:0)								
VTH2	2B(w)	0F	t2(6:0)								
VTH3	2C(w)	09	t3(6:0)								
VTH4	2D(w)	05	t4(6:0)								
PR	31(w)	1F	0	0	0	E4	E3	E2	E1	E0	
VSEARCH	32(w)	19	A/M	FECmode	SN(1:0)		TO(1:0)		H(1:0)		
RS	33(w)	FC	deint	sync	RS	descram	Err bit	MPEG	clk pol	clk cfg	
ERRCNT	34(w)	13	Errmode	0	Error Source		0	0	NOE		

Note1 The level depend on the hardware configration of the application.

Note2 Bit 0 to 5 are dependent symbol rate

10M～45Mbaud	95
5M～10Mbaud	8F
2M～5Mbaud	89

Note3 22kHz pulse on:63/off:60

Note4 When C/N is low, test value is the following

Address	Value
12	39
15	C9
29	28

Note5 Symb_freq(19:0)=symbol rate/(MCLK/2^{20})

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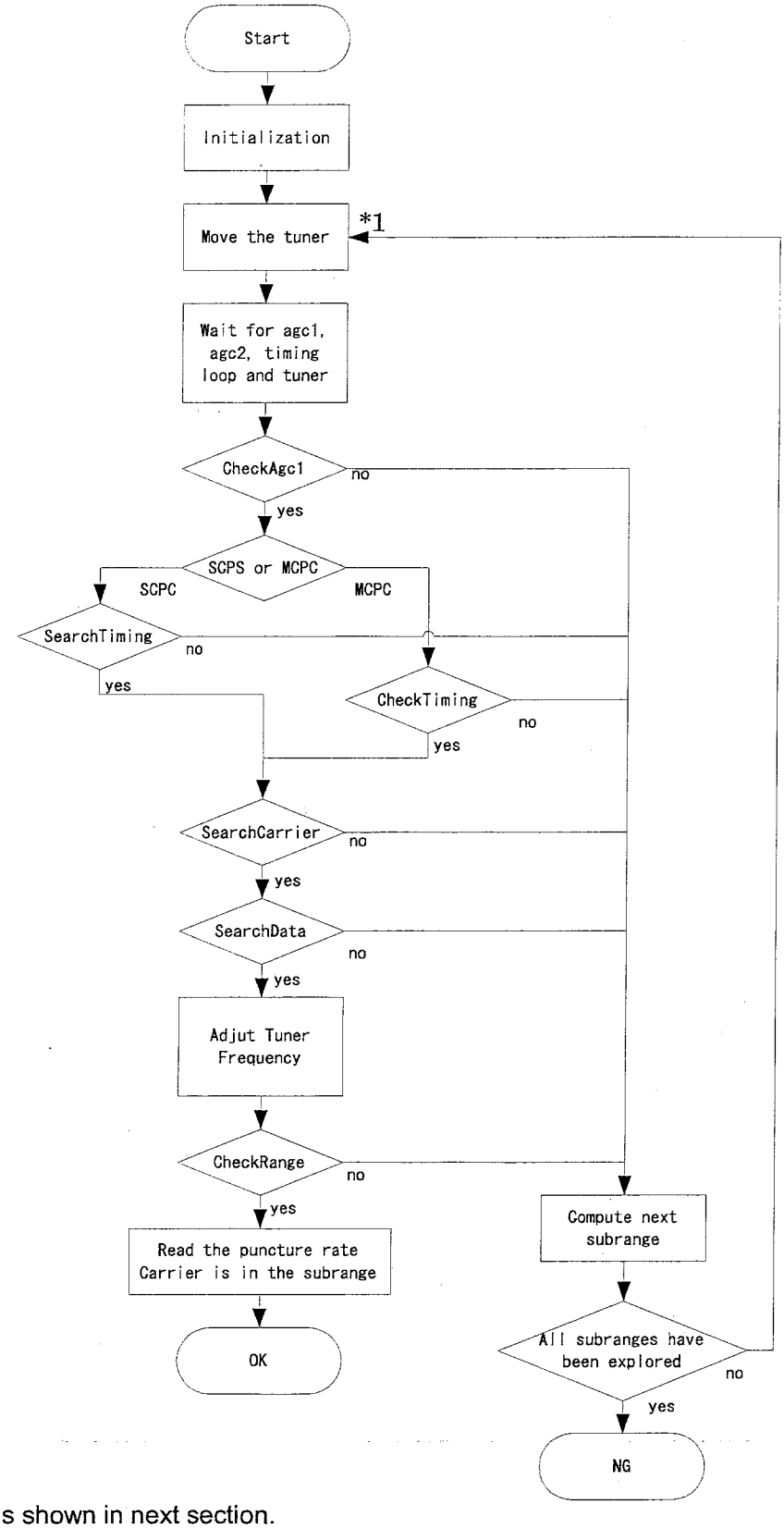
[8]TUNER CONTROL PROCEDURE

8-1 FLOW CHART

The following flow charts show recommended internal PLL and STV0299 control flows.



*1 Tuning details is shown in next section.

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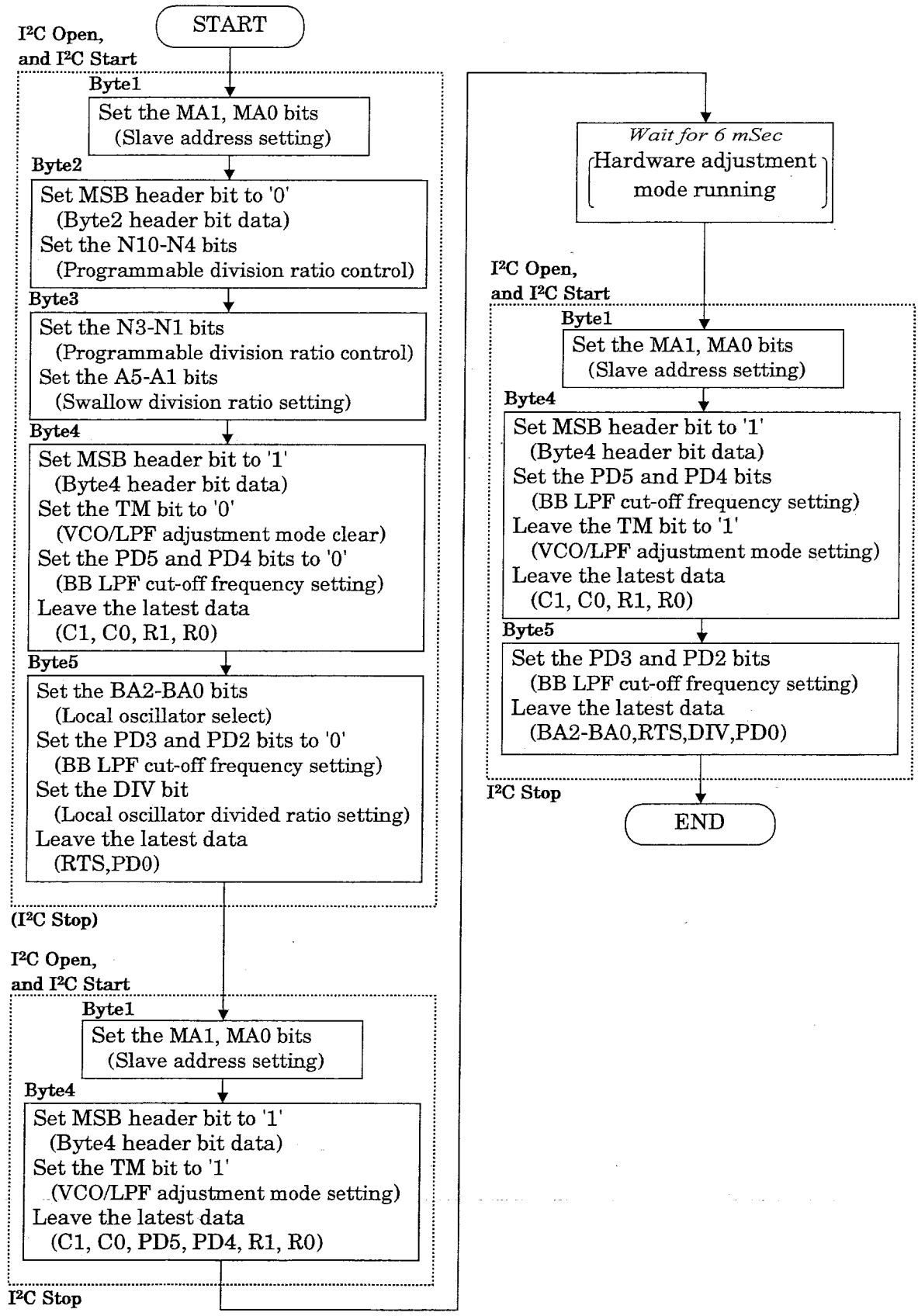
8-2 VCO AND LPF ADJUSTMENT MODE SETTING SEQUENCE AFTER POWER ON



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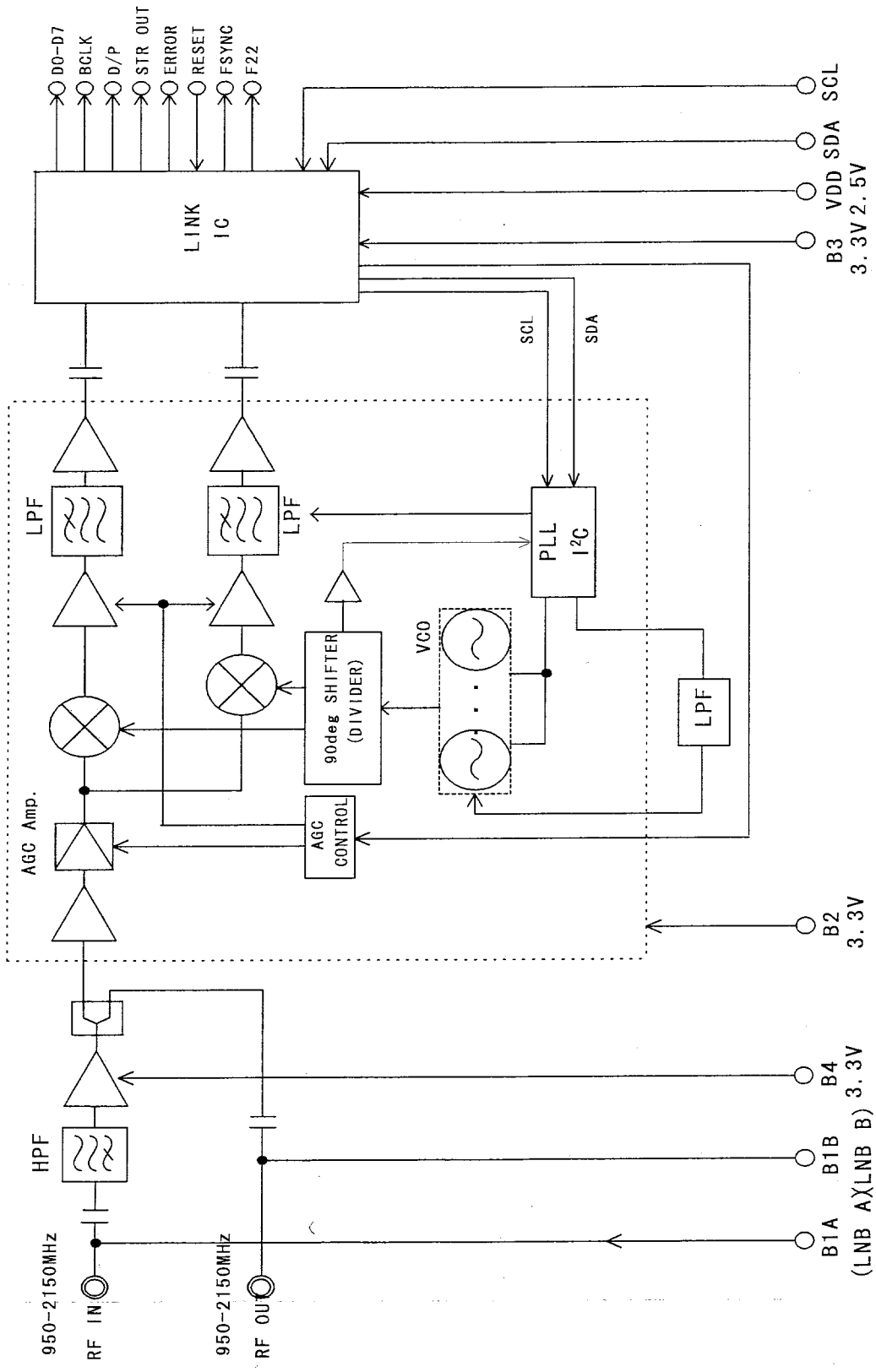

Fig 1. BLOCK DIAGRAM

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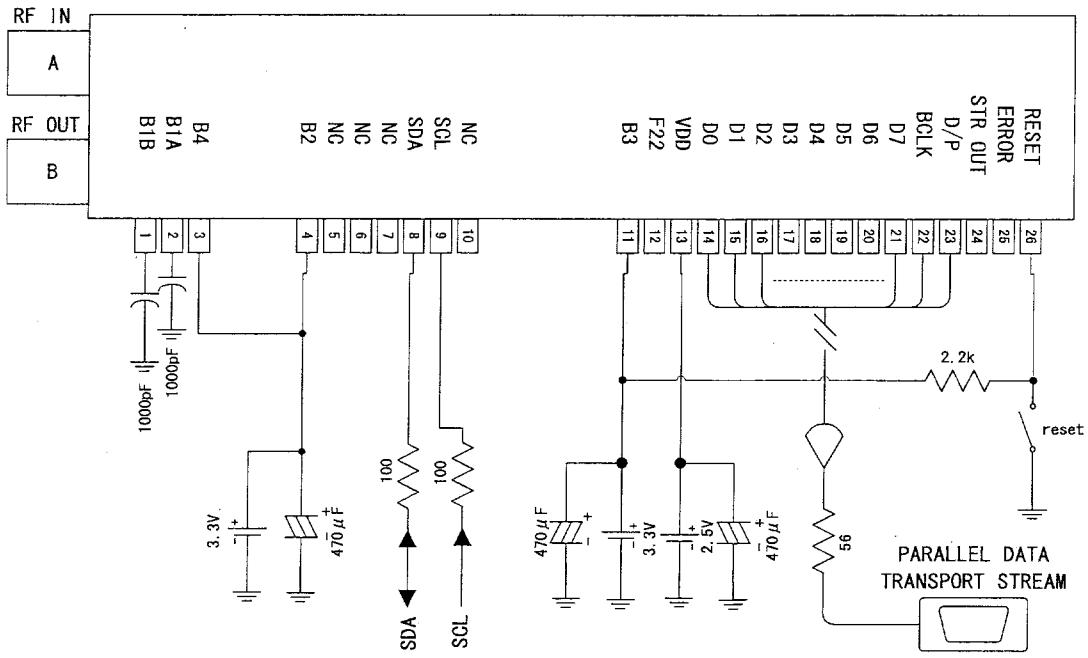
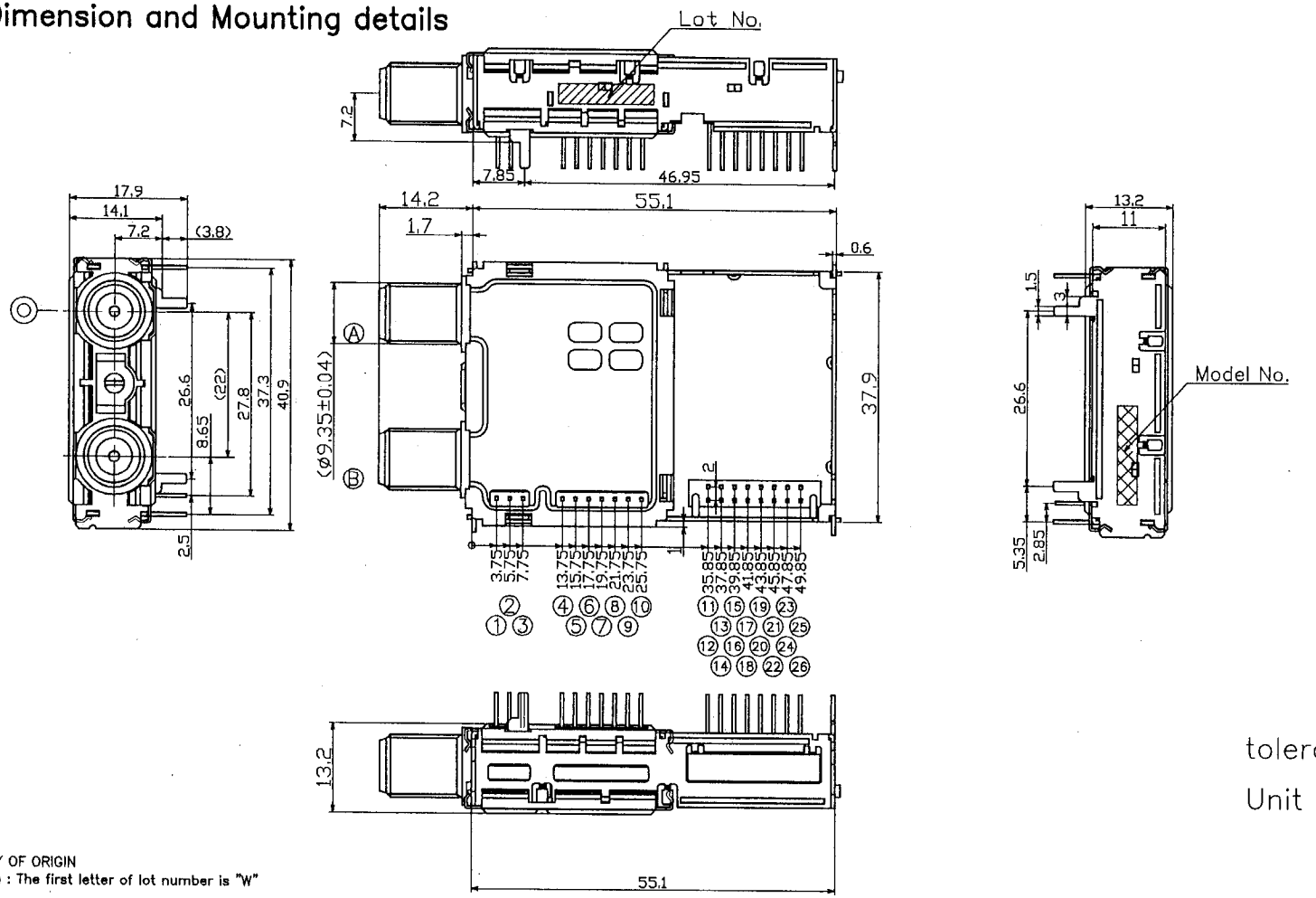


Fig 2. CONNECTION DIAGRAM

PIN LIST

PIN NAME	PIN No.	PIN DESCRIPTION
B1B	1	Voltage supply of LNB B. Please ground it with a 1000pF ceramic capacitor.
B1A	2	Voltage supply of LNB A. Please ground it with a 1000pF ceramic capacitor.
B4	3	3.3V supply for RF Booster Amp of tuner.
B2	4	3.3V supply for the Front-end section. Please keep a ripple at the Power Supply less than 10mVp-p.
NC	5,6,7,10	It is not connected inside the unit. We advice to ground it.
SDA	8	I^2C Bus. Please connect a pull-up resistor which is more than 2k ohm outside of the tuner.
SCL	9	
B3	11	3.3V supply for LINK IC.
F22	12	Pulse output for LNB.
VDD	13	2.5V supply for LINK IC.
D0,...,D7	14,...,21	Transport Stream (TS) Packet output.
BCLK	22	Transport stream byte clock output data.
D/P	23	Transport stream enable output data. While the effective data in the packet is streaming, it outputs "H". While the other data (parity byte, etc) is streaming, it outputs "L".
STR OUT	24	Packet synchronization output. It outputs "Start Signals" for each packet. While the synchronized byte in the top of the packet is streaming, it outputs "H".
ERROR	25	Error indicator output. For the packets, where the errors could not be corrected by the read solomon decoder, "H" is outputted, where the errors could be corrected, "L" is outputted.
RESET	26	Reset input. If "L" is inputted, the LINK IC is initialized. When powering the unit, please input the reset signal. Please input "H", when the unit should not be initialized.

Fig 3 Dimension and Mounting details



Note : The COUNTRY OF ORIGIN
Made in China : The first letter of lot number is "W"

tolerances : ±0.3mm

Unit : mm

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Recommended location and dimension of pin holes on mother PWB
(Reference drawing)

▨ A special vacant space like this area is structualy required (dead spaee)