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FOR CUSTOMER'S APPROVAL

DEVICE SPECIFICATION for
DIGITAL DBS TUNER with LINK

MODEL NO. BS2F7HZ0164

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RF DEVICES DIVISION
ELECTRONIC COMPONENTS GROUP

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DESCRIPTION:

This specification covers DBS tuner intended for use in Digital Broadcasting Satellites. This tuner incorporates "LINK" section that is composed of 8bit ADC, multistandard DVB-S/DVB-S2 demodulator and multistandard FEC. This tuner has DVB common interface compliant transport stream output.

[1] GENERAL SPECIFICATIONS

| | |
|---|---|
| 1-1. Receiving frequency range | 950MHz to 2150MHz |
| 1-2. Input level | -65dBm to -25dBm |
| 1-3. Input structure | F type Female |
| 1-4. Nominal input impedance | 75 ohm |
| 1-5. Channel selection system | PLL synthesizer built in tuner IC “IX2470VA”<br>(Address:C0h)<br>(Reference clock: Internal 4.0MHz crystal oscillation) |
| 1-6. Tuning step frequency | 1MHz |
| 1-7. Cutoff frequency of Baseband(=I/Q out) LPF | Variable from 10MHz to 34MHz by 2MHz step |
| 1-8. LINK IC | STB0899 (Address: D0h)<br>(Reference clock: 4MHz supplied from “IX2470VA”) |
| 1-9. System clock specification | $F_{sampling}=F_{M\_CLK}=99MHz$ |
| 1-10. Multistandard demodulation and decoding | [DVB-S]<br>>Channel symbol rate up to QPSK 45MSps<br>>Inner Viterbi and Outer Reed-solomon decoding<br>>Punctured rates 1/2, 2/3, 3/4, 5/6, 6/7, 7/8<br>[DVB-S2]<br>>Channel symbol rates up to QPSK 36MSps, and 8PSK 30MSps<br>>Inner LDPC and outer BCH decoding<br>>Punctured rates 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10 |
| 1-11. Operating voltage | (B2, B3 and B4) 3.3V +/- 0.165V DC<br>(VDD) 1.8V +/- 0.090V DC |
| 1-12. Storage condition | Temperature 15 deg.C to 35 deg.C<br>Humidity 25 %RH to 75 %RH<br>Period 6 months |
| 1-13. Environmental characteristics | RoHS compliant<br>(RoHS refers to the "DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.") |

1-14. Attention items:

1) This unit contains components that can be damaged by electro-static discharge. Before handling this unit, ground your hands, tools, working desks and equipment to protect the unit from Electronic Static Destroy.
2) Avoid following actions;
   a) to store this unit in the place of the high temperature and humidity.
   b) to expose this unit to corrosive gases.

[2] MECHANICAL SPECIFICATION

| | |
|---|---|
| 2-1. Dimension and mounting details | see section [14] |
| 2-2. Mass | 44g (typical) |
| 2-3. Strength of F-connector | No severe transform or distortion at bending moment, 0.98N・m. To be connected electrically. |
| 2-4. Clamp Torque of F-connector | No severe transform or distortion on the connection with F-connector at bending moment, 0.98N・m. To be connected electrically. |

[3] ENVIRONMENTAL SPECIFICATION
(ELECTRICAL FUNCTIONAL OPERATION GUARANTEE)

| | | |
|---|---|---|
| 3-1. Operating | Temperature | 0deg.C to +50deg.C |
| | Humidity | Less than 85% No condensation |
| 3-2. Storage | Temperature | -20deg.C to +85deg.C |
| | Humidity | Less than 95% Water vapor pressure 6643Pa max, without condensation |

<Notice>
Please be careful that sudden temperature changes may cause condensation during storage, and such condensation may cause corrosion.

[4] ABSOLUTE MAXIMUM VOLTAGE

| Pin name | Pin No. | MIN. | MAX | UNIT | Note |
|---|---|---|---|---|---|
| B1B | 1 | | 25 | V | 400mA max. |
| B1A | 2 | | 25 | V | 400mA max. |
| B4 | 3 | -0.3 | 3.63 | V | |
| B2 | 4 | -0.3 | 4.0 | V | |
| B3 | 11 | -0.25 | 3.63 | V | |
| VDD | 13 | -0.1 | 2.0 | V | |
| SDA, SCL, RESETB | 8, 9, 26 | -0.3 | B3+0.3 | V | |

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[5] TESTING CONDITION

5-1. Supply voltage

| Pin name | Pin No. | MIN. | TYP. | MAX. | UNIT | Note |
|---|---|---|---|---|---|---|
| B4 | 3 | 3.25 | 3.30 | 3.35 | V | |
| B2 | 4 | 3.25 | 3.30 | 3.35 | V | |
| B3 | 11 | 3.25 | 3.30 | 3.35 | V | |
| VDD | 13 | 1.77 | 1.80 | 1.83 | V | |

5-2. Ambient temperature 25deg.C +/- 5deg.C

5-3. Ambient humidity 65% +/- 10%

[6] ELECTRICAL SPECIFICATION （Unless otherwise stated testing condition 5-1～5-3.）

| No. | Item | | Specification | | | | Condition |
|---|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | UNIT | |
| 6-1 | RF input VSWR | | | 2.0 | 2.5 | | 950MHz to 2150MHz |
| 6-2 | Noise figure(at max. gain) | | | 8 | 12 | dB | 950MHz to 2150MHz |
| 6-3 | 3rd order Intermodulation Undesired signal (2 signals) ($F_D$+29.5MHz, $F_D$+59MHz) or ($F_D$ -29.5MHz, $F_D$ -59MHz) | | 40 | 60 | | dB | Input level: -25dBm<br>I/Q amplitude: 0.6$V_{P-P}$<br><br>BBLPF Fc=30MHz |
| 6-4 | L.O. leak at input terminal | | | -68 | -63 | dBm | 950MHz to 2150MHz |
| 6-5 | PLL synthesizer tuning time | | | 10 | 50 | ms | limited to IX2470VA |
| 6-6 | PLL phase noise | | | -80 | -70 | dBc/Hz | 10kHz offset |
| | | | | -91 | -86 | dBc/Hz | 100kHz offset |
| 6-7 | PLL reference leak | | | -40 | -30 | dBc | 1MHz |
| 6-8 | RF output VSWR | | | 2.0 | 2.5 | | 950MHz to 2150MHz |
| 6-9 | RF output gain | | -5 | 0 | +5 | dB | measured at RF out |
| 6-10 | Current consumption | B2 | | 90 | 135 | mA | 3.3V |
| | | B3 | | 70 | 130 | mA | 3.3V |
| | | B4 | | 25 | 40 | mA | 3.3V |
| | | VDD | | 1200 | 1800 | mA | 1.8V |

[7] ERROR RATE PERFORMANCE

Es/No performance at Quasi Error Free

| Mode | ETSI Ideal | Performance (Typical) | Unit | Note |
|---|---|---|---|---|
| QPSK 1/2 | 1.00 | 1.2 | dB | >DVB-S2<br>>Pilot: ON<br>>BW = Synbol_rate<br>>BERTester: SFU |
| QPSK 3/5 | 2.23 | 2.4 | | |
| QPSK 2/3 | 3.10 | 3.2 | | |
| QPSK 3/4 | 4.03 | 4.2 | | |
| QPSK 4/5 | 4.68 | 4.8 | | |
| QPSK 5/6 | 5.18 | 5.3 | | |
| QPSK 8/9 | 6.20 | 6.4 | | |
| QPSK 9/10 | 6.42 | 6.6 | | |
| 8PSK 3/5 | 5.50 | 5.8 | | |
| 8PSK 2/3 | 6.62 | 6.8 | | |
| 8PSK 3/4 | 7.91 | 8.1 | | |
| 8PSK 5/6 | 9.35 | 9.6 | | |
| 8PSK 8/9 | 10.69 | 10.9 | | |
| 8PSK 9/10 | 10.98 | 11.3 | | |

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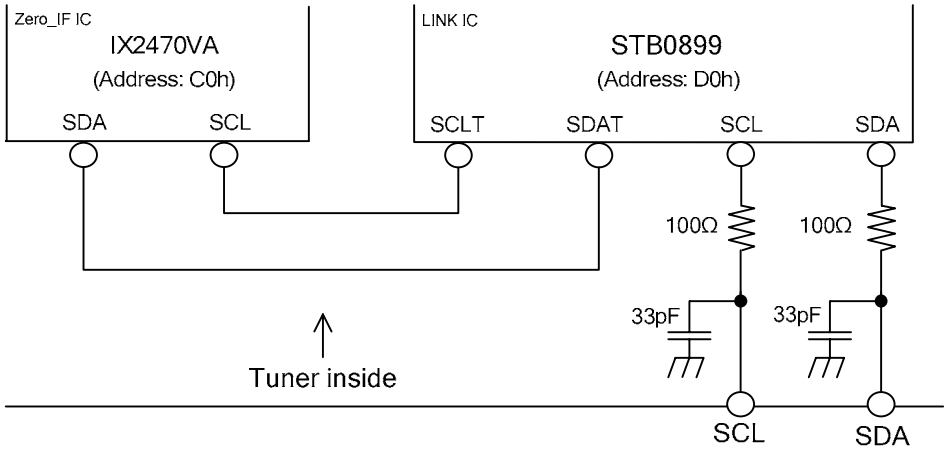
[8] I²C INTERFACE

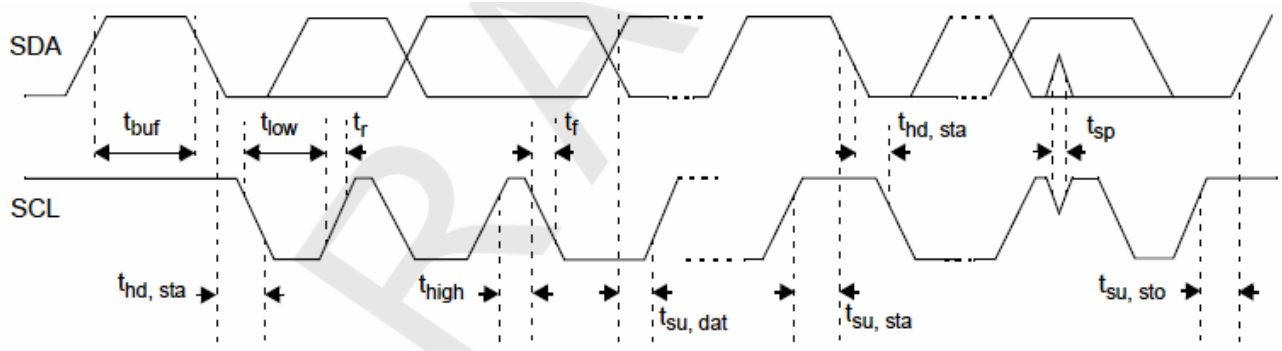
8-1. Internal circuits

The interface of this tuner is as following figure. It is using the I²C private repeater of STB0899 for tuner isolation.




8-2. I2C bus characteristic (conforms to the specification of STB0899)

| Item | Synbol | MIN. | MAX. | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage | $v_{ih}$ | 2.0 | 3.6 | V | |
| Input low voltage | $v_{il}$ | -0.5 | 0.8 | V | |
| SCL clock rate | $f_{scl}$ | | 400 | kHz | Normal mode |
| Bus free time between a stop and start condition | $t_{buf}$ | 1.3 | | us | |
| Hold time (repeated) start condition | $t_{hd,\ sta}$ | 0.6 | | us | After this period, the first clock pulse is generated. |
| Low period of the SCL | $t_{low}$ | 1.3 | | us | |
| High period of the SCL | $t_{high}$ | 0.6 | | us | |
| Rise time for SDA and SCL | $t_r$ | | 300 | ns | Fast mode |
| Fall time for SDA and SCL | $t_f$ | | 300 | ns | Fast mode |
| Setup time for a repeated start condition | $t_{su,\ sta}$ | 0.6 | | us | |
| Setup time for stop condition | $t_{su,\ sto}$ | 0.6 | | us | |
| Data setup time | $t_{su,\ dat}$ | 100 | | ns | |
| Pulse width of spikes to be suppressed by input filter | $t_{sp}$ | | 50 | ns | Fast mode |



[9] IX2470VA FUNCTIONAL DESCRIPTION

PLL and VCO are promptly set up without fail when the user correctly program the data with the prompt $I^2C$ access sequence as long as the following are also applied;

a) Follow the $I^2C$ standard specification
b) Leave RTS to 0

9-1. $I^2C$-BUS DATA FORMATS

Table 1 ; Write data format (MSB is transmitted first)

| MSB | | | | | | | LSB | | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0(MA1) | 0(MA0) | 0 | A | Byte1 |
| 0 | 1(BG1) | 0(BG0) | N8 | N7 | N6 | N5 | N4 | A | Byte2 |
| N3 | N2 | N1 | A5 | A4 | A3 | A2 | A1 | A | Byte3 |
| 1 | 1(C1) | 1(C0) | PD5 | PD4 | TM | 0(RTS) | REF | A | Byte4 |
| BA2 | BA1 | BA0 | PSC | PD3 | PD2/TS2 | DIV/TS1 | PD0/TS0 | A | Byte5 |

| | | |
|---|---|---|
| * A | ; Acknowledge bit | |
| * N8 to N1 | ; Programmable division ratio control bits | (see Table 3) |
| * A5 to A1 | ; Swallow division ratio setting bits | (see Table 4) |
| * REF | ; Reference division ratio setting bits | (see Table 5) |
| * PSC | ; Prescaler division ratio setting bits | (see Table 6) |
| * MA1, MA0 | ; Address setting bits | (see Table 7) |
| * PD0 | ; PO control bit | (see Table 8) |
| * BA2, BA1, BA0 | ; Local oscillator select | (see Table 9) |
| * DIV | ; Local oscillator divided ratio setting | |
| * PD5 to PD2 | ; BB LPF cut-off frequency setting | (see Table 10) |
| * RTS | ; Test mode control bit | (see Table 11) |
| * TS2, TS1, TS0 | ; Test mode setting bits (when RTS = '1') | |
| * C1, C0 | ; Charge pump current setting bits | (see Table 12) |
| * BG1, BG0 | ; BB AMP gain setting bits | (see Table 13) |
| * TM | ; VCO/LPF adjustment mode setting bits | (see section 9-3) |

Write PLL register data to set one among the following $I^2C$ access sequence as #a) to h).
It is available to skip the bytes which does not require for renewal or change the sequence of the bytes to choose one of the following.

$I^2C$ start->1st byte->2nd byte->3rd byte->4th byte->5th byte

a) $I^2C$ start -> byte1 -> byte2 -> byte3 -> byte4 -> byte5 * byte1: $I^2C$ address byte
b) $I^2C$ start -> byte1 -> byte4 -> byte5 -> byte2 -> byte3 *
c) $I^2C$ start -> byte1 -> byte2 -> byte3 -> byte4 -> either $I^2C$ stop or (another) start
d) $I^2C$ start -> byte1 -> byte4 -> byte5 -> byte2 -> either $I^2C$ stop or (another) start
e) $I^2C$ start -> byte1 -> byte2 -> byte3 -> either $I^2C$ stop or (another) start
f) $I^2C$ start -> byte1 -> byte4 -> byte5 -> either $I^2C$ stop or (another) start
g) $I^2C$ start -> byte1 -> byte2 -> either $I^2C$ stop or (another) start
h) $I^2C$ start -> byte1 -> byte4 -> either $I^2C$ stop or (another) start

*: Either $I^2C$ stop or (another) start is available to follow after the 5th byte, but not mandatory

CAUTION: During receiving signals, don't access $I^2C$ bus to satisfy the phase noise character specification.

NOTE: PLL set up rules

The following conditions are required to program the $I^2C$ access sequence.
According to a required renewal data on each byte, one of the access sequence shown above as a) to h) should be chosen.

1) Write byte1 on the 1st byte after $I^2C$ start.
2) Write either byte2 or byte4 on the 2nd byte.
   When the MSB header is 0 on the 2nd byte, the 2nd byte is recognized as byte2.
   When the MSB header is 1 on the 2nd byte, the 2nd byte is recognized as byte4.
3) The following byte after byte2 or byte4 should be the sequent # of the last byte as;
   The byte3 should be followed after byte2.
   The byte5 should be followed after byte4.
4) The number of byte to write in one access sequence as from a start to a stop (or another start) state should be two bytes at least. Review #g) and #h). Maximum bytes are five as write all byte1 to byte5 data in one access sequence. Review #a) and #b)
5) The renewal of the register data is only available when it becomes an $I^2C$ stop or another start state after all the bytes to write in case of #c) to h). Only in the case when the renewal of the register data all from byte2 to byte5 in one access sequence as #a) and #b), a stop state or another start state is not mandatory required for data renewal.
6) The data already registered and not to write for renewal has kept as it is as the last state.
7) Every time when the power is on, write all the register data on byte2 to byte5 in one sequence for the purpose of the initial default set up to follow either #a) or #b). Because the initial values on byte2 to byte5 are not fixed before the initialization.
8) As for POR (POWER ON RESET) of this tuner, the rise of the power-supply voltage might not operate normally when it is not linear, and the noise enters while the power-supply voltage is rising. For this case, the tuner might not accept the data input (Ack is not returned). Please input data again (re-try) for this case.

Table 2; Read data format

| MSB | | | | | | | LSB | | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | 1 | A | Byte1 |
| POR | FL | RD2 | RD1 | RD1 | X | X | X | A | Byte2 |

* POR ; Power on reset indicator (see table 14)
* FL ; Phase lock detect flag (see table 15)
* RD2 – RD0 ; Reserved (These bit values change under the condition of ICs.)
* X ; don't care
* All data of byte2 will be "H", when "Power on reset" operates under the condition of a pulled up SDA.
* "Read mode" will change to "Write mode" after completing to output the byte2.

9-2. PROGRAMING

9-2-1 Programmable divider bits data

Please set P, N, A, R as follows.

$$fvco = [(P * N) + A] * fosc / R$$

fvco: Receiving frequency
P : Dividing factor of prescaler (16 or 32)
N : Programmable division ratio (5 to 255)
A : Swallow division ratio (0 to 31 and A < N)
fosc: Reference oscillation frequency (4 MHz)
R : Reference division ratio (see table 5)

9-2-2 Data setting

Table 3; Programmable division ratio control (Binary: 8 bits)

| Dividing factor (N) | Bit data | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 |
| 5 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| · | · | · | · | · | · | · | · | · |
| 255 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 4; Swallow division ratio setting (Binary: 5 bits)

| Dividing factor (A) | Bit data | | | | |
|---|---|---|---|---|---|
| | A5 | A4 | A3 | A2 | A1 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| · | · | · | · | · | · |
| 31 | 1 | 1 | 1 | 1 | 1 |

* The using of 4 or smaller dividing factors is inhibited.
* The dividing factor is set by the data of N8 to N1 and A5 to A1 in byte2, 3 on $I^2C$ write data. (table 1)

Table 5; Reference division ratio setting (Binary: 1 bit)

| REF | Dividing factor (R) | Compare frequency | fvco(MHz) |
|---|---|---|---|
| 0 | 4 | 1 MHz | 1024 – 2150 MHz* |
| 1 | 8 | 500 KHz | 950 – 2150 MHz |

Caution: Only use REF=0

* When the reference division ratio set to 4(REF = '0'), the fvco's minimum frequency must be higher than 1024 MHz (including 1024 MHz). If the frequency is lower than 1023 MHz, the condition mentioned in section 6-2-1 "A < N" is not satisfied. But all receiving ranges can be covered with combination with PSC setting. (see Table 6)

Table 6; Prescaler division ratio setting (Binary: 1 bit)

| PSC | Dividing factor (P) | fvco |
|---|---|---|
| 0 | 32 | 950 – 2150 MHz |
| 1 | 16 | 950 – 1375 MHz* |

The dividing factor is set by PSC in byte 4 on $I^2C$ write data.

* When the prescaler division ratio of the prescaler is set to 16(PSC = '1'), the fvco's maximum frequency must be lower than 1375 MHz (including 1375 MHz). This fvco's maximum frequency limitation is depended on the operation frequency of the internal programmable counter. Refer to Table 9 about PSC detailed setting.

Table 7; Address selection (Binary: 2 bits)

| Bit | | ADR input voltage |
|---|---|---|
| MA1 | MA0 | |
| 0 | 0 | 0V ～ 0.1VCC |
| 0 | 1 | open |
| 1 | 0 | 0.4VCC ～ 0.6VCC |
| 1 | 1 | 0.9VCC ～ VCC |

Table 8; PO control (Binary: 1 bit)

| Bit | Output of PO | | |
|---|---|---|---|
| PD0 | Normal | Power on | Power on |
| 1 | L | Hi-Z | Hi-Z |
| 0 | Hi-Z | Hi-Z | |

* Hi-Z : High impedance

Table 9; Local oscillator select (Binary: 4 bits)

| BAND | Byte 4 | | Byte 5 | | | | | Local frequency (Receiving frequency) |
|---|---|---|---|---|---|---|---|---|
| | PSC | PSC div.ratio | DIV | BA2 | BA1 | BA0 | VCO div.ratio | |
| 1 | 1 | 1/16 | 1 | 1 | 0 | 1 | 1/4 | 950 ~ 986 MHz |
| 2 | 1 | 1/16 | 1 | 1 | 1 | 0 | 1/4 | 986 ~ 1073 MHz |
| 3 | 0 | 1/32 | 1 | 1 | 1 | 1 | 1/4 | 1073 ~ 1154 MHz |
| 4 | 0 | 1/32 | 0 | 0 | 0 | 1 | 1/2 | 1154 ~ 1291 MHz |
| 5 | 0 | 1/32 | 0 | 0 | 1 | 0 | 1/2 | 1291 ~ 1447 MHz |
| 6 | 0 | 1/32 | 0 | 0 | 1 | 1 | 1/2 | 1447 ~ 1615 MHz |
| 7 | 0 | 1/32 | 0 | 1 | 0 | 0 | 1/2 | 1615 ~ 1791 MHz |
| 8 | 0 | 1/32 | 0 | 1 | 0 | 1 | 1/2 | 1791 ~ 1972 MHz |
| 9 | 0 | 1/32 | 0 | 1 | 1 | 0 | 1/2 | 1972 ~ 2150 MHz |
| — | 0 | 1/32 | 0/1 | 0 | 0 | 0 | — | VCO disable |

Table 10; Baseband LPF cut-off frequency setting

| Register Bit | | | | LPF cut-off Frequency |
|---|---|---|---|---|
| PD2 | PD3 | PD4 | PD5 | |
| 0 | 0 | 1 | 1 | 10 MHz |
| 0 | 1 | 0 | 0 | 12 MHz |
| 0 | 1 | 0 | 1 | 14 MHz |
| 0 | 1 | 1 | 0 | 16 MHz |
| 0 | 1 | 1 | 1 | 18 MHz |
| 1 | 0 | 0 | 0 | 20 MHz |
| 1 | 0 | 0 | 1 | 22 MHz |
| 1 | 0 | 1 | 0 | 24 MHz |
| 1 | 0 | 1 | 1 | 26 MHz |
| 1 | 1 | 0 | 0 | 28 MHz |
| 1 | 1 | 0 | 1 | 30 MHz |
| 1 | 1 | 1 | 0 | 32 MHz |
| 1 | 1 | 1 | 1 | 34 MHz |

Table 11; Test mode setting

| Register Bit | | | | Test mode |
|---|---|---|---|---|
| RTS | TS2 | TS1 | TS0 | |
| 0 | X | X | X | Normal operation |
| 1 | | Don't use | | Reserved (Test Mode) |

X: don't care

* When RTS=1 on "$I^2C$ write data (table 1)", it changes to test mode.

Table 12; Charge pump output current selection

| Bit | | Charge pump output current [μA] | | |
|---|---|---|---|---|
| C1 | C0 | min | typ | max |
| 0 | 0 | ±78 | ±120 | ±150 |
| 0 | 1 | ±169 | ±260 | ±325 |
| 1 | 0 | ±360 | ±555 | ±694 |
| 1 | 1 | ±780 | ±1200 | ±1500 |

Table 13; Baseband AMP gain control (Depend on PLL register setting)

| BG1 | BG0 | ATTENUATION (Typ.) |
|---|---|---|
| 0 | 0/1 | 0 |
| 1 | 0 | –2 dB |
| 1 | 1 | –4 dB |

* Set BG1,BG0 as 1,0.

Table 14; POR bit polarity

| | VCC > 2.2V | VCC < 2.2V |
|---|---|---|
| POR bit | L | H |

* SDA has to be pulled up.

Table 15; FL bit polarity

| | lock | unlock |
|---|---|---|
| FL bit | H | L |

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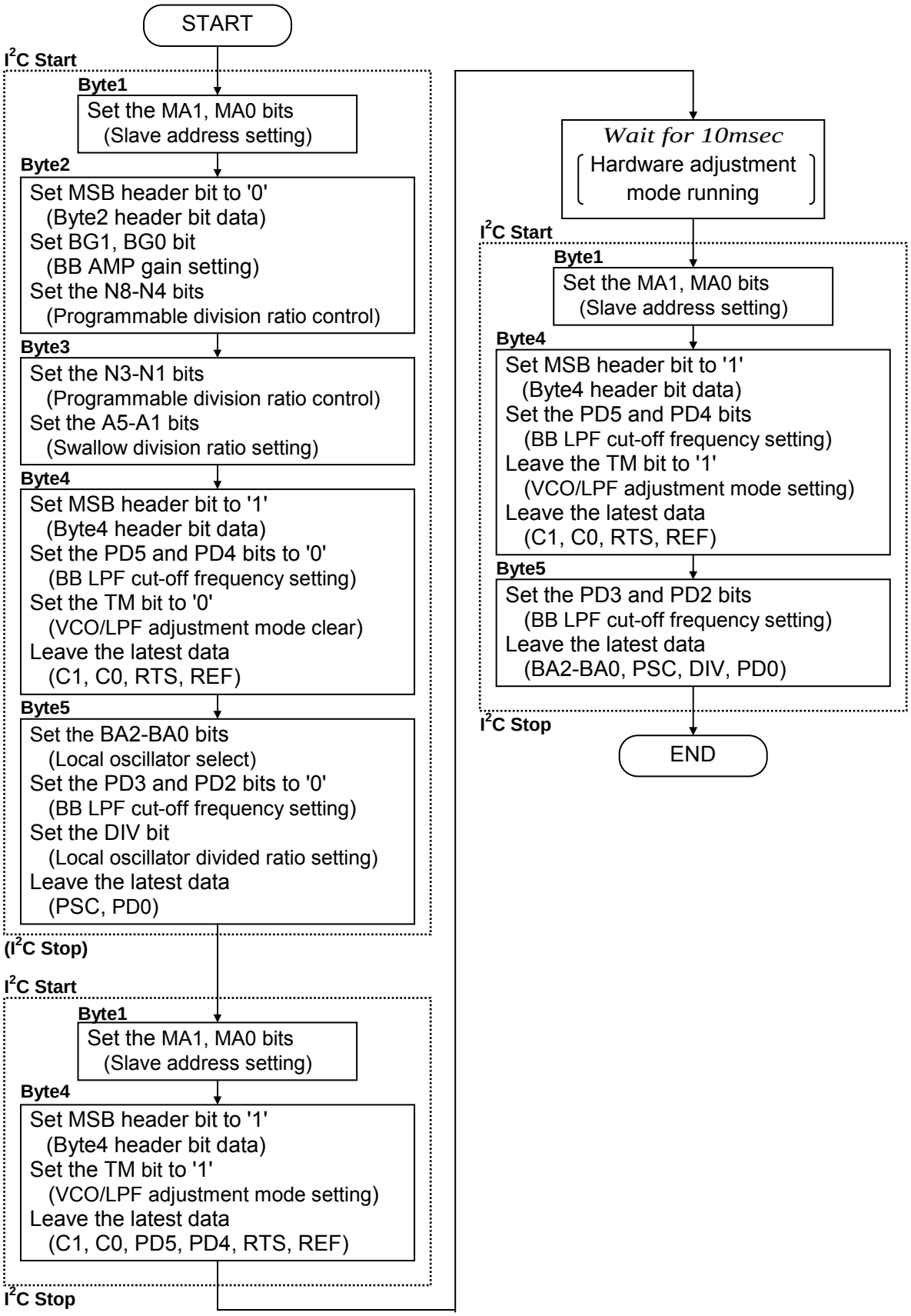
9-3. Tuner control procedure

VCO and LPF adjustment mode setting sequence after power on



[10] Reliability

10-1. High temperature high humidity load (40deg.C, 90% RH, 500h)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After cycling DUT in the constant chamber at 40deg.C/90-95% RH in on state, for total 500h, leave the DUT at room temperature and humidity for 2h and then measure value after test.
3) Must meet the specifications of Table 17.
4) The contact resistance of F-connector must be less than 0.02 ohm. (*)

10-2. High temperature load (70deg.C, 40% RH, 500h)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After leaving DUT in the constant chamber at 70+/-2deg.C/40% RH for total 500h, leave the DUT at room temperature and humidity for 2h and then measure value after test.
3) Must meet the specifications of Table 17.

10-3. Cold test (-25deg.C, 500h)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After leaving DUT in the constant temperature chamber at -25deg.C for 500h, leave the DUT at room temperature and humidity for 2h and then measure the values after test.
3) Must meet the specifications of Table 17.

10-4. Shock (686 $m/s^2$, 6 planes, 3 times)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial values.
2) Using the shock tester, apply shock of 686 $m/s^2$ three times to each of 6 planes and then measure the values.
3) Must meet the specifications of Table 17.
4) This test is to be conducted using a single tuner.

10-5. Vibration (10-55 Hz, 1.5 mm, in each of three mutually perpendicular directions, each 2 times)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial values.
2) Using the vibration tester, apply motion having an amplitude of 1.5 mm (constant), the frequency being varied uniformly between 10 and 55 Hz, to DUT, for 2h in each of three mutually perpendicular directions (X, Y and Z, total of 6h). After the test, measure the values.
3) Must meet the specifications of Table 17.
4) This test is to be conducted using a single tuner.

10-6. Heat shock test (1 cycle=1h (-20deg.C; 0.5h, 70deg.C;0.5h), 50 cycles))

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) Using the heat shock tester, apply heat shock to DUT. After the test, measure the values.
3) Must meet the specifications of Table 17.
4) The contact resistance of F-connector must be less than 0.02 ohm. (*)

10-7. Solderability of terminal

Pretreatment of heating terminal at 150deg.C for 1h is performed and leave it at room temperature for 2h or longer. Immerse 1.9 mm length of terminal (from the tip) to be soldered into rosin (JIS-K-5902), isopropyl alcohol (JIS-K-8839 or JIS-K-1522, rosin concentration (10-35% range) approx. 25% by weight unless otherwise specified) or equivalent solution for 3–5s, and then immerse the length of the terminal into a pool of molten solder (Sn/3.0Ag/0.5Cu, or equivalent) at 240 +/-2deg.C for 3s.Dipped terminal portion shall be wetted by more than 95%. (Excluding the cutting plane of the chassis)

10-8. Soldering heat resistance

Immerse the terminal mounted on a PCB (1.6t thick) into solder at 350±5deg.C for 3.0-3.5 seconds or at 260 +/-5deg.C for 10 +/-1 seconds. Remove the PCB from the solder and leave it for 1 hour at room temperature. The test sample shall show no degradation in appearance and electrical characteristics.

10-9. ESD protection

Table 16; ESD Test Condition (IEC61000-4-2 Compliant)

| Terminal | Limits | Condition |
|---|---|---|
| RF_IN (coaxial center) | +/-6kV DC | 150pF/330ohm each 5 times |
| Others | +/-200V DC | 150pF/330ohm each 5 times |

Table 17

| No. | Item | | Spec. | UNIT | Condition |
|---|---|---|---|---|---|
| 10-1 | Noise figure(at max. gain) | | < 12 | dB | 950MHz to 2150MHz |
| 10-2 | PLL phase noise | | < -70 | dBc/Hz | 10kHz offset |
| | | | < -86 | dBc/Hz | 100kHz offset |
| 10-3 | Current consumption | B2 | < 135 | mA | 3.3V |
| | | B3 | < 130 | mA | 3.3V |
| | | B4 | < 40 | mA | 3.3V |
| | | VDD | < 1800 | mA | 1.8V |
| 10-4 | Es/No at QEF | 8PSK 3/4 | < 8.2 | dB | DVB-S2, Pilot: ON |

(*)Method of measuring contact resistance

Center-contact

Insert the gauge pin(φ0.8mm) to F-connector.

Measure the resistance between the gauge and the center-contact of F-connector.

Outer-shell

Connect the plug(3/8-32 UNEF-2B) to F-connector at 29.4N・cm of the clamping torque.

Measure the resistance between the plug and chassis.

(Measuring device: Milliohm meter)

SHARP

[11] BLOCK DIAGRAM

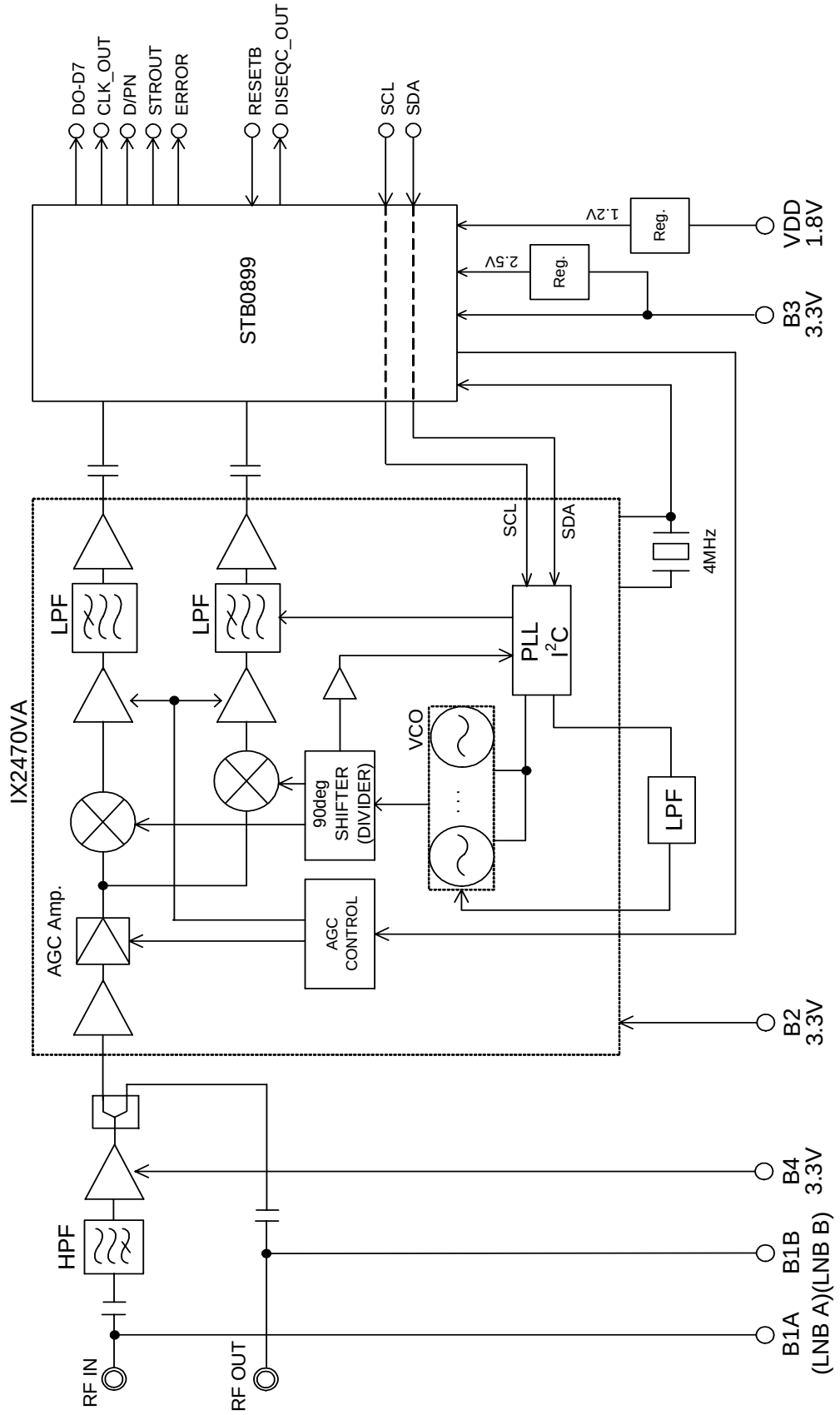



Fig 1. BLOCK DIAGRAM

SHARP

[12] PIN LIST

| No. | NAME | LOGIC | PIN DESCRIPTION |
|---|---|---|---|
| 1 | B1B | | Voltage supply of LNB B. Please ground it with a 1000pF ceramic capacitor. |
| 2 | B1A | | Voltage supply of LNB A. Please ground it with a 1000pF ceramic capacitor. |
| 3 | B4 | | 3.3V supply for RF Booster Amp of tuner. |
| 4 | B2 | | 3.3V supply for the Front-end section. Please keep a ripple at the Power Supply less than 10mVp-p. |
| 5,6,7,10 | NC | | It is not connected inside the unit. We advice to ground it. |
| 8 | SDA | 3.3V | $I^2C$ Bus. Please connect a pull-up resistor which is more than 2k ohm outside of the tuner. |
| 9 | SCL | 3.3V | |
| 11 | B3 | | 3.3V supply for demodulator IC. It is internally converted into 2.5V. |
| 12 | DISEQC_ OUT | 3.3V | Digital satellite equipment control output. |
| 13 | VDD | | 1.8V digital core supply. It is internally converted into 1.2V. |
| 14,...,21 | D0,...,D7 | 3.3V | Transport stream parallel data. |
| 22 | CLK_OUT | 3.3V | Transport stream byte or bit clock. |
| 23 | D/PN | 3.3V | Transport stream data valid signal. |
| 24 | STROUT | 3.3V | Transport stream sync bit. |
| 25 | ERROR | 3.3V | Transport stream packet error signal. |
| 26 | RESETB | 3.3V | Reset signal active low. |

[13] CONECTION DIAGRAM

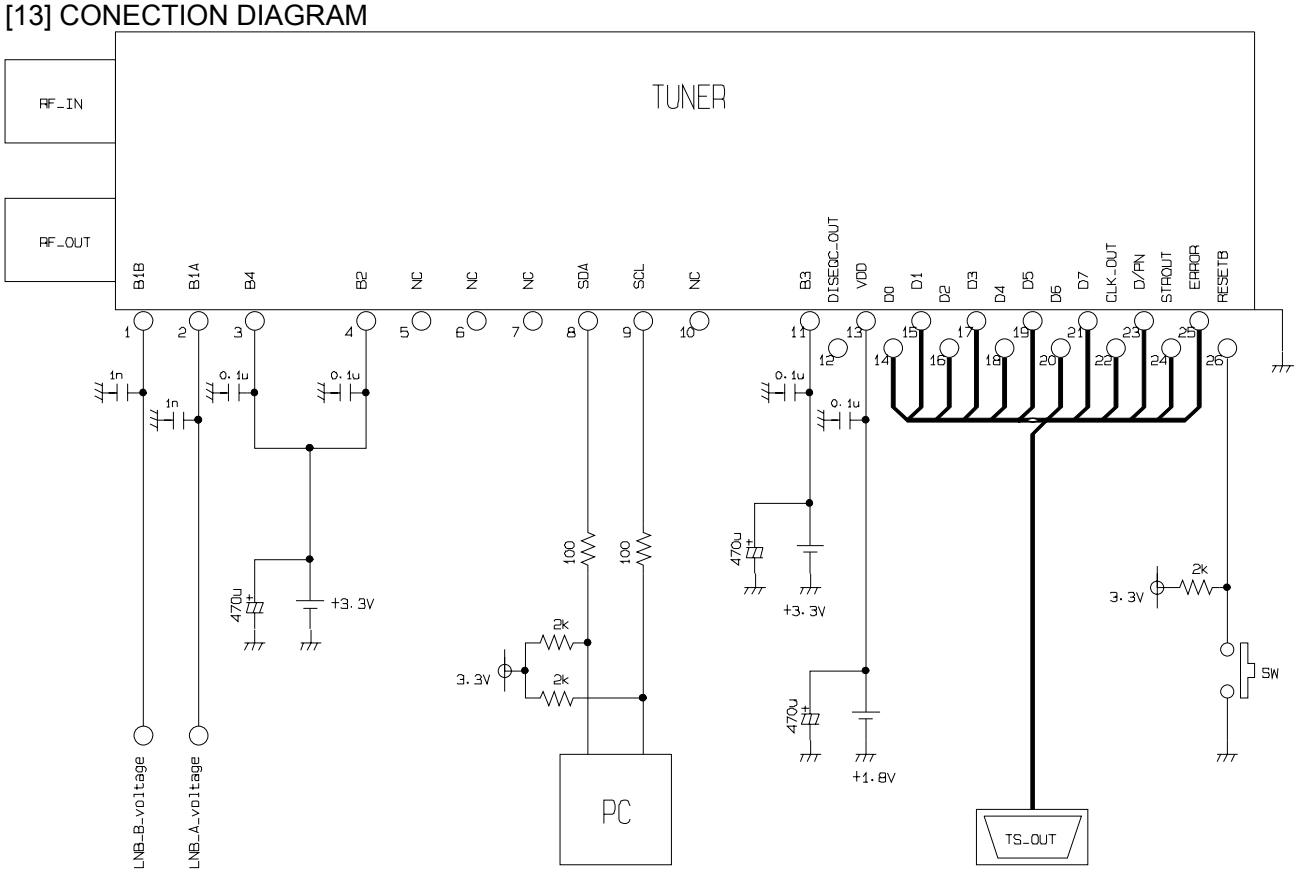



Fig 2. CONNECTION DIAGRAM

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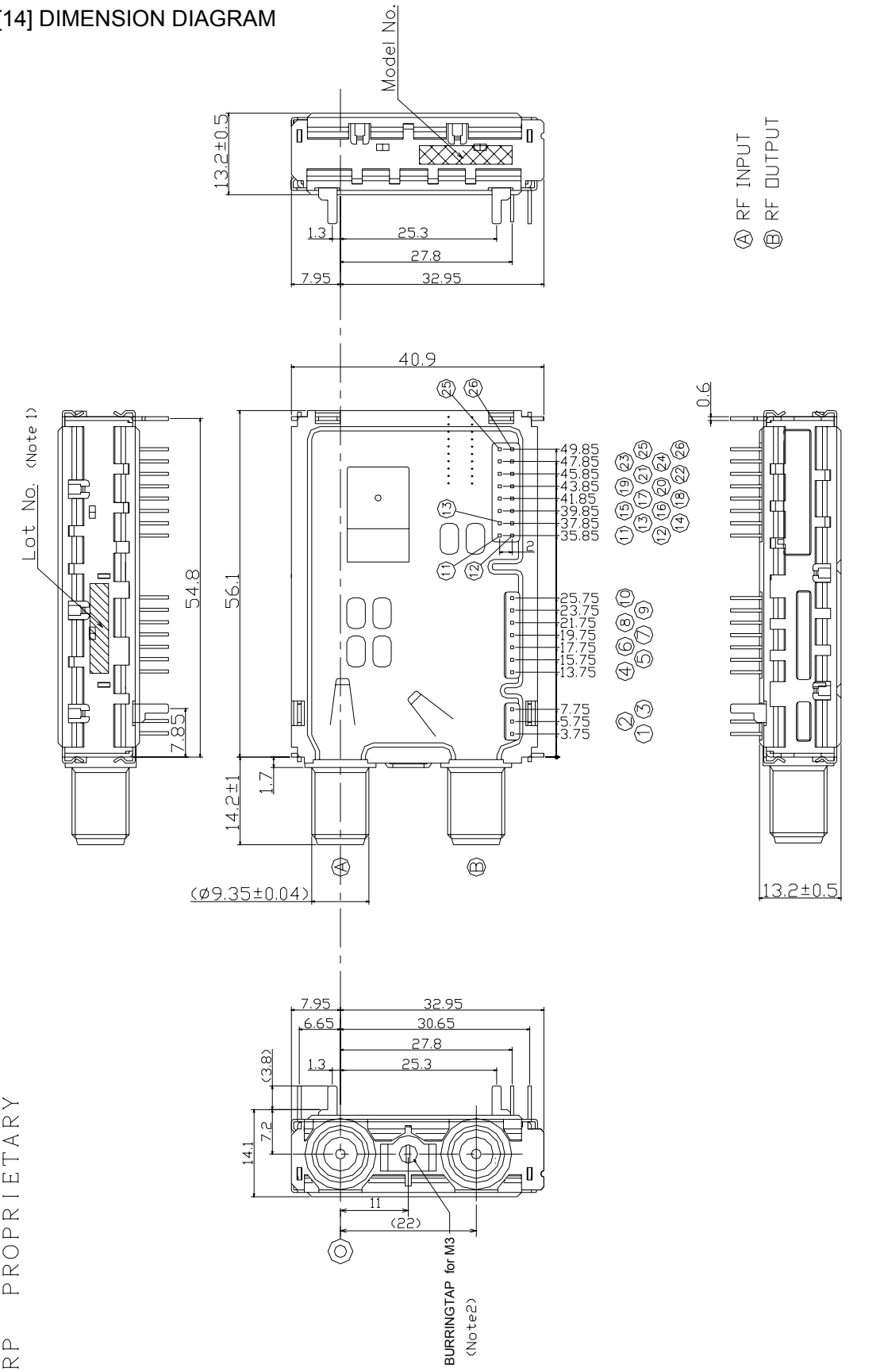
## [14] DIMENSION DIAGRAM




SHARP PROPRIETARY

Note1 : The first letter of lot number "W" means made in China.
This tuner is made in China.

Note2 : The length of screw(inside of tuner) should be less than 2mm.

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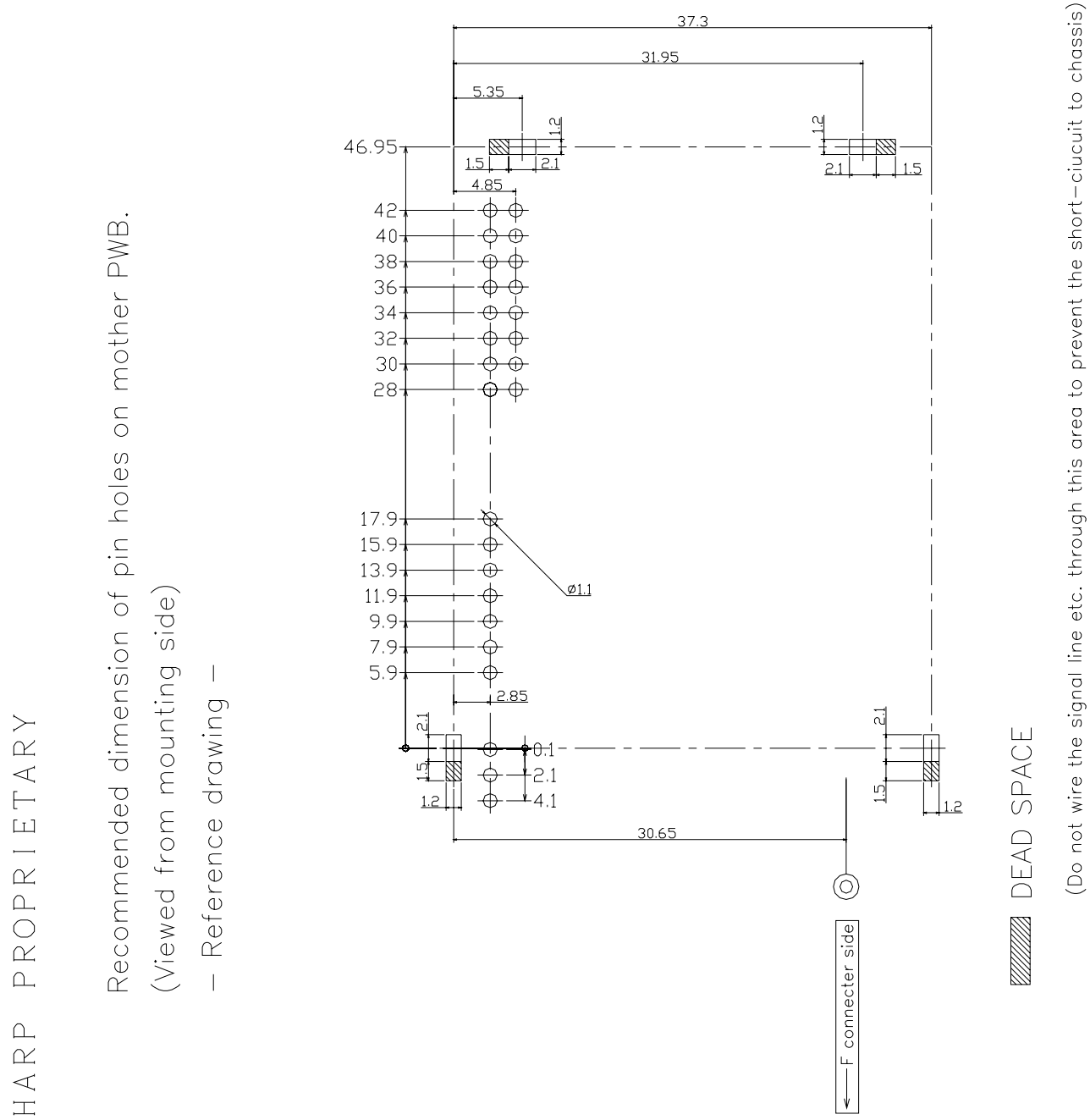
[15] MOUNTING DATALIS

Unit : mm

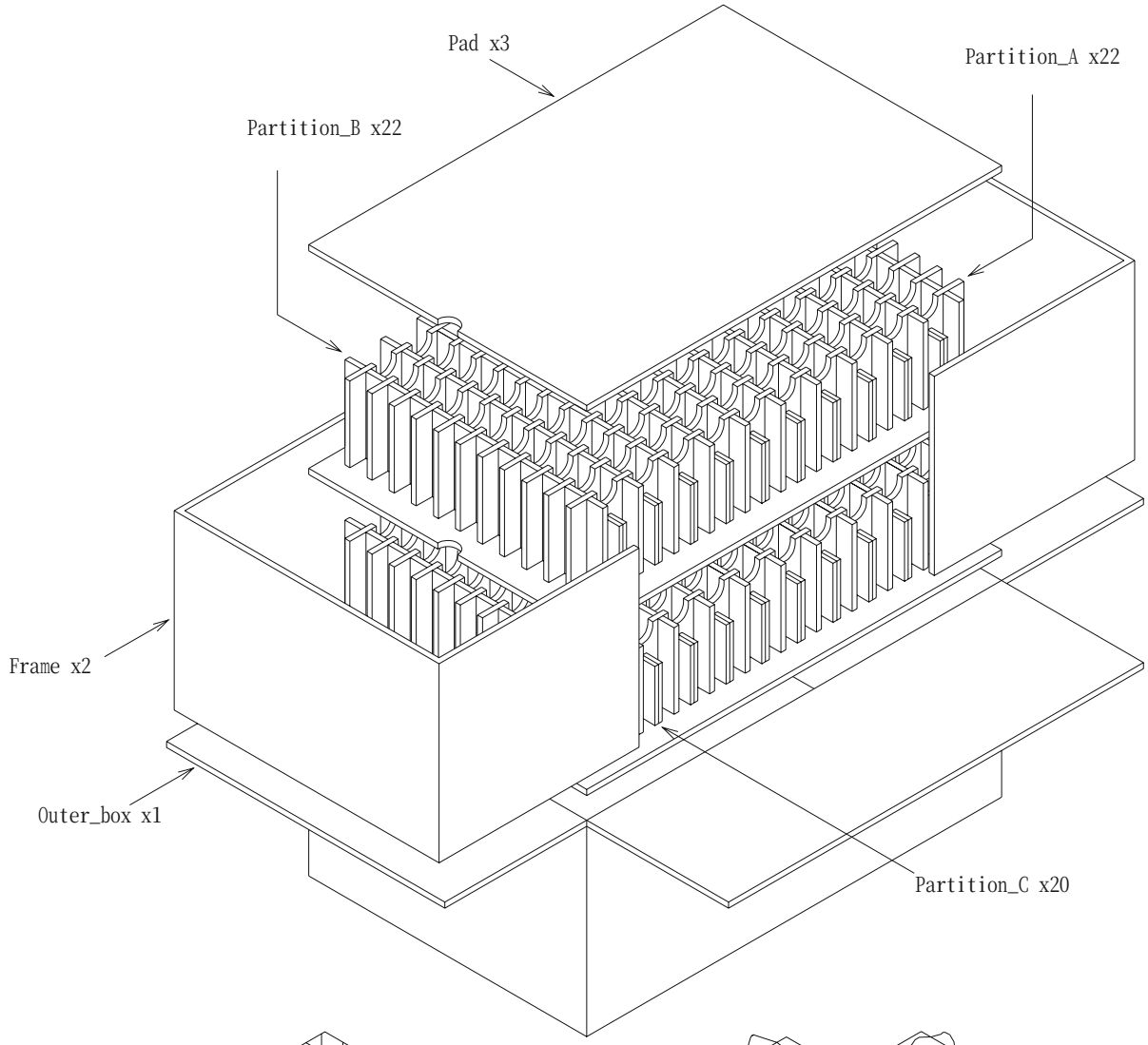


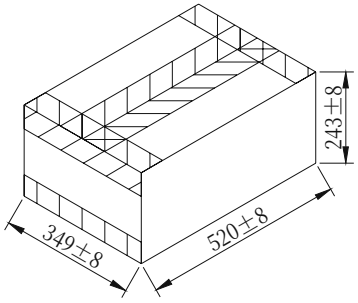

Recommended dimension of pin holes on mother PWB.
(Viewed from mounting side)
— Reference drawing —

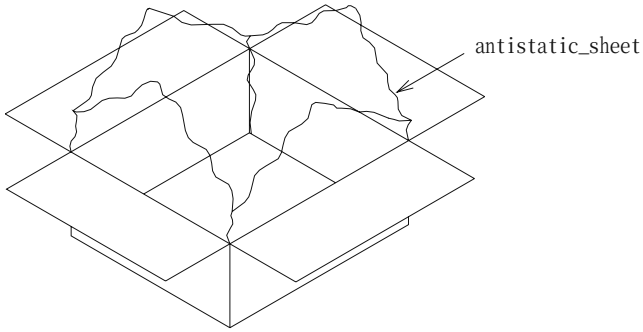
SHARP PROPRIETARY

SHARP

[16] PACKAGEING DATAILS




UNIT :mm
QUANTITY :200pcs