Very Low Power/Voltage CMOS SRAM
128K X 16 bit

BS616LV2018

■ FEATURES

- Very low operation voltage : 2.4 ~ 3.6V
- Very low power consumption :
  Vcc = 3.0V C-grade: 16mA (Max.) operating current
  I -grade: 20mA (Max.) operating current
  0.1uA (Typ.) CMOS standby current
- High speed access time :
  -70 70ns (Max.) at Vcc = 3.0V
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ options
- I/O Configuration x8/x16 selectable by $\overline{\text{LB}}$ and $\overline{\text{UB}}$ pin

■ DESCRIPTION

The BS616LV2018 is a high performance, very low power CMOS Static Random Access Memory organized as 131,072 words by 16 bits and operates from a wide range of 2.4V to 3.6V supply voltage.
Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.1uA and maximum access time of 70ns in 3V operation.
Easy memory expansion is provided by active LOW chip enable($\overline{\text{CE}}$), active LOW output enable($\overline{\text{OE}}$) and three-state output drivers.
The BS616LV2018 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.
The BS616LV2018 is available in DICE form, JEDEC standard 48-pin TSOP Type I package and 48-ball BGA package.

■ PRODUCT FAMILY

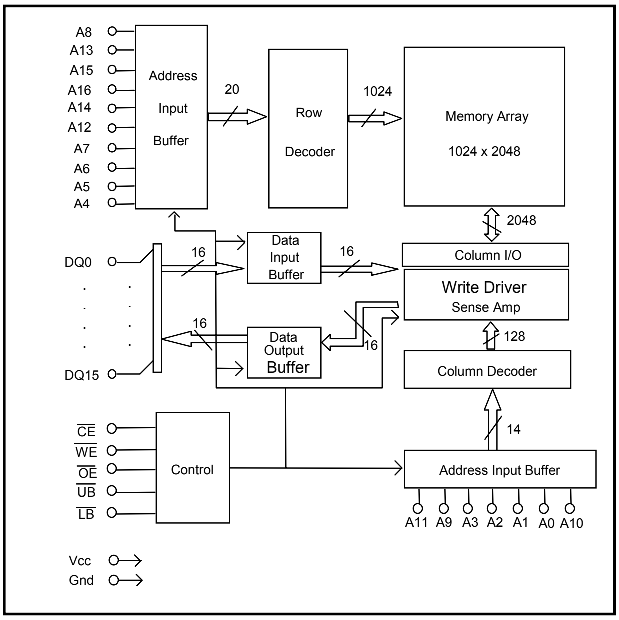
PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED (ns)	POWER DISSIPATION		PKG TYPE
				STANDBY (ICCSB1, Max)	Operating (ICC, Max)	
			Vcc= 3.0V	Vcc=3.0V	Vcc=3.0V	
BS616LV2018DC	0 °C to +70 °C	2.4V ~3.6V	70	0.7 uA	16 mA	DICE
BS616LV2018TC						TSOP1-48
BS616LV2018AC						BGA-48-0608
BS616LV2018DI	-40 °C to +85 °C		70	1.5 uA	20 mA	DICE
BS616LV2018TI						TSOP1-48
BS616LV2018AI						BGA-48-0608

■ PIN CONFIGURATIONS

	1	2	3	4	5	6
A	$\overline{\text{LB}}$	$\overline{\text{OE}}$	A0	A1	A2	N.C.
B	D8	$\overline{\text{UB}}$	A3	A4	$\overline{\text{CE}}$	D0
C	D9	D10	A5	A6	D1	D2
D	VSS	D11	N.C.	A7	D3	VCC
E	VCC	D12	N.C.	A16	D4	VSS
F	D14	D13	A14	A15	D5	D6
G	D15	N.C.	A12	A13	$\overline{\text{WE}}$	D7
H	N.C.	A8	A9	A10	A11	N.C.

48-ball BGA top view

■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Function
A0-A16 Address Input	These 17 address inputs select one of the 131,072 x 16-bit words in the RAM.
$\overline{CE}$ Chip Enable Input	$\overline{CE}$ is active LOW. Chip enables must be active when data read from or write to the device. if chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
$\overline{LB}$ and $\overline{UB}$ Data Byte Control Input	Lower byte and upper byte data input/output control pins.
DQ0 - DQ15 Data Input/Output Ports	These 16 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
Gnd	Ground

■ TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	DQ0~DQ7	DQ8~DQ15	Vcc CURRENT
Not selected (Power Down)	H	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	L	L	L	Dout	Dout	I_{CC}
				H	L	High Z	Dout	I_{CC}
				L	H	Dout	High Z	I_{CC}
Write	L	L	X	L	L	Din	Din	I_{CC}
				H	L	X	Din	I_{CC}
				L	H	Din	X	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0 °C to +70 °C	2.4V ~ 3.6V
Industrial	-40 °C to +85 °C	2.4V ~ 3.6V

■ CAPACITANCE (1) (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

1. This parameter is guaranteed and not tested.

■ DC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN.	TYP. (1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		Vcc=3.0V	-0.5	--	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		Vcc=3.0V	2.0	--	Vcc+0.2	V
I_{IL}	Input Leakage Current	Vcc = Max, V_{IN} = 0V to Vcc		--	--	1	uA
I_{OL}	Output Leakage Current	Vcc = Max, $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to Vcc		--	--	1	uA
V_{OL}	Output Low Voltage	Vcc = Max, I_{OL} = 2mA	Vcc=3.0V	--	--	0.4	V
V_{OH}	Output High Voltage	Vcc = Min, I_{OH} = -1mA	Vcc=3.0V	2.4	--	--	V
I_{CC}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, I_{DQ} = 0mA, F = Fmax(3)	Vcc=3.0V	--	--	16	mA
I_{CCSB}	Standby Current-TTL	$\overline{CE}$ = V_{IH}, I_{DQ} = 0mA	Vcc=3.0V	--	--	1	mA
I_{CCSB1}	Standby Current-CMOS	$\overline{CE} \geq$ Vcc-0.2V, $V_{IN} \geq$ Vcc - 0.2V or $V_{IN} \leq$ 0.2V	Vcc=3.0V	--	0.1	0.7	uA

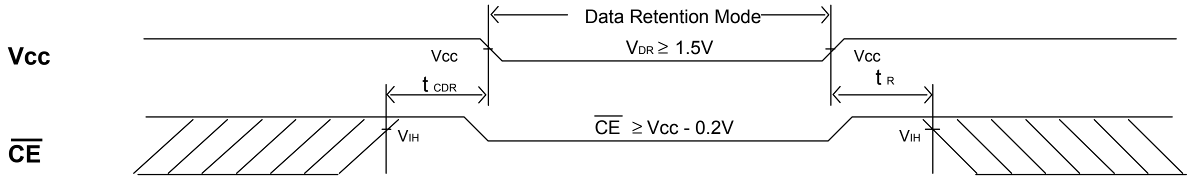
1. Typical characteristics are at TA = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
3. Fmax = $1/t_{RC}$.

■ DATA RETENTION CHARACTERISTICS (TA = 0 to + 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V_{DR}	Vcc for Data Retention	$\overline{CE} \geq$ Vcc - 0.2V $V_{IN} \geq$ Vcc - 0.2V or $V_{IN} \leq$ 0.2V	1.5	--	--	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq$ Vcc - 0.2V $V_{IN} \geq$ Vcc - 0.2V or $V_{IN} \leq$ 0.2V	--	0.05	0.5	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		T_{RC} (2)	--	--	ns

1. Vcc = 1.5V, T_A = + 25°C
2. t_{RC} = Read Cycle Time

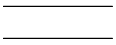
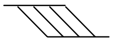
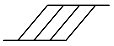
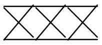
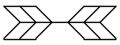
■ LOW V_{CC} DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



■ AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5Vcc

■ KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

■ AC TEST LOADS AND WAVEFORMS

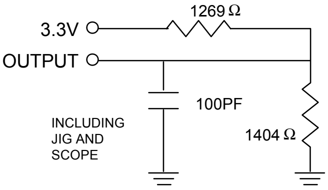


FIGURE 1A

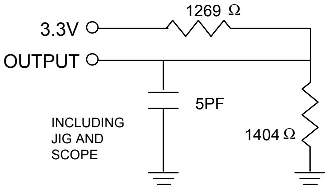
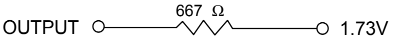


FIGURE 1B

THEVENIN EQUIVALENT



ALL INPUT PULSES

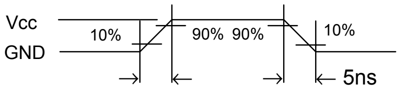


FIGURE 2

■ AC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C , Vcc = 3.0V)

READ CYCLE

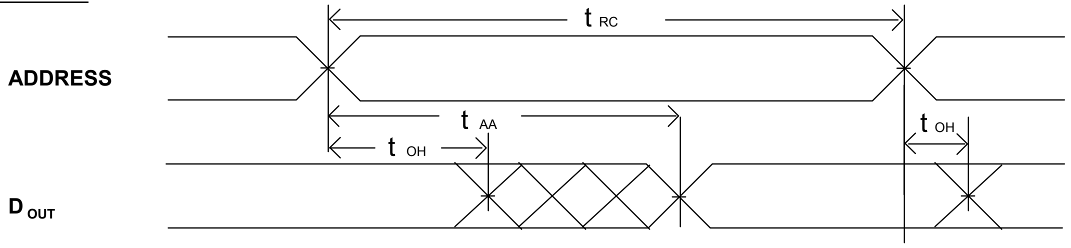
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616LV2018-70 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	70	--	--	ns
t_{AVQV}	t_{AA}	Address Access Time	--	--	70	ns
t_{ELQV}	t_{ACS}	Chip Select Access Time ($\overline{CE}$)	--	--	70	ns
t_{BA}	t_{BA}(1)	Data Byte Control Access Time ($\overline{LB}$,$\overline{UB}$)	--	--	35	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	35	ns
t_{E1LQX}	t_{CLZ}	Chip Select to Output Low Z ($\overline{CE}$)	10	--	--	ns
t_{BE}	t_{BE}	Data Byte Control to Output Low Z ($\overline{LB}$,$\overline{UB}$)	10	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	10	--	--	ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z ($\overline{CE}$)	0	--	35	ns
t_{BDO}	t_{BDO}	Data Byte Control to Output High Z ($\overline{LB}$,$\overline{UB}$)	0	--	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	--	30	ns
t_{AXOX}	t_{OH}	Output Disable to Address Change	10	--	--	ns

NOTE :

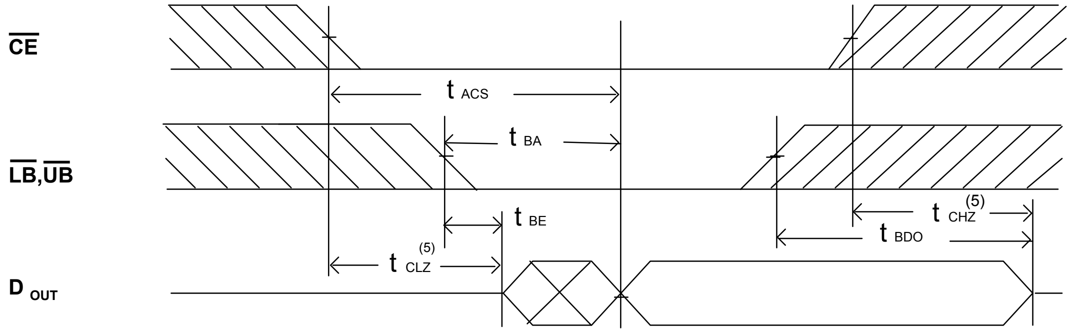
1. t_{BA} is 35ns (@speed=70ns) with address toggle. ; .t_{BA} is 70ns (@speed=70ns) without address toggle.

■ SWITCHING WAVEFORMS (READ CYCLE)

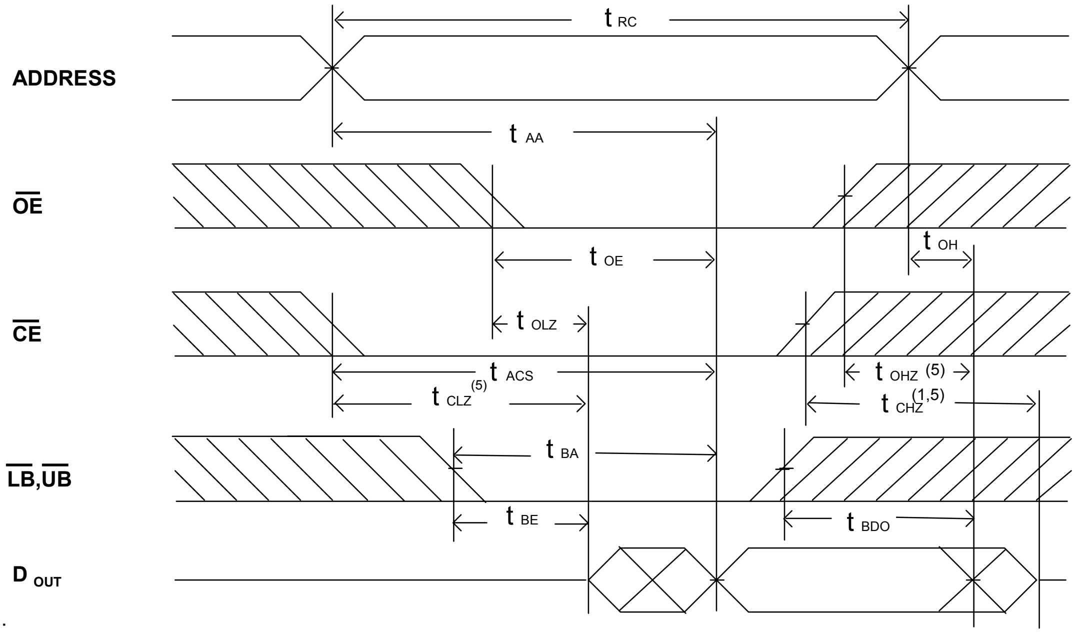
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:

1. $\overline{\text{WE}}$ is high for read Cycle.
2. Device is continuously selected when $\overline{\text{CE}} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{\text{CE}}$ transition low.
4. $\overline{\text{OE}} = V_{IL}$.
5. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1B.
   The parameter is guaranteed but not 100% tested.

■ AC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70ºC , Vcc = 3.0V)

WRITE CYCLE

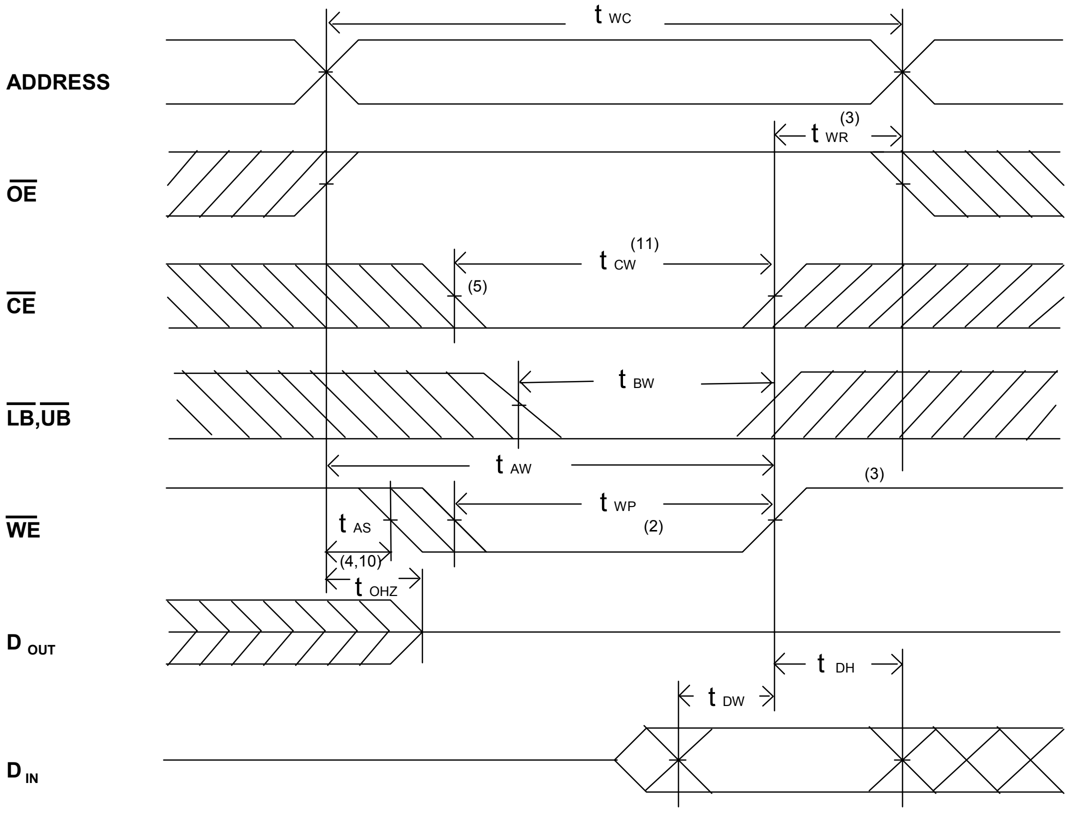
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616LV2018-70			UNIT
			MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	70	--	--	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	70	--	--	ns
t_{AVWL}	t_{AS}	Address Setup Time	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	70	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	35	--	--	ns
t_{WHAX}	t_{WR}	Write recovery Time $(\overline{CE},\overline{WE})$	0	--	--	ns
t_{BW}	$t_{BW}^{(1)}$	Date Byte Control to End of Write $(\overline{LB},\overline{UB})$	30	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	--	30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	30	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	--	30	ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5	--	--	ns

NOTE :

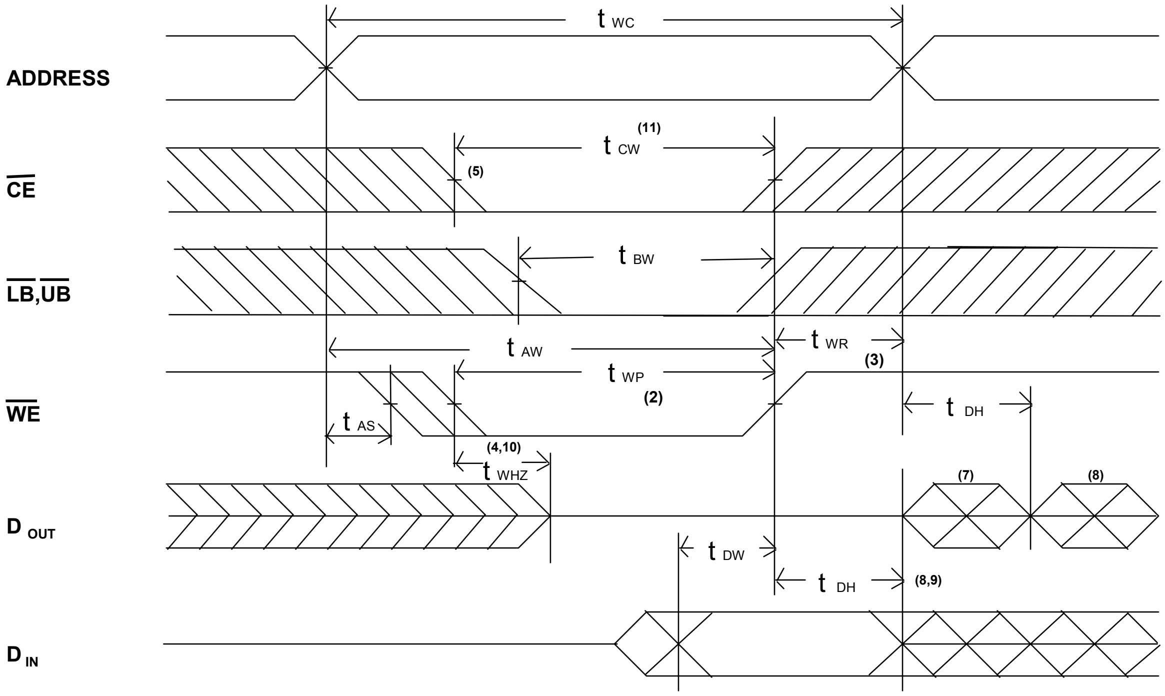
1. t_{BW} is 30ns (@speed=70ns) with address toggle. ; t_{BW} is 70ns (@speed=70ns) without address toggle.

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (1)



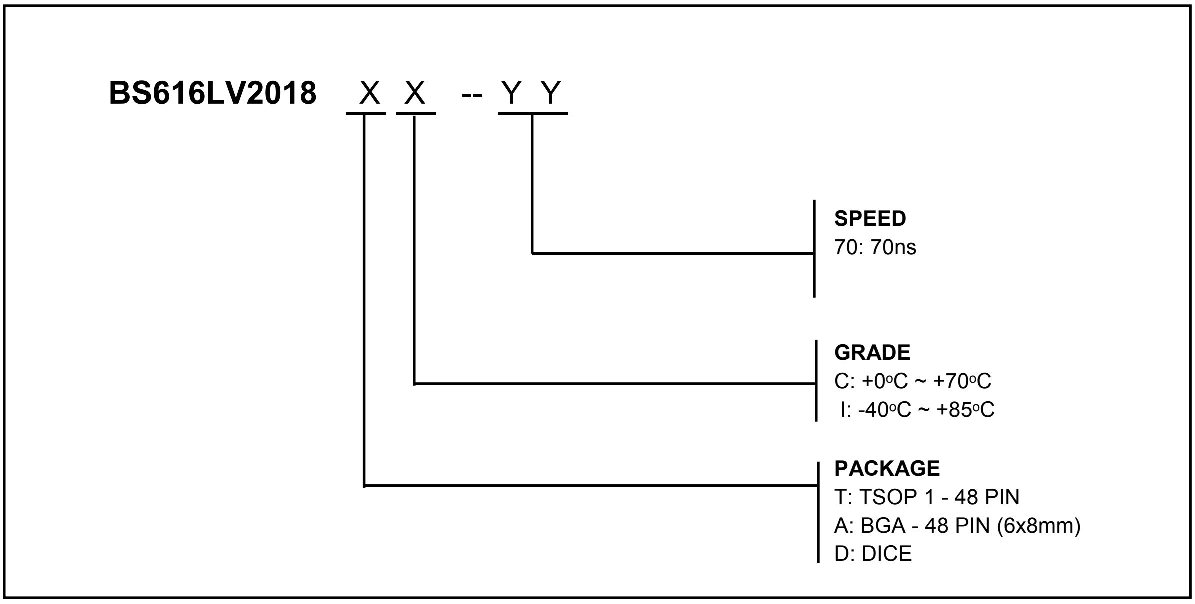
WRITE CYCLE2 (1,6)



NOTES:

1. $\overline{\text{WE}}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ and $\overline{\text{WE}}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{\text{CE}}$ low transition occurs simultaneously with the $\overline{\text{WE}}$ low transitions or after the $\overline{\text{WE}}$ transition, output remain in a high impedance state.
6. $\overline{\text{OE}}$ is continuously low ($\overline{\text{OE}} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{\text{CE}}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of $\overline{\text{CE}}$ going low to the end of write.

■ ORDERING INFORMATION



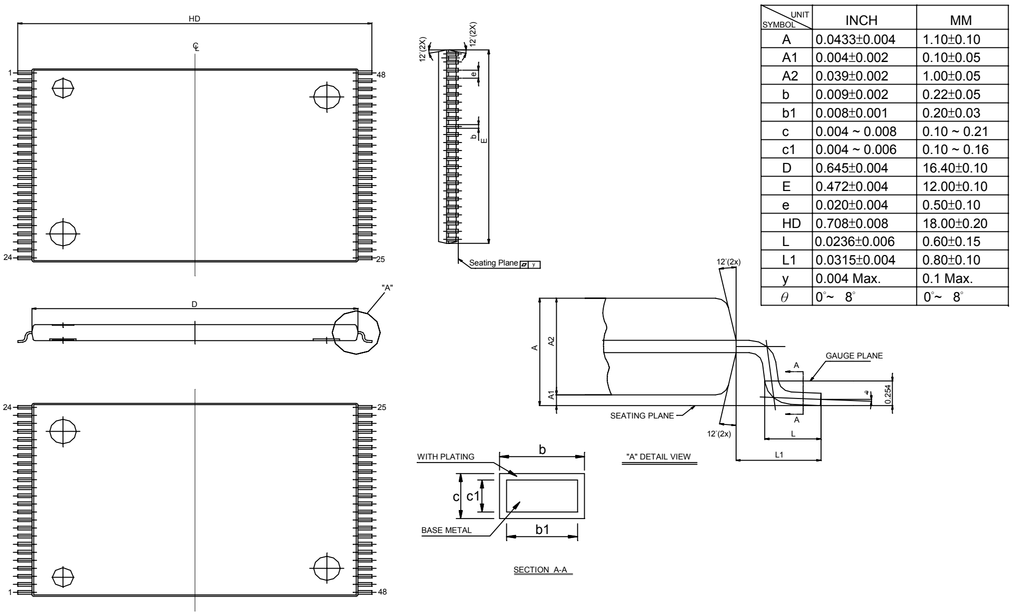
BS616LV2018 X X -- Y Y

SPEED
70: 70ns

GRADE
C: +0°C ~ +70°C
I: -40°C ~ +85°C

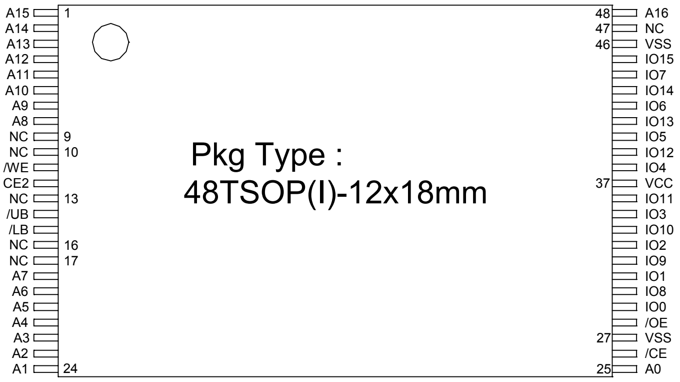
PACKAGE
T: TSOP 1 - 48 PIN
A: BGA - 48 PIN (6x8mm)
D: DICE

■ PACKAGE DIMENSIONS

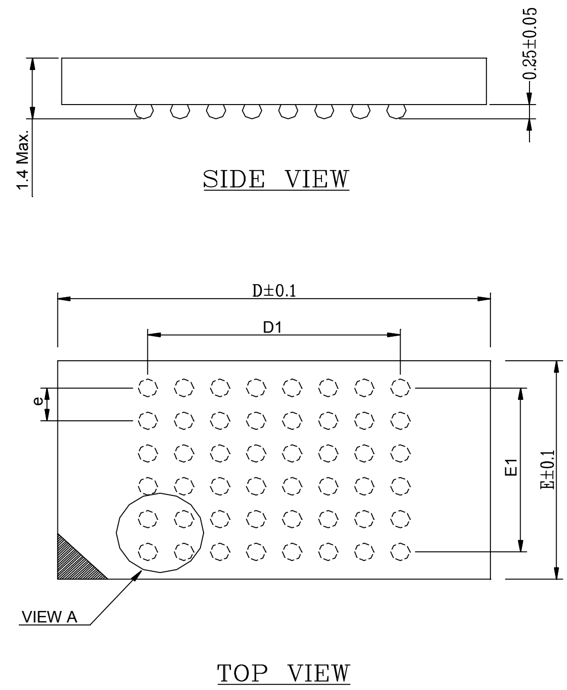


SYMBOL \ UNIT	INCH	MM
A	0.0433±0.004	1.10±0.10
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.009±0.002	0.22±0.05
b1	0.008±0.001	0.20±0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.645±0.004	16.40±0.10
E	0.472±0.004	12.00±0.10
e	0.020±0.004	0.50±0.10
HD	0.708±0.008	18.00±0.20
L	0.0236±0.006	0.60±0.15
L1	0.0315±0.004	0.80±0.10
y	0.004 Max.	0.1 Max.
θ	0°~ 8°	0°~ 8°

TSOP1-48PIN



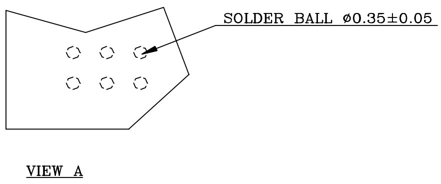
■ PACKAGE DIMENSIONS (continued)



48 mini-BGA (6 x 8)

NOTES:
1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

BALL PITCH e = 0.75				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75



REVISION HISTORY

Revision	Description	Date	Note
1.0	**Data Sheet release**	**Jan. 30, 2001**	
2.0	**Modify some AC parameters**	**April,12,2002**	