BSI

Very Low Power/Voltage CMOS SRAM
512K X 16 bit

BS616LV8011

■ FEATURES

- Very low operation voltage : 2.7 ~ 3.6V
- Very low power consumption :
  - Vcc = 3.0V C-grade: 40mA (Max.) operating current
  - I-grade : 50mA (Max.) operating current
  - 1uA (Typ.) CMOS standby current
- High speed access time :
  - -70 70ns (Max.) at Vcc=3.0V
  - -10 100ns (Max.) at Vcc=3.0V
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with $\overline{\text{CE1}}$,CE2 and $\overline{\text{OE}}$ options

■ DESCRIPTION

The BS616LV8011 is a high performance, very low power CMOS Static Random Access Memory organized as 524,288 words by 16 bits and operates from a wide range of 2.7V to 3.6V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 1uA and maximum access time of 70/100ns in 3V operation.

Easy memory expansion is provided by an active LOW chip enable($\overline{\text{CE1}}$,CE2) and active LOW output enable($\overline{\text{OE}}$) and three-state output drivers.

The BS616LV8011 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

The BS616LV8011 is available in 48-pin BGA package.

■ PRODUCT FAMILY

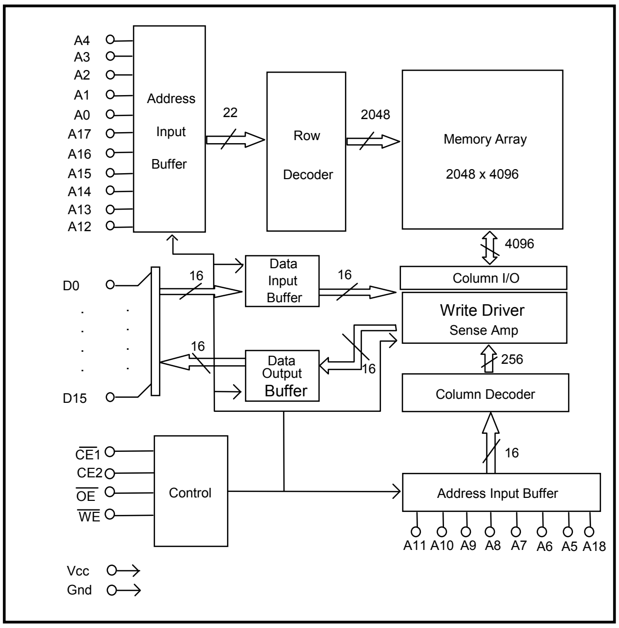
PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED (ns)	POWER DISSIPATION		PKG TYPE
				STANDBY (ICCSB1, Max)	Operating (ICC, Max)	
			Vcc=3.0V	Vcc=3.0V	Vcc=3.0V	
BS616LV8011AC	+0°C to +70°C	2.7V ~ 3.6V	70 / 100	16uA	40mA	BGA-48-0608
BS616LV8011AI	-40°C to +85°C	2.7V ~ 3.6V	70 / 100	24uA	50mA	BGA-48-0608

■ PIN CONFIGURATIONS

	1	2	3	4	5	6
A	X	$\overline{\text{OE}}$	A0	A1	A2	CE2
B	D8	X	A3	A4	$\overline{\text{CE1}}$	D0
C	D9	D10	A5	A6	D1	D2
D	VSS	D11	A17	A7	D3	VCC
E	VCC	D12	Vss	A16	D4	VSS
F	D14	D13	A14	A15	D5	D6
G	D15	NC	A12	A13	$\overline{\text{WE}}$	D7
H	A18	A8	A9	A10	A11	NC

48-Ball CSP top View X: Don't care

■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Function
A0-A18 Address Input	These 19 address inputs select one of the 524,288 x 16-bit words in the RAM.
$\overline{\text{CE1}}$ Chip Enable 1 Input **CE2 Chip Enable 2 Input**	$\overline{\text{CE1}}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{\text{WE}}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when WE is HIGH and $\overline{\text{OE}}$ is LOW, output data will be present on the DQ pins; when $\overline{\text{WE}}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{\text{OE}}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{\text{OE}}$ is inactive.
D0 - D15 Data Input/Output Ports	These 16 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
Gnd	Ground

■ TRUTH TABLE

MODE	$\overline{\text{CE1}}$	CE2	$\overline{\text{WE}}$	$\overline{\text{OE}}$	D0~D7	D8~D15	Vcc CURRENT
Not selected (Power Down)	H	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
	X	L	X	X			
Output Disabled	L	H	H	H	High Z	High Z	I_{CC}
Read	L	H	H	L	Dout	Dout	I_{CC}
Write	L	H	L	X	Din	Din	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to +70°C	2.7V ~ 3.6V
Industrial	-40°C to +85°C	2.7V ~ 3.6V

■ CAPACITANCE [1] (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	10	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	12	pF

1. This parameter is guaranteed and not tested.

■ DC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70ºC)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN.	TYP. (1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		Vcc=3V	-0.5	--	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		Vcc=3V	2.0	--	Vcc+0.2	V
I_{IL}	Input Leakage Current	Vcc = Max, V_{IN} = 0V to Vcc		--	--	1	uA
I_{OL}	Output Leakage Current	Vcc = Max, $\overline{CE1}$ = V_{IH}, or CE2 = V_{IL}, or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to Vcc		--	--	1	uA
V_{OL}	Output Low Voltage	Vcc = Max, I_{OL} = 2mA	Vcc=3V	--	--	0.4	V
V_{OH}	Output High Voltage	Vcc = Min, I_{OH} = -1mA	Vcc=3V	2.4	--	--	V
I_{CC}	Operating Power Supply Current	Vcc=max, $\overline{CE1}$=V_{IL} and CE2= V_{IH}, I_{DQ} = 0mA, F = Fmax(3)	Vcc=3V	--	--	40	mA
I_{CCSB}	Standby Current-TTL	Vcc= max, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, I_{DQ} = 0mA	Vcc=3V	--	--	1	mA
I_{CCSB1}	Standby Current-CMOS	Vcc= max,$\overline{CE1}$≧Vcc-0.2V, or CE2 ≦0.2V, V_{IN}≧Vcc-0.2V or V_{IN}≦0.2V	Vcc=3V	--	1	16	uA

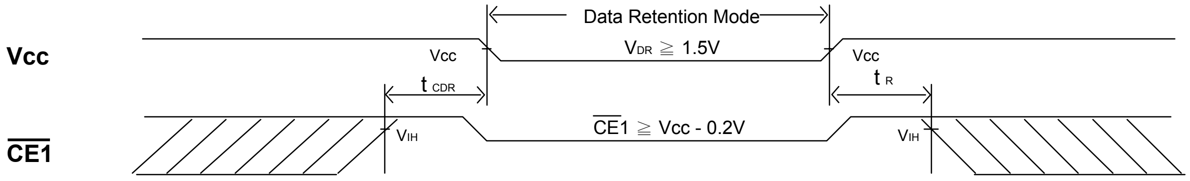
1. Typical characteristics are at TA = 25ºC.
2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
3. Fmax = $1/t_{RC}$.

■ DATA RETENTION CHARACTERISTICS (TA = 0 to + 70ºC)

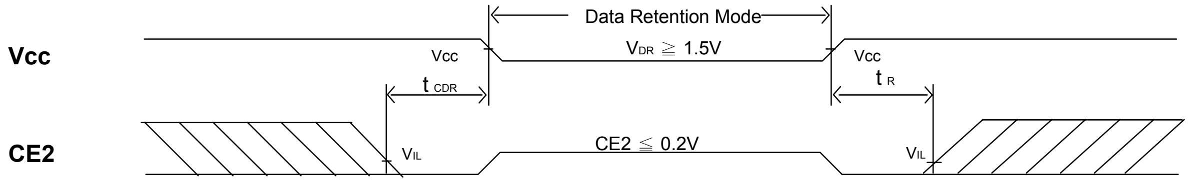
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V_{DR}	Vcc for Data Retention	$\overline{CE1}$ ≧ Vcc - 0.2V or CE2 ≦ 0.2V or V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	1.5	--	--	V
I_{CCDR}	Data Retention Current	$\overline{CE1}$ ≧ Vcc - 0.2V or CE2 ≦ 0.2V V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	--	0.8	12	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		T_{RC} (2)	--	--	ns

1. Vcc = 1.5V, T_A = + 25ºC
2. t_{RC} = Read Cycle Time

■ LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)



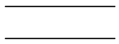
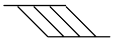
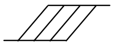
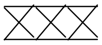
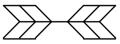
■ LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)



■ AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5Vcc

■ KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF "STATE

■ AC TEST LOADS AND WAVEFORMS

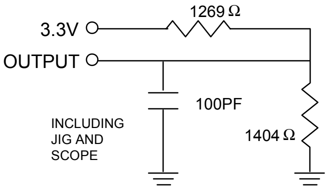


FIGURE 1A

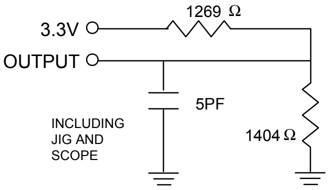
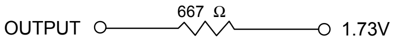


FIGURE 1B

THEVENIN EQUIVALENT



ALL INPUT PULSES

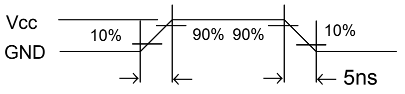


FIGURE 2

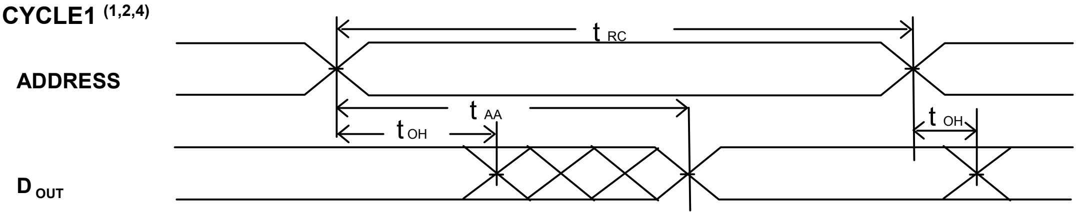
■ AC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C, Vcc=3V)

READ CYCLE

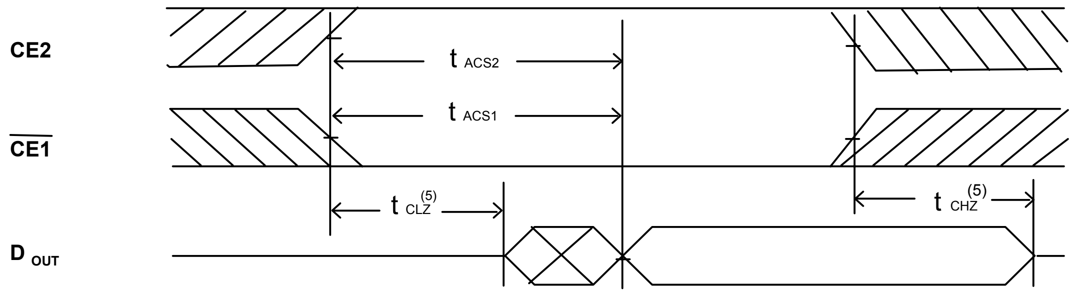
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616LV8011-70 MIN.	TYP.	MAX.	BS616LV8011-10 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	70	--	--	100	--	--	ns
t_{AVQV}	t_{AA}	Address Access Time	--	--	70	--	--	100	ns
t_{ELQV1}	t_{ACS1}	Chip Select Access Time ($\overline{CE1}$)	--	--	70	--	--	100	ns
t_{ELQV2}	t_{ACS2}	Chip Select Access Time (CE2)	--	--	70	--	--	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	35	--	--	50	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z (CE2,$\overline{CE1}$)	10	--	--	15	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	10	--	--	15	--	--	ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z(CE2,$\overline{CE1}$)	0	--	40	0	--	45	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	--	35	0	--	40	ns
t_{AXOX}	t_{OH}	Output Disable to Address Change	10	--	--	15	--	--	ns

SWITCHING WAVEFORMS (READ CYCLE)

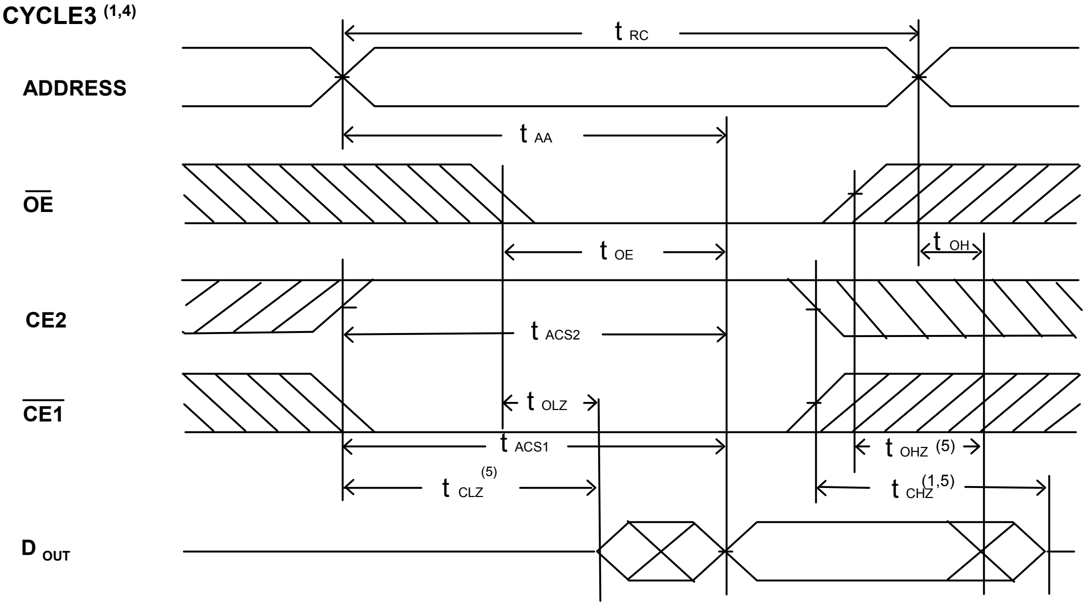
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:
1. $\overline{\text{WE}}$ is high in read Cycle.
2. Device is continuously selected when $\overline{\text{CE1}}$ = V_{IL} and CE2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{\text{CE1}}$ transition low and CE2 transition high.
4. $\overline{\text{OE}}$ = V_{IL} .
5. Transition is measured ± 500mV from steady state with CL = 30pF as shown in Figure 1B.
   The parameter is guaranteed but not 100% tested.

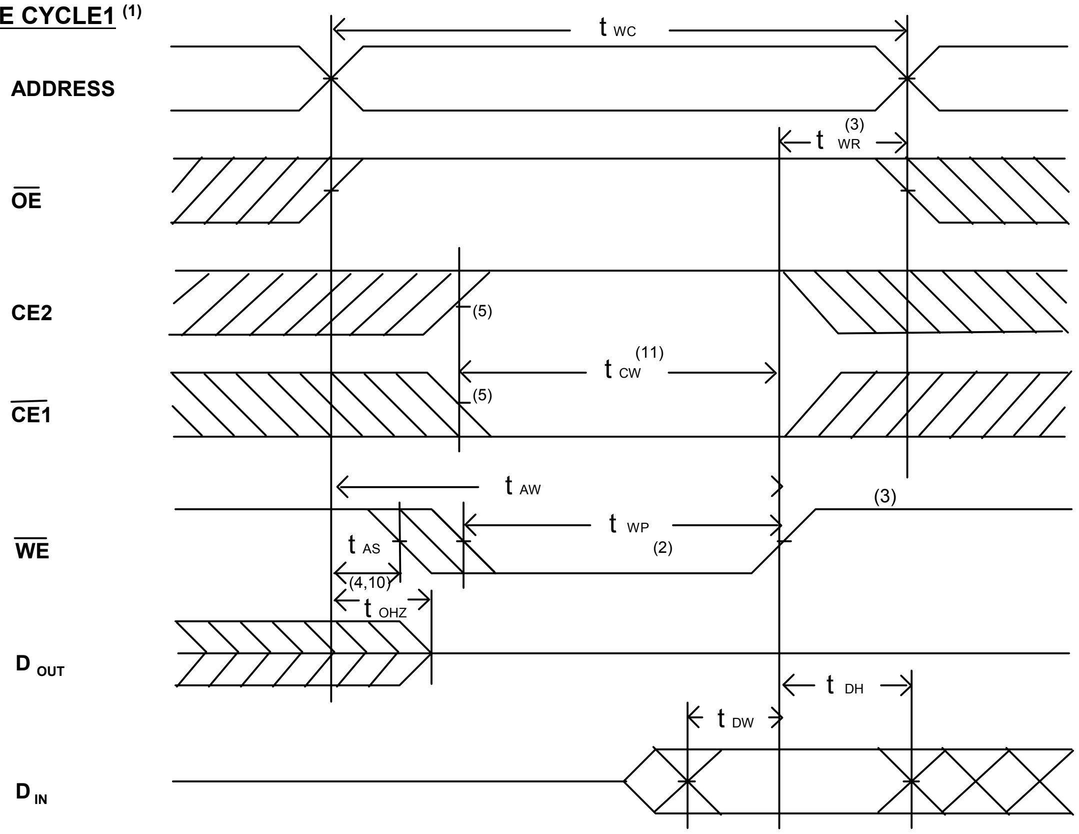
■ AC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C, Vcc=3V)

WRITE CYCLE

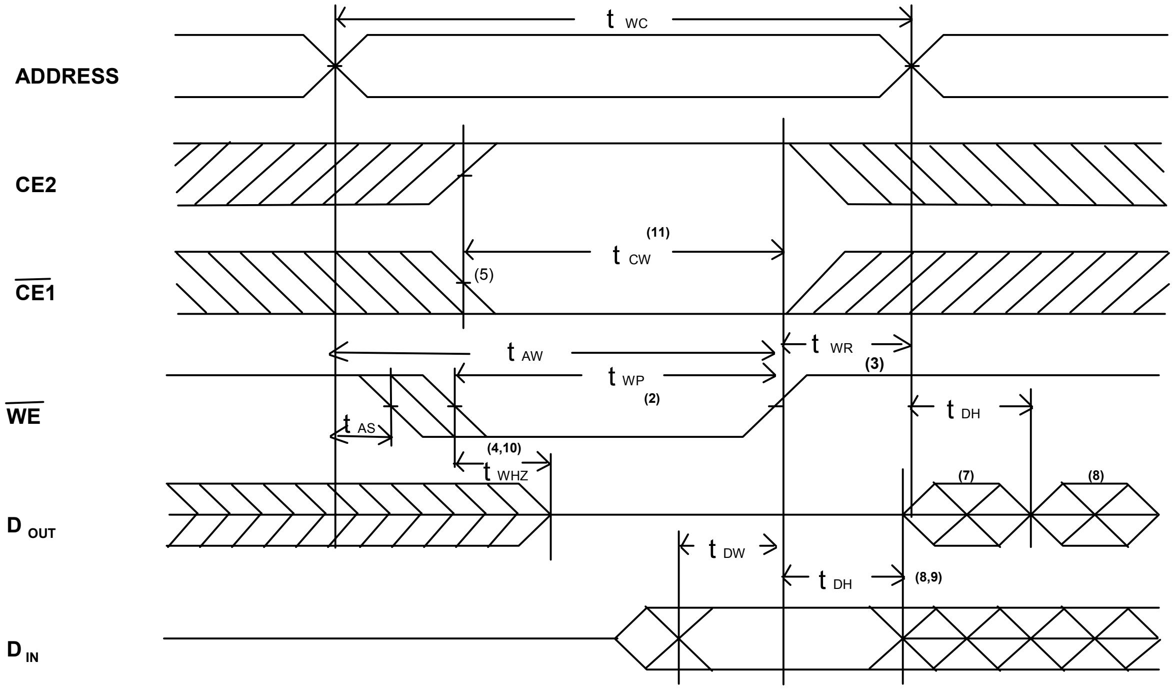
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616LV8011-70			BS616LV8011-10			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	70	--	--	100	--	--	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	70	--	--	100	--	--	ns
t_{AVWL}	t_{AS}	Address Setup Time	0	--	--	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	70	--	--	100	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	35	--	--	50	--	--	ns
t_{WHAX}	t_{WR}	Write recovery Time $(\overline{CE1}, CE2, \overline{WE})$	0	--	--	0	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	--	30	0	--	40	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	30	--	--	40	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	--	30	0	--	40	ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5	--	--	10	--	--	ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (1)



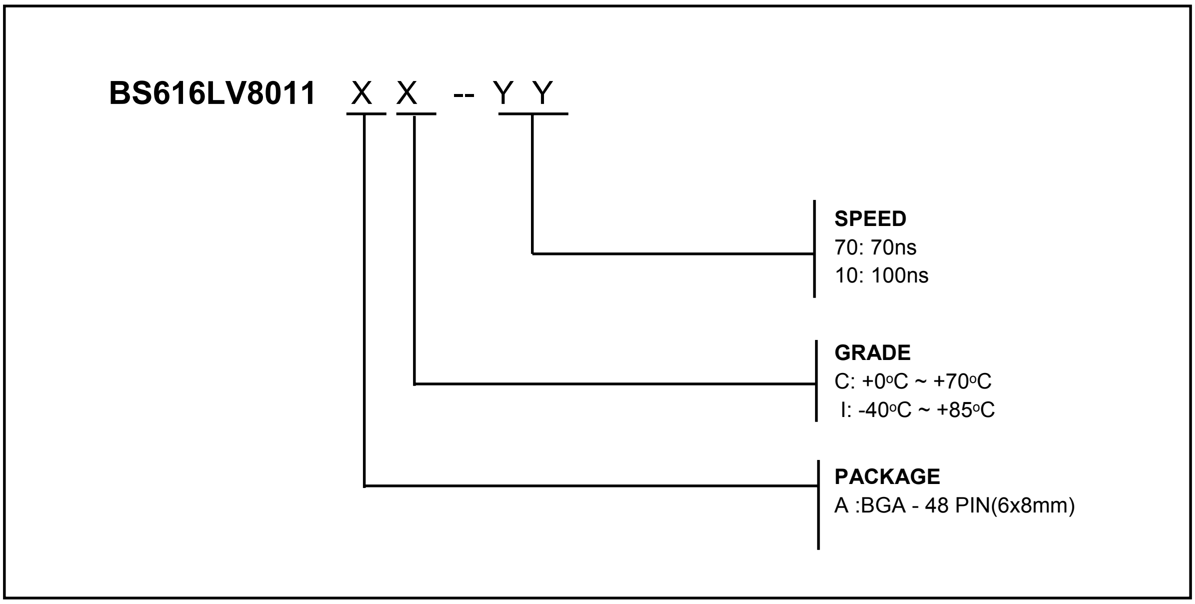
WRITE CYCLE2 (1,6)



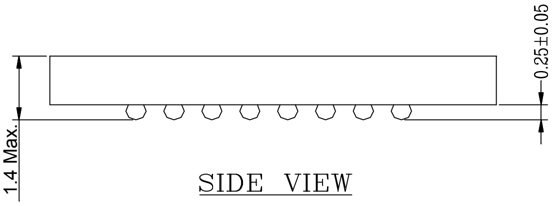
NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of CE2, $\overline{CE1}$ and $\overline{WE}$ low.
   All signals must be active to initiate a write and any one signal can terminate
   a write by going inactive. The data input setup and hold timing should be referenced to the
   second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of CE2 going low, or $\overline{CE1}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite
   phase to the outputs must not be applied.
5. If the CE2 high transition or $\overline{CE1}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions
   or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. DOUT is the same phase of write data of this write cycle.
8. DOUT is the read data of next address.
9. If CE2 is high or $\overline{CE1}$ is low during this period, DQ pins are in the output state. Then the
   data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500mV from steady state with CL = 30pF as shown in Figure 1B.
    The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of CE2 going high or $\overline{CE1}$ going low to the end of write.

■ ORDERING INFORMATION



■ PACKAGE DIMENSIONS



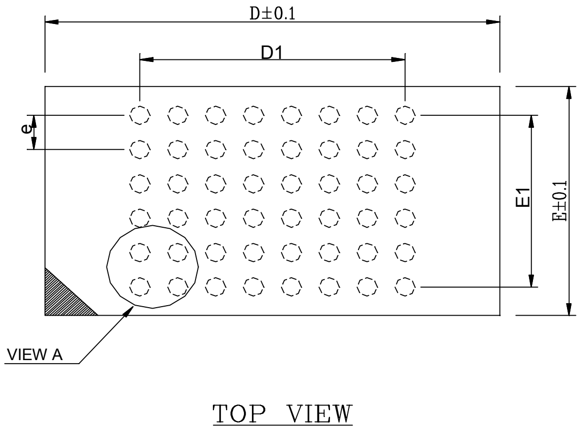
NOTES:

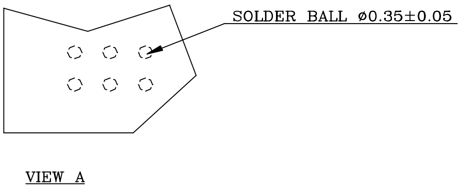
1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.

2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.

3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

BALL PITCH e = 0.75				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75





48 mini-BGA (6 x 8mm)

REVISION HISTORY

Revision	Description	Date	Note
2.2	**2001 Data Sheet release**	**Apr. 15, 2001**	
2.3	**Modify some AC parameters**	**April,11,2002**	