

P-CHANNEL ENHANCEMENT MODE DMOS TRANSISTOR

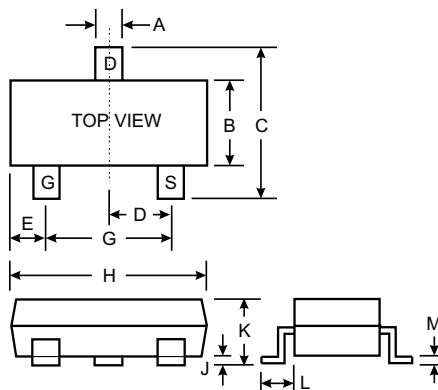
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Features

- High Input Impedance
- Fast Switching Speed
- CMOS Logic Compatible Input
- No Thermal Runaway or Secondary Breakdown
- Surface Mount Package Ideally Suited for Automatic Assembly

Mechanical Data

- Case: SOT-23, Plastic
- Terminals: Solderable per MIL-STD-202 Method 208
- Pin Connection: See Diagram
- Marking: S50
- Weight: 0.008 grams (approx.)



SOT-23		
Dim	Min	Max
A	0.37	0.51
B	1.19	1.40
C	2.10	2.50
D	0.89	1.05
E	0.45	0.61
G	1.78	2.05
H	2.65	3.05
J	0.013	0.15
K	0.89	1.10
L	0.45	0.61
M	0.076	0.178
All Dimensions in mm		

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DS}$	60	V
Drain-Gate Voltage	$-V_{DG}$	60	V
Gate-Source Voltage (pulsed)	V_{GS}	± 20	V
Drain Current (continuous)	$-I_D$	250	mA
Power Dissipation @ $T_C = 25^\circ\text{C}$ (Note 1)	P_d	310	mW
Operating and Storage Temperature Range	T_j, T_{STG}	-65 to +150	$^\circ\text{C}$

Inverse Diode @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Maximum Forward Current (continuous)	I_F	0.30	A
Forward Voltage Drop (typ.) @ $V_{GS} = 0, I_F = 0.12\text{A}, T_j = 25^\circ\text{C}$	V_F	0.85	V

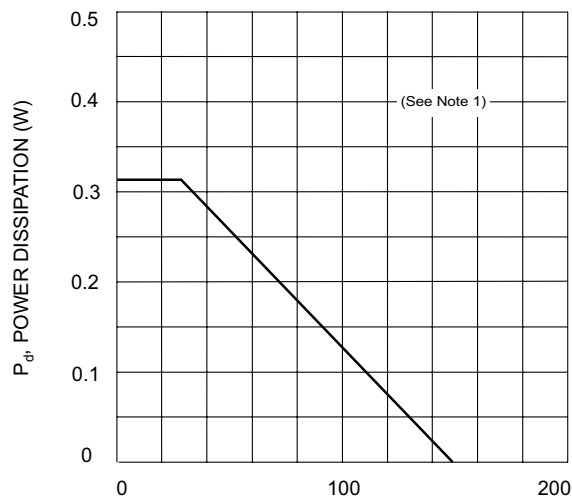
Notes: 1. Device mounted on Ceramic Substrate 0.7mm; 2.5 cm² area.

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

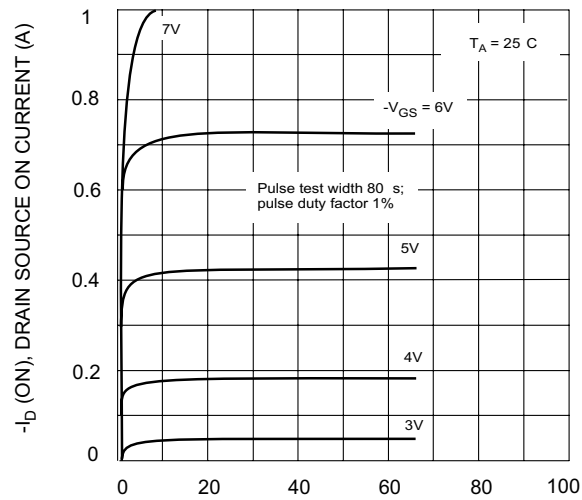
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Drain-Source Breakdown Voltage	$-V_{(BR)DSS}$	60	90	—	V	$-I_D = 100\mu\text{A}$, $V_{GS} = 0$
Gate Threshold Voltage	$V_{GS(th)}$	—	1.0	3.0	V	$-V_{GS} = V_{DS}$, $-I_D = 1.0\text{mA}$
Gate-Body Leakage Current	$-I_{GSS}$	—	—	10	nA	$-V_{GS} = 15\text{V}$, $V_{DS} = 0$
Drain-Source Cutoff Current	$-I_{DSS}$	—	—	0.5	μA	$-V_{DS} = 25\text{V}$, $V_{GS} = 0$
Drain-Source ON Resistance	$r_{DS(ON)}$	—	3.5	5.0	Ω	$-V_{GS} = 10\text{V}$, $-I_D = 0.2\text{A}$
Thermal Resistance, Junction to Ambient Air	$R_{\theta JA}$	—	—	400	K/W	Note 1
Thermal Resistance Junction to Substrate Backside	$R_{\theta JSB}$	—	—	320	K/W	Note 1
Forward Transconductance	g_{FS}	—	200	—	mS	$-V_{DS} = 10\text{V}$, $-I_D = 0.2\text{A}$, $f = 1.0\text{MHz}$
Input Capacitance	C_{iss}	—	60	—	pF	$-V_{DS} = 10\text{V}$, $V_{GS} = 0$, $f = 1.0\text{MHz}$
Switching Times Turn On Time Turn Off Time	t_{on} t_{off}	—	5.0 25	—	ns	$-V_{GS} = 10\text{V}$, $-V_{DS} = 10\text{V}$, $R_D = 100\Omega$

Notes: 1. Device mounted on ceramic substrate 0.7mm; 2.5 cm² area.

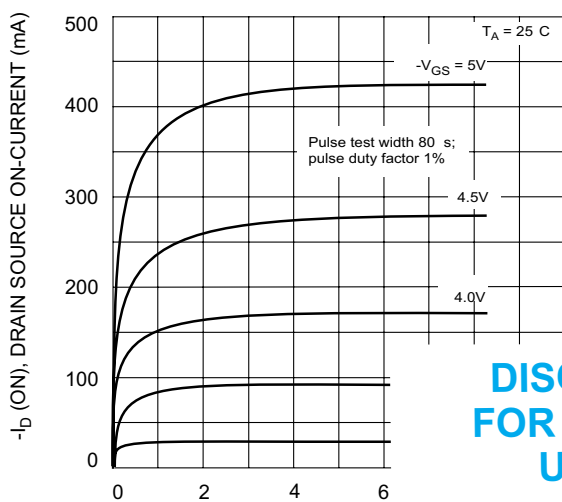
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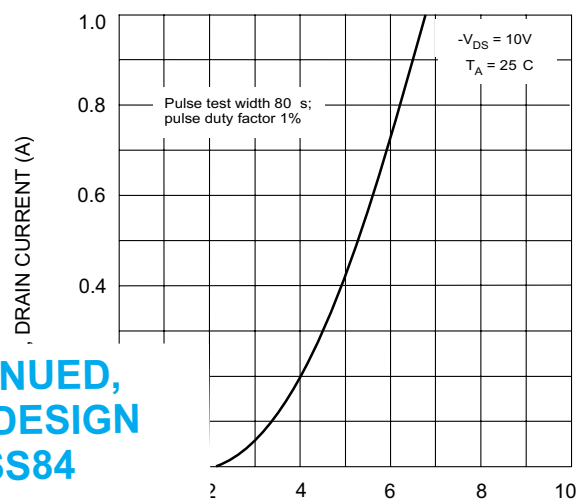
T_A , AMBIENT TEMPERATURE (°C)
Fig. 1. Power Derating Curve



$-V_{DS}$, DRAIN-SOURCE VOLTAGE (V)
Fig. 2. Output Characteristics



$-V_{DS}$, DRAIN-SOURCE VOLTAGE (V)
Fig. 3. Saturation Characteristics



$-V_{GS}$, GATE-SOURCE VOLTAGE (V)
Fig. 4. Drain Current vs Gate-Source Voltage

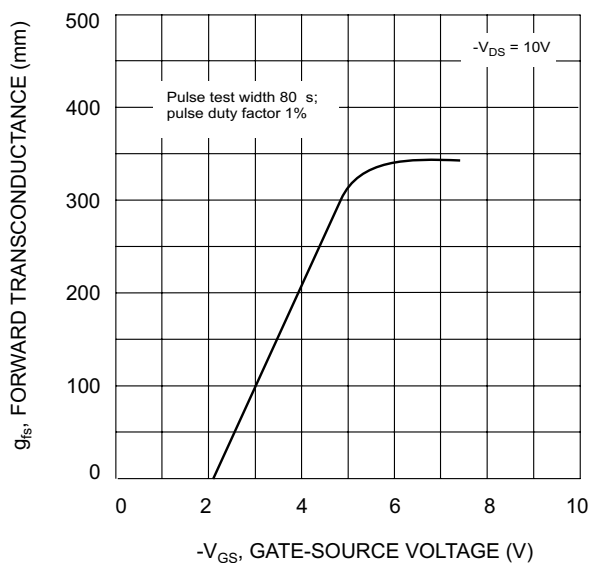


Fig. 5. Transconductance vs Gate-Source Voltage

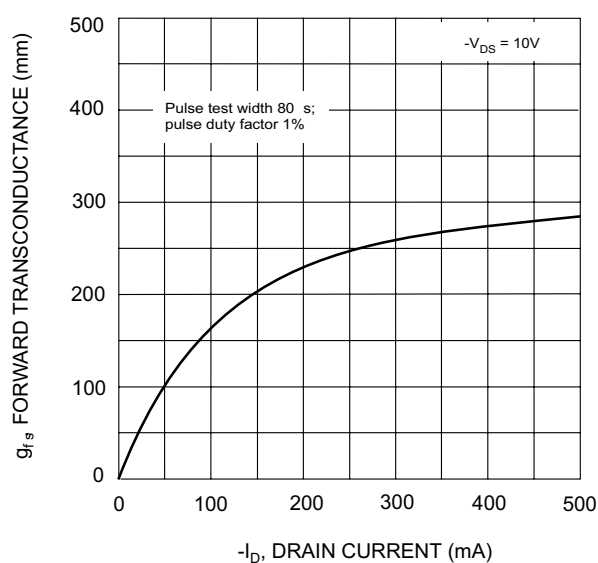


Fig. 6. Transconductance vs. Drain Current

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