

## MOSFET

OptiMOS™ Power-Transistor, 60 V

### Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 175°C rated
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

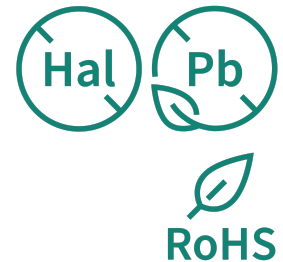
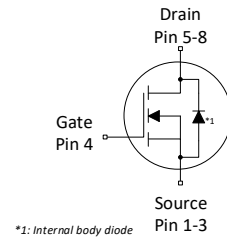
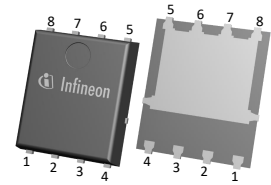
### Product validation

Fully qualified according to JEDEC for Industrial Applications

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	60	V
$R_{DS(on),max}$	2.8	mΩ
$I_D$	137	A
$Q_{oss}$	43	nC
$Q_G(0..10V)$	37	nC

PG-TDSON-8



Type/Ordering Code	Package	Marking	Related Links
BSC028N06NS	PG-TDSON-8	028N06NS	-



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# 1 Maximum ratings

unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	137 97 24	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$ $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{K/W}^2)$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	548	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	100	mJ	$I_D=50\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	100 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^3)$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	0.9	1.5	K/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	$R_{thJA}$	-	-	50	K/W	-

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}, I_D=50\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.5 10	1 100	$\mu\text{A}$	$V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$ $V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.3 3.4	2.8 4.2	m $\Omega$	$V_{GS}=10\text{ V}, I_D=50\text{ A}$ $V_{GS}=6\text{ V}, I_D=12.5\text{ A}$
Gate resistance <sup>6)</sup>	$R_G$	-	1.3	1.95	$\Omega$	-
Transconductance	$g_{fs}$	50	100	-	S	$ V_{DS} >2 I_D  R_{DS(on)max}, I_D=50\text{ A}$

<sup>6)</sup> Defined by design. Not subject to production test

**Table 5 Dynamic characteristics <sup>7)</sup>**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	2025	2700	3375	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Output capacitance	$C_{oss}$	495	660	825	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	8.5	28	56	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	11	22	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=3\text{ }\Omega$
Rise time	$t_r$	-	38	57	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=3\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	19	38	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=3\text{ }\Omega$
Fall time	$t_f$	-	8	16	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=3\text{ }\Omega$

<sup>7)</sup> Defined by design. Not subject to production test

**Table 6 Gate charge characteristics <sup>8)</sup>**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	9	12	16.5	nC	$V_{DD}=30\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	6	8	11	nC	$V_{DD}=30\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	5	7	10.3	nC	$V_{DD}=30\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	8	12	17	nC	$V_{DD}=30\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	$Q_g$	31	37	49	nC	$V_{DD}=30\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	4.0	4.6	5.2	V	$V_{DD}=30\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	27	33	43	nC	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }10\text{ V}$

**Table 6 Gate charge characteristics** <sup>8)</sup>

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Output charge	$Q_{oss}$	32	43	54	nC	$V_{DD}=30\text{ V}, V_{GS}=0\text{ V}$

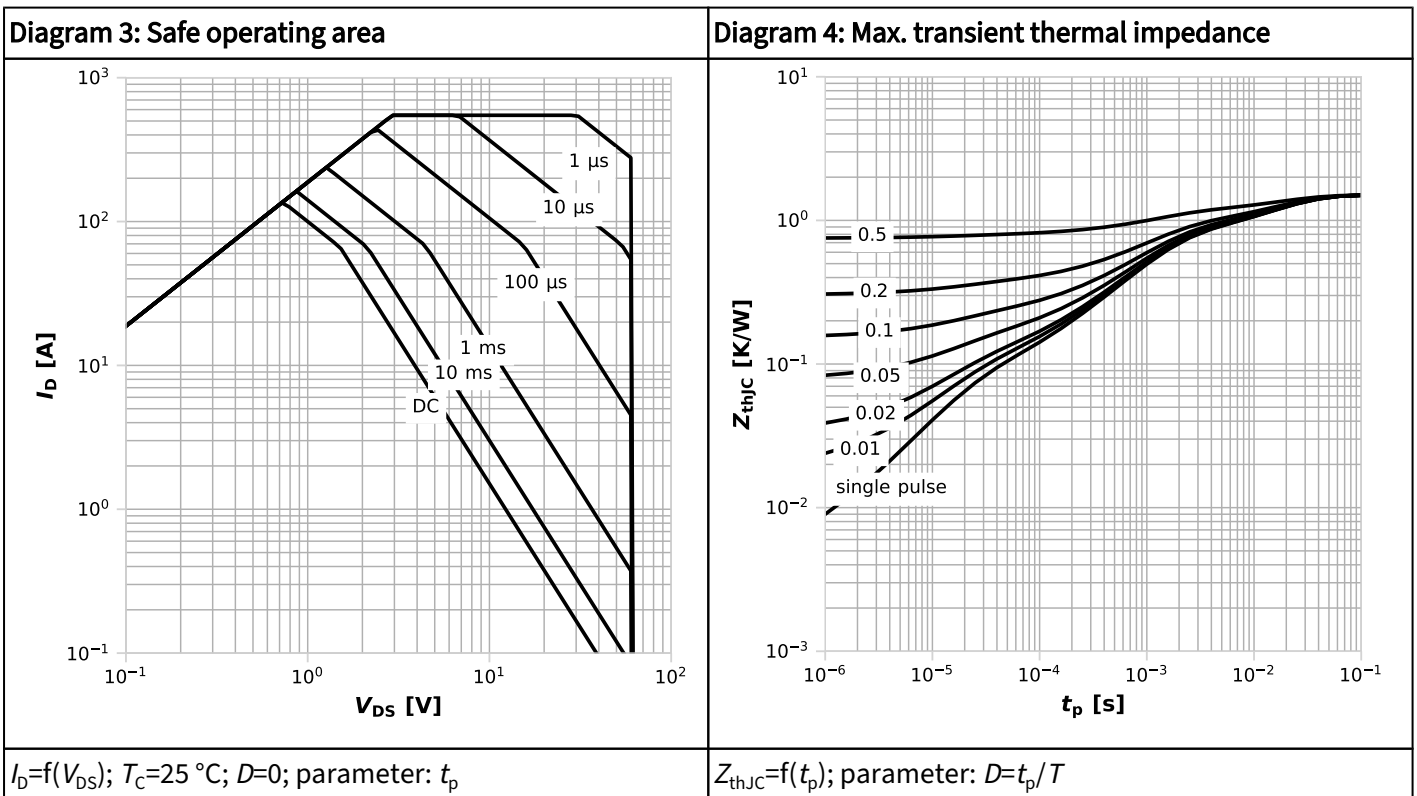
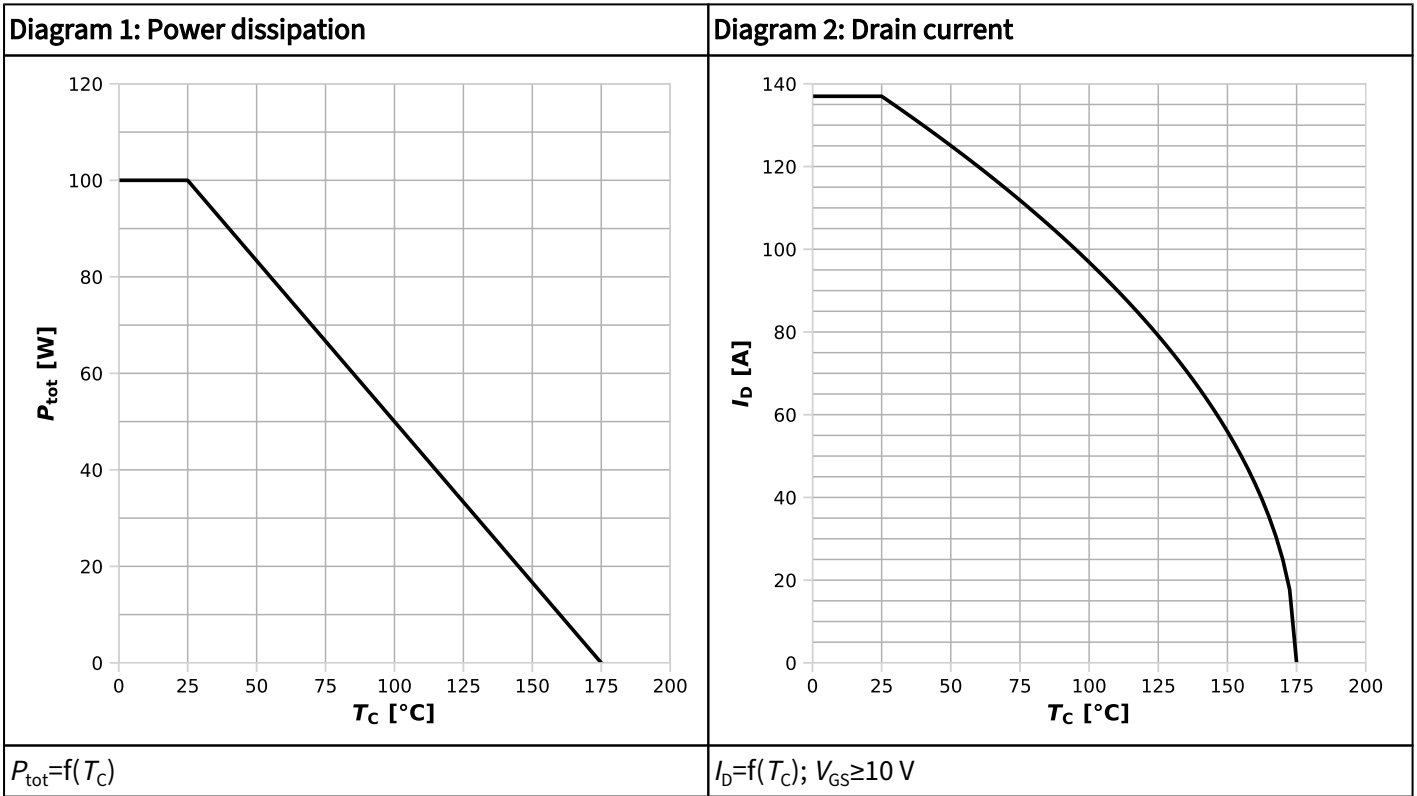
<sup>8)</sup> See "Gate charge waveforms" for parameter definition. Defined by design. Not subject to production test

**Table 7 Reverse diode**

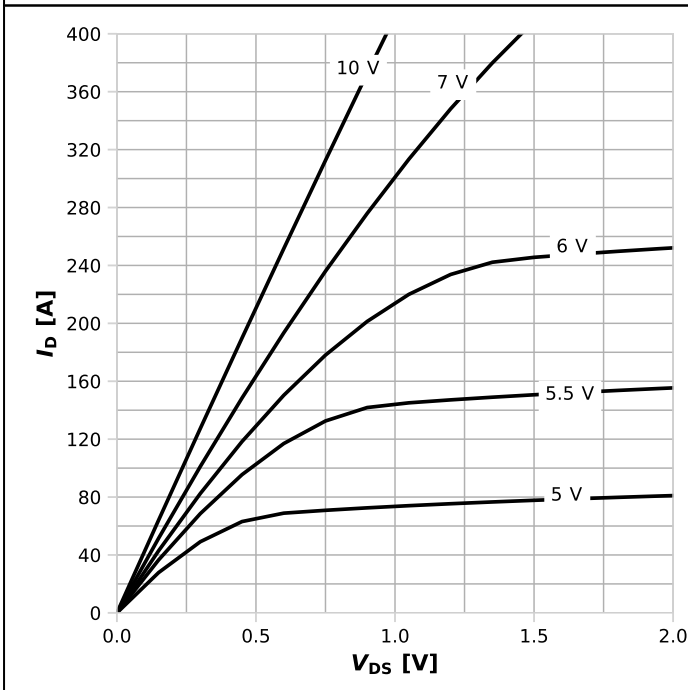
Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	91	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	548	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.9	1.2	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>9)</sup>	$t_{rr}$	14	35	56	ns	$V_R=30\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>9)</sup>	$Q_{rr}$	14	29	58	nC	$V_R=30\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>9)</sup> Defined by design. Not subject to production test

## 4 Electrical characteristics diagrams

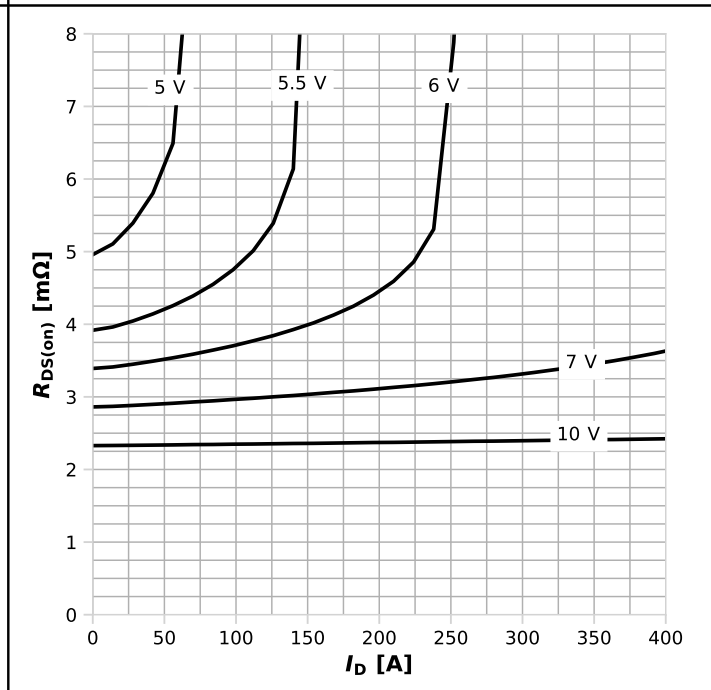


**Diagram 5: Typ. output characteristics**



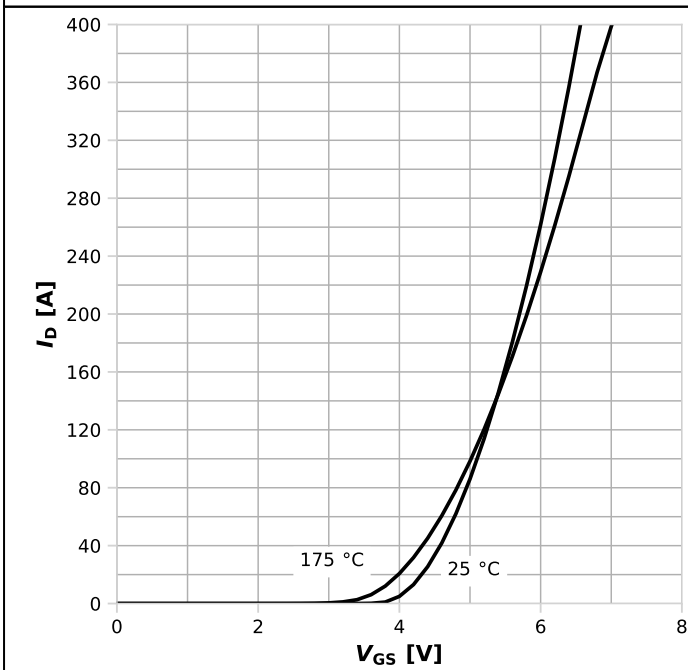
$I_D = f(V_{DS}); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



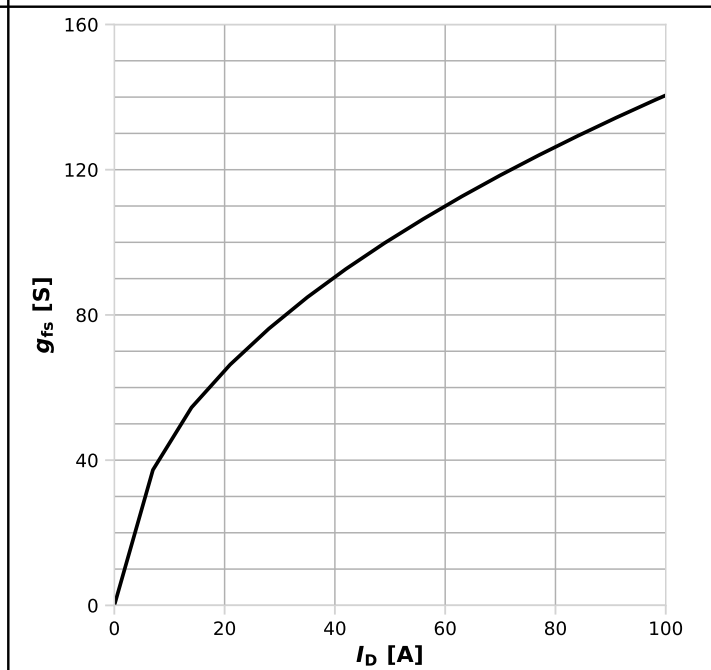
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

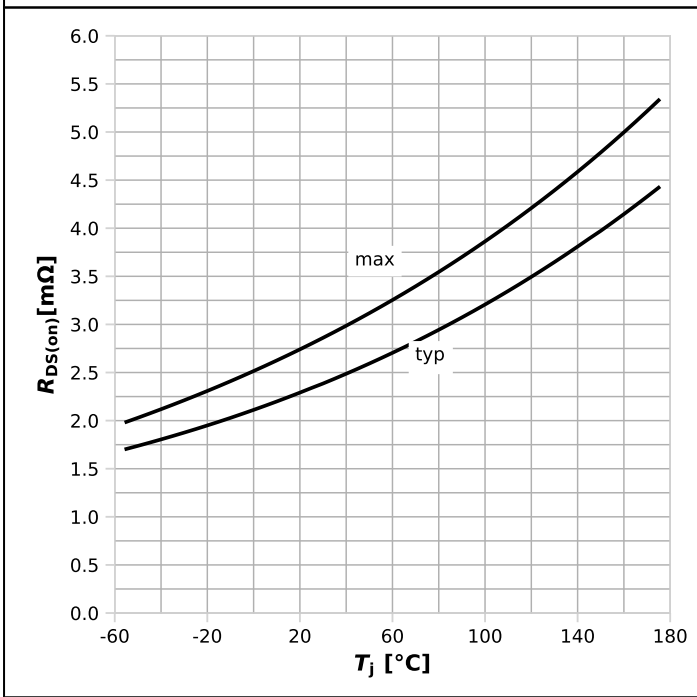
**Diagram 8: Typ. forward transconductance**



$g_{fs} = f(I_D); T_j = 25\text{ °C}$

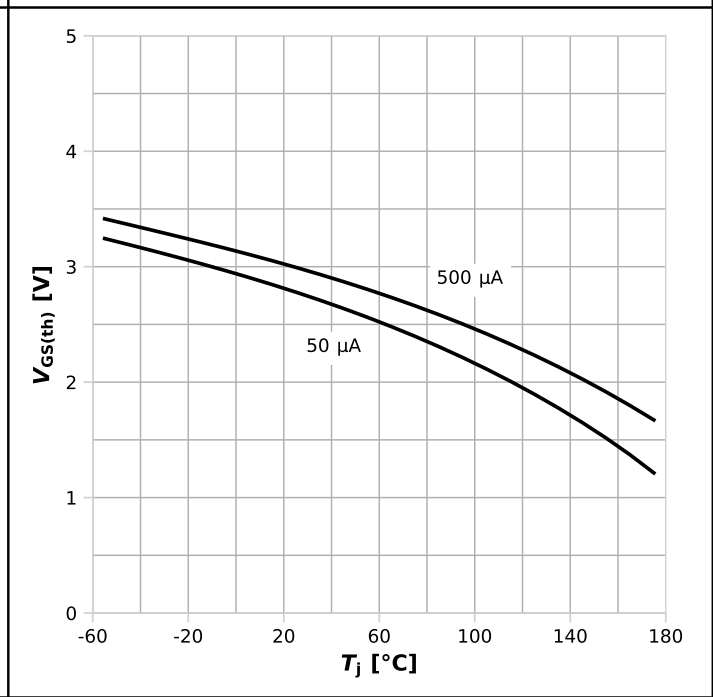


**Diagram 9: Drain-source on-state resistance**



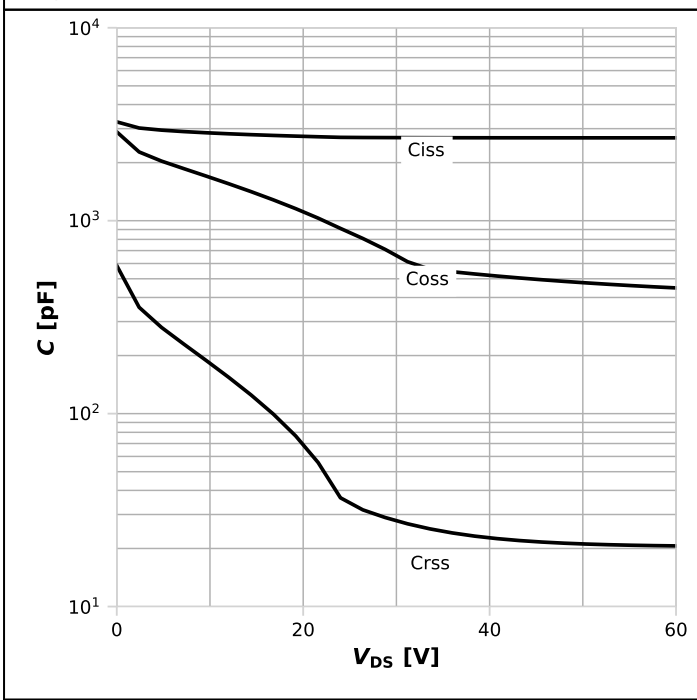
$R_{DS(on)}=f(T_j); I_D=50\text{ A}; V_{GS}=10\text{ V}$

**Diagram 10: Typ. gate threshold voltage**



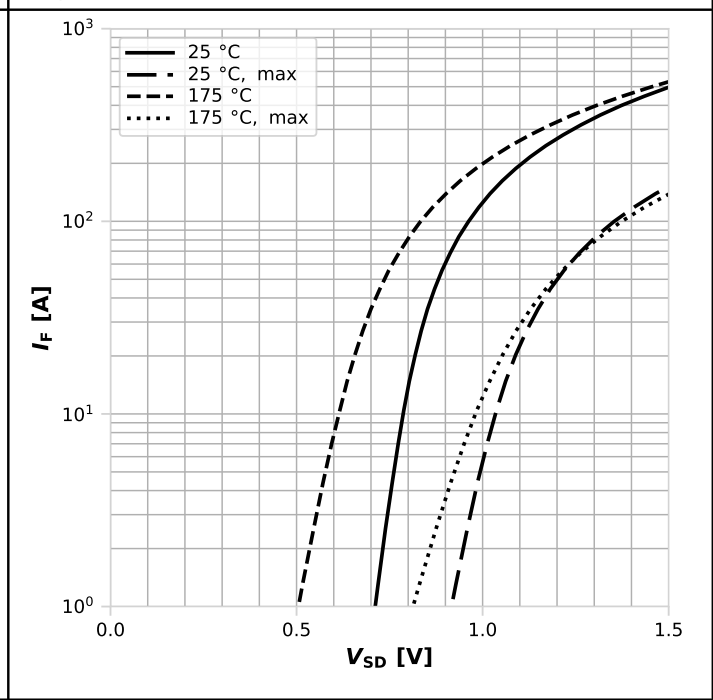
$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$

**Diagram 11: Typ. capacitances**



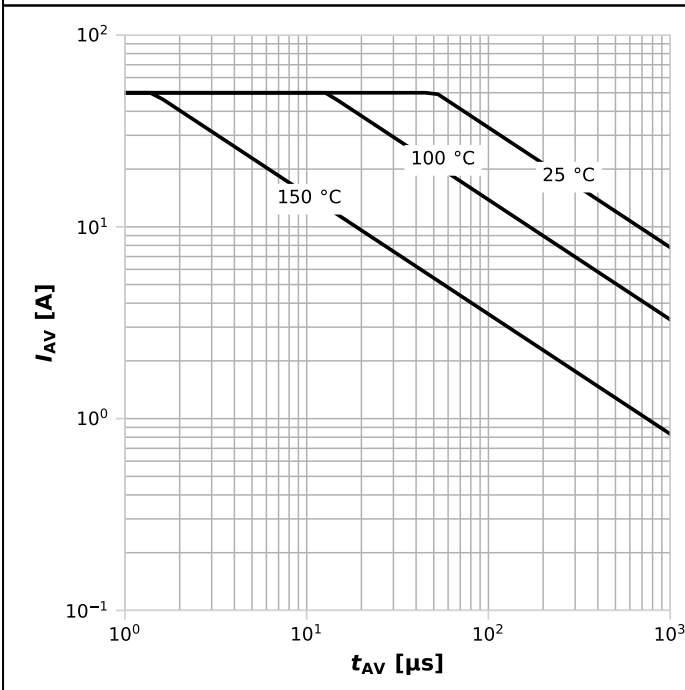
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

**Diagram 12: Forward characteristics of reverse diode**



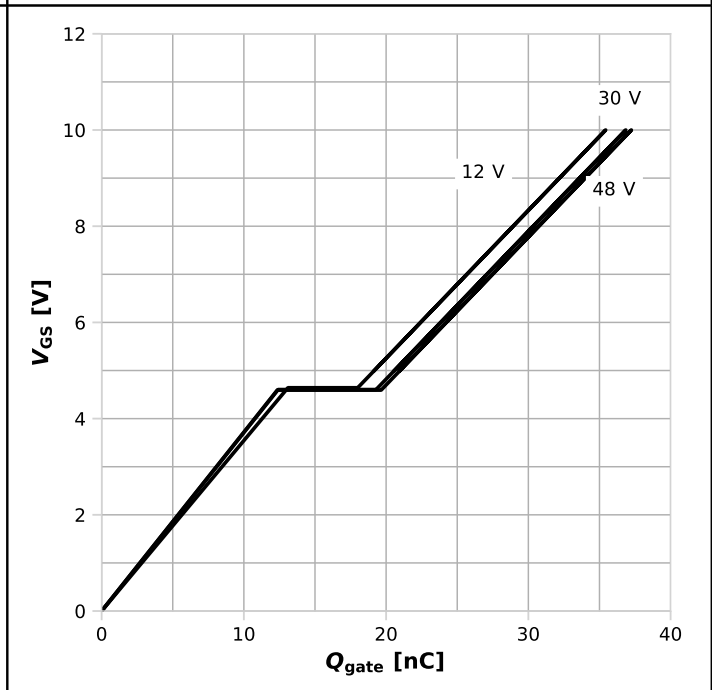
$I_F=f(V_{SD}); \text{parameter: } T_j$

**Diagram 13: Avalanche characteristics**



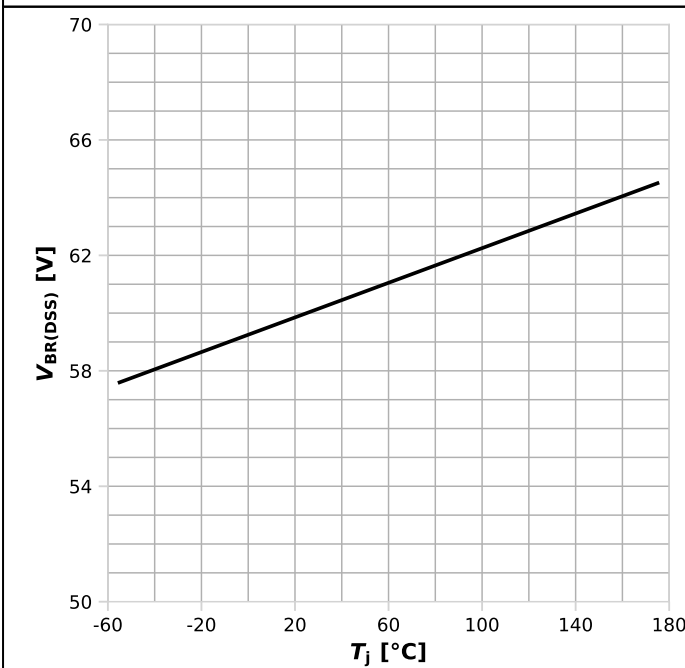
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

**Diagram 14: Typ. gate charge**



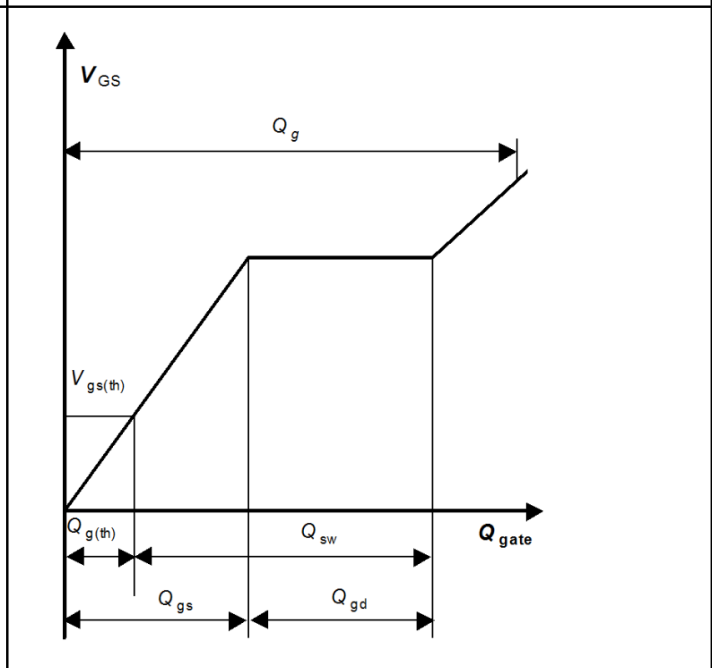
$V_{GS}=f(Q_{gate}); I_D=50 \text{ A pulsed}$ ; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**



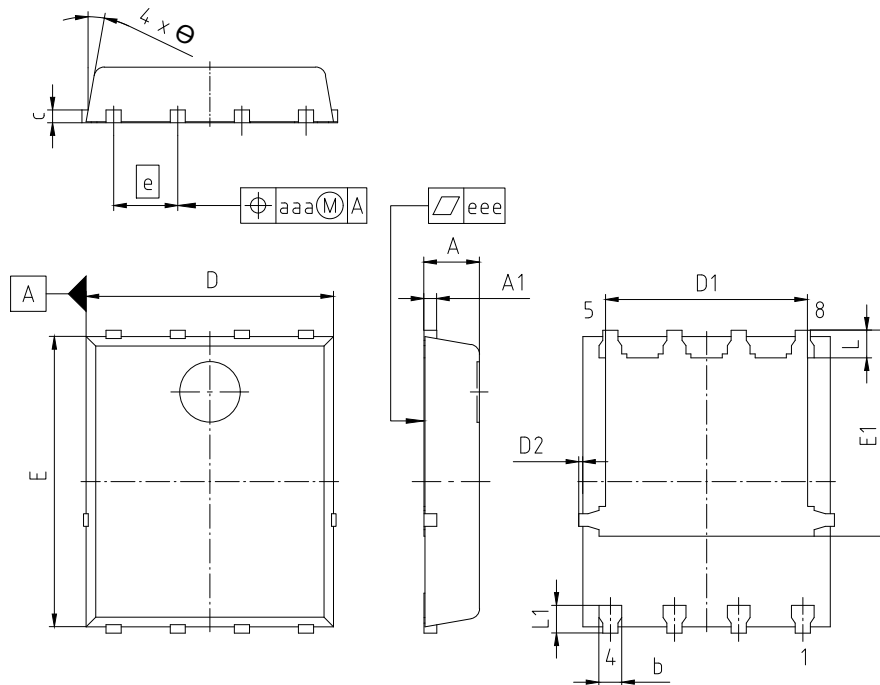
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Gate charge waveforms**



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## 5 Package Outlines



PACKAGE - GROUP NUMBER: PG-TDSON-8-U08		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	4.03	4.25
e	1.27	
L	0.45	0.72
L1	0.45	0.71
aaa	0.25	
eee	0.05	
θ	8°	12°

- 1) EXCLUDING MOLD FLASH
- 2) REMOVAL ON MOLD GATE  
INTRUSION 0.1 MM  
PROTRUSION 0.1 MM
- 3) ALL METAL SURFACES ARE PLATED,  
EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

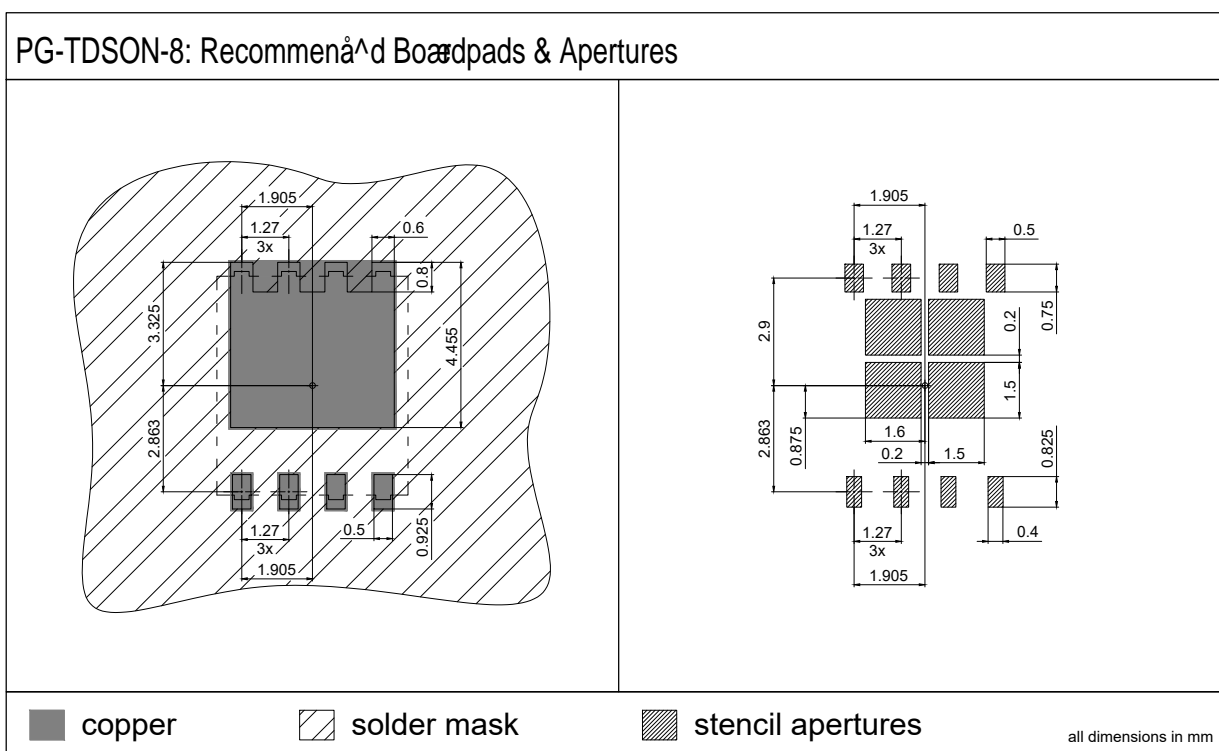
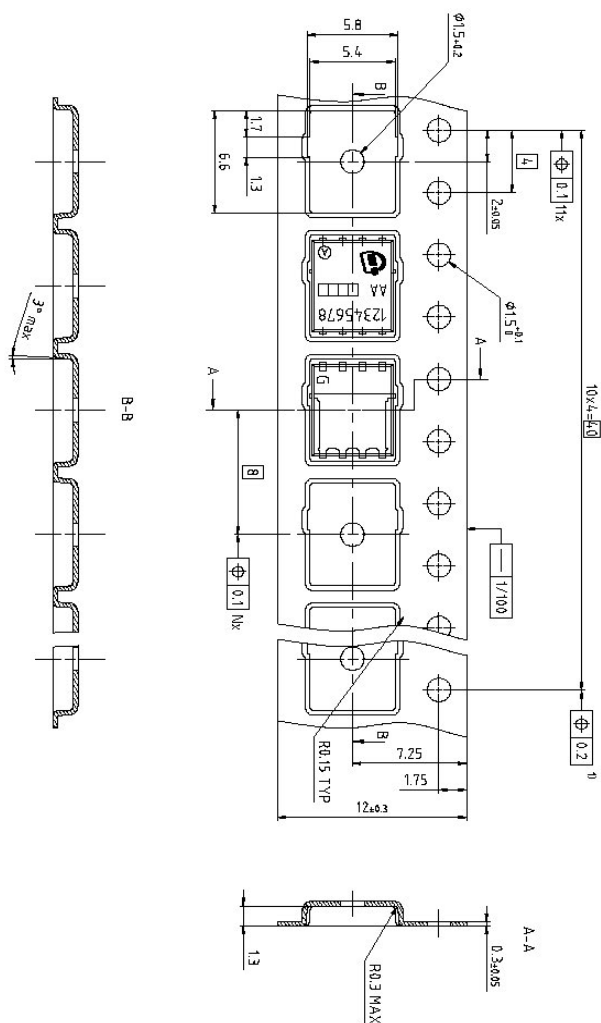


Figure 2 Outline PG-TDSON-8, dimensions in mm



Dimension in mm

Figure 3 Outline PG-TDSON-8, dimensions in mm

## Revision History

BSC028N06NS

### Revision 2024-06-11, Rev. 2.6

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.3	2014-11-10	Added RthJC_typ, updated outline and footprint drawings, insert footnote "Defined by design...."
2.4	2020-02-04	Update package drawings
2.5	2020-09-21	Update current rating
2.6	2024-06-11	Upgrade Operating and storage temperature max to 175°C . Update drawings in section 5 Package Outlines. Production validation added on page1. Update Is max and Is Pulse Max.

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Public

OptiMOS™ Power-Transistor, 60 V

BSC028N06NS

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