

OptiMOS™2 Power-Transistor

Features

- N-channel, logic level
- Very low gate charge x $R_{DS(on)}$ product (FOM)
- Ideal for high-frequency switching and synchronous rectification
- Low on-resistance $R_{DS(on)}$
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target application
- 150 °C operating temperature
- Halogen-free according to IEC61249-2-21

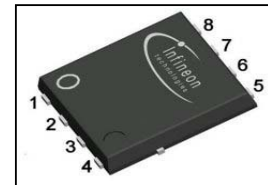


Halogen-Free

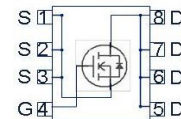
Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	26.5	mΩ
I_D	40	A

PG-TDSON-8



Type	Package	Marking
BSC265N10LSF G	PG-TDSON-8	265N10LS



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$	40	A
		$T_C=100\text{ °C}$	26	
		$T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}^{2)}$	6.5	
Pulsed drain current ³⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	160	
Avalanche energy, single pulse	E_{AS}	$I_D=40\text{ A}$, $R_{GS}=25\text{ Ω}$	68	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	78	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}	bottom	-	-	1.6	K/W
		top	-	-	18	
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ²⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=43\text{ }\mu\text{A}$	1.2	1.85	2.4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}$, $I_D=10\text{ A}$	-	27.7	36	m Ω
		$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$	-	20	26.5	
Gate resistance	R_G		-	1.5	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=40\text{ A}$	21	41	-	S

¹⁾J-STD20 and JESD22

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ see figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V},$ $f=1\text{ MHz}$	-	1200	1600	pF
Output capacitance	C_{oss}		-	280	370	
Reverse transfer capacitance	C_{rss}		-	8	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V},$ $I_D=25\text{ A}, R_G=1.6\ \Omega$	-	10	-	ns
Rise time	t_r		-	24	-	
Turn-off delay time	$t_{d(off)}$		-	20	-	
Fall time	t_f		-	4	-	

Gate Charge Characteristics⁴⁾

Gate to source charge	Q_{gs}	$V_{DD}=50\text{ V}, I_D=25\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	5	-	nC
Gate to drain charge	Q_{gd}		-	3	-	
Switching charge	Q_{sw}		-	6	-	
Gate charge total	Q_g		-	16	21	
Gate plateau voltage	$V_{plateau}$		-	4.1	-	V
Output charge	Q_{oss}	$V_{DD}=50\text{ V}, V_{GS}=0\text{ V}$	-	27	36	nC

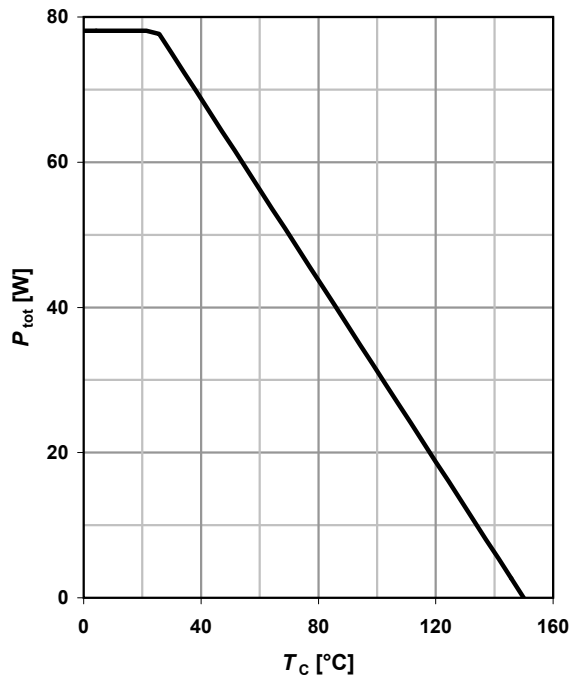
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	40	A
Diode pulse current	$I_{S,pulse}$		-	-	160	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=40\text{ A},$ $T_j=25\text{ °C}$	-	1	1.2	V
Reverse recovery time	t_{rr}	$V_R=50\text{ V}, I_F=25\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	86	-	ns
Reverse recovery charge	Q_{rr}		-	238	-	nC

⁴⁾ See figure 16 for gate charge parameter definition

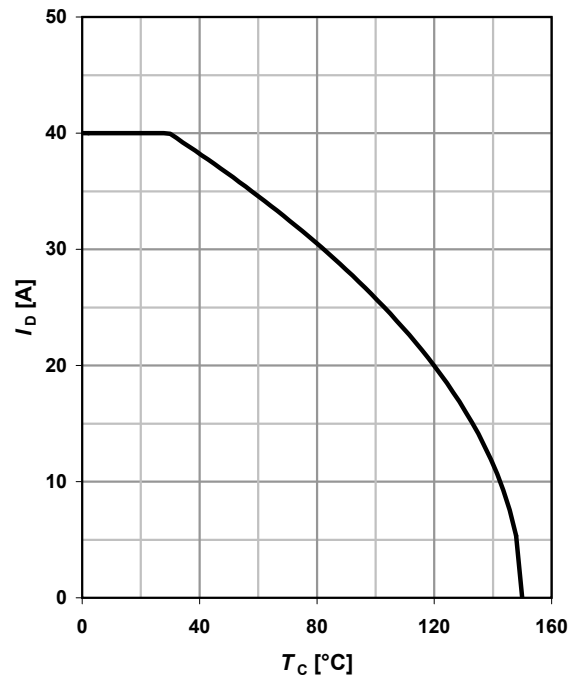
1 Power dissipation

$$P_{\text{tot}} = f(T_c)$$



2 Drain current

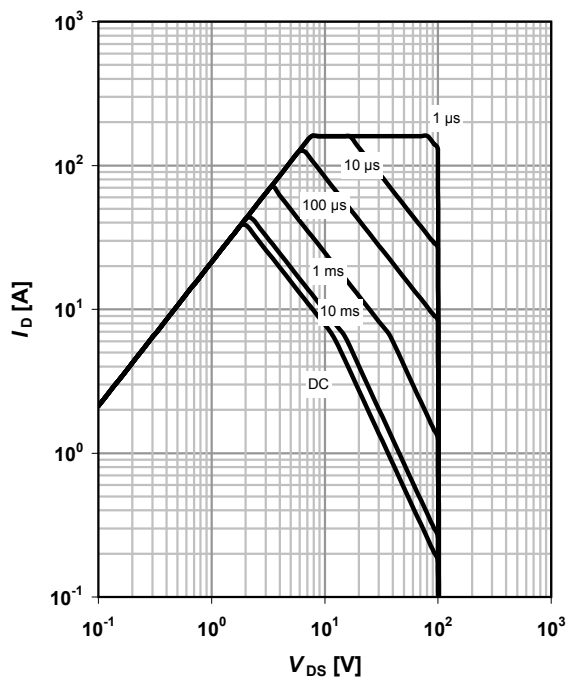
$$I_D = f(T_c); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_c = 25^\circ\text{C}; D = 0$$

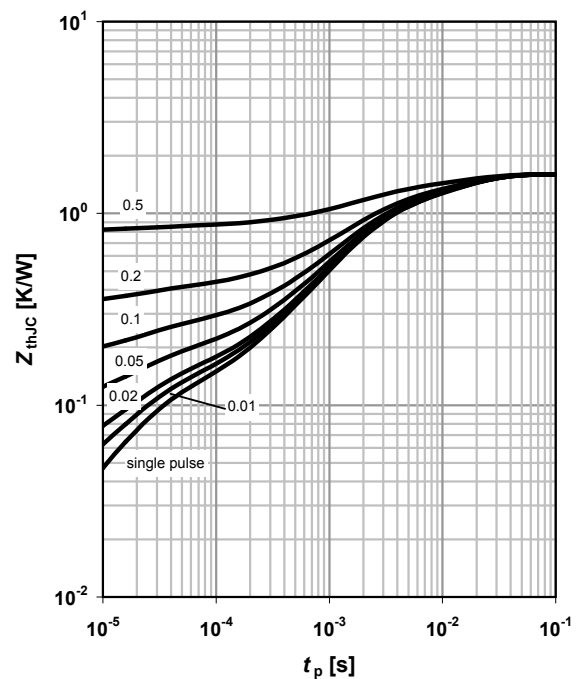
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

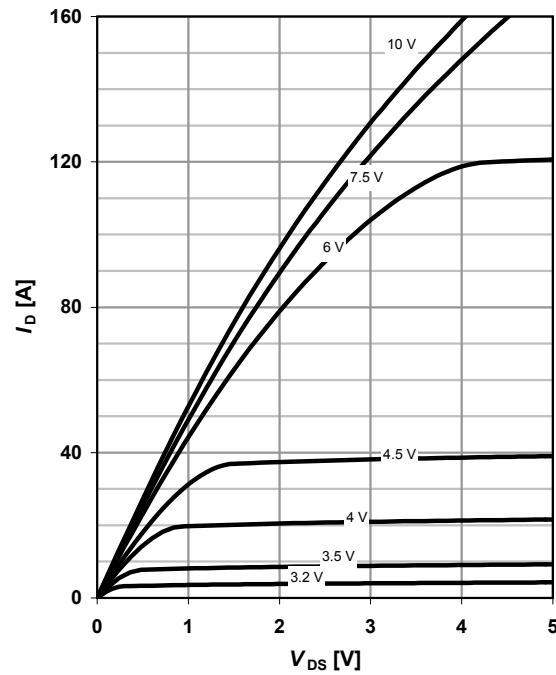
parameter: $D = t_p / T$



5 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

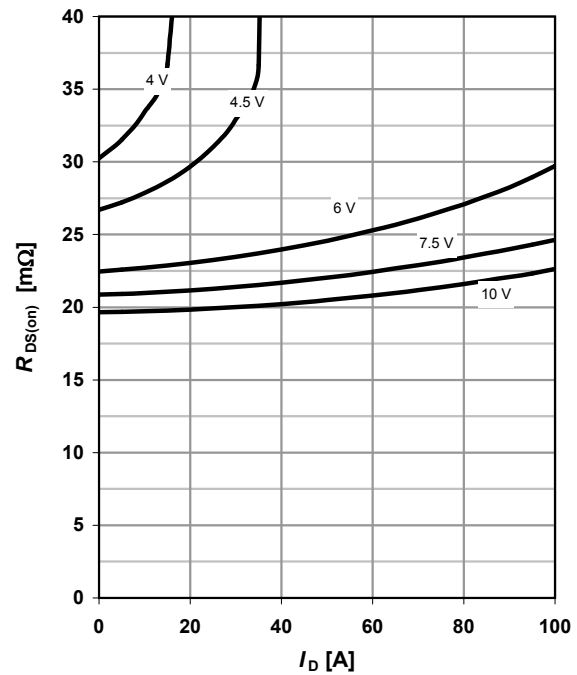
parameter: V_{GS}



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

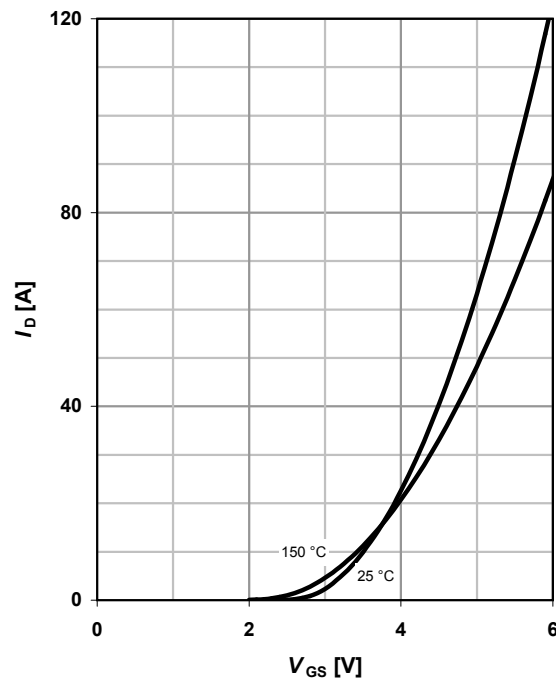
parameter: V_{GS}



7 Typ. transfer characteristics

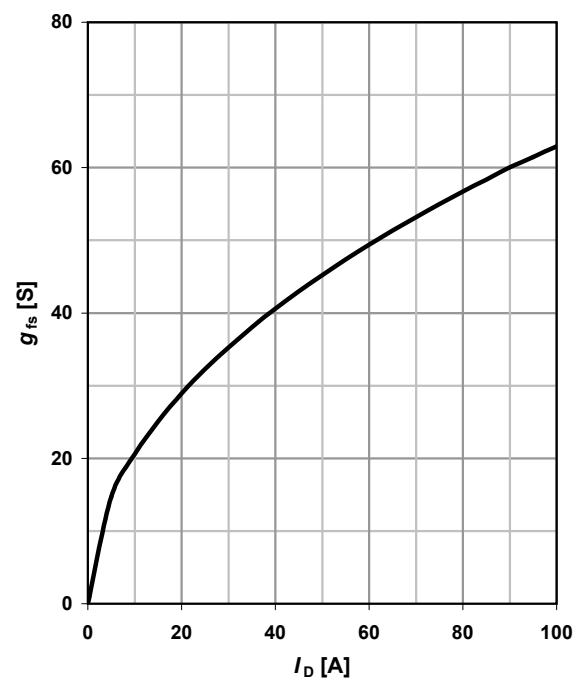
$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)\max}$$

parameter: T_j



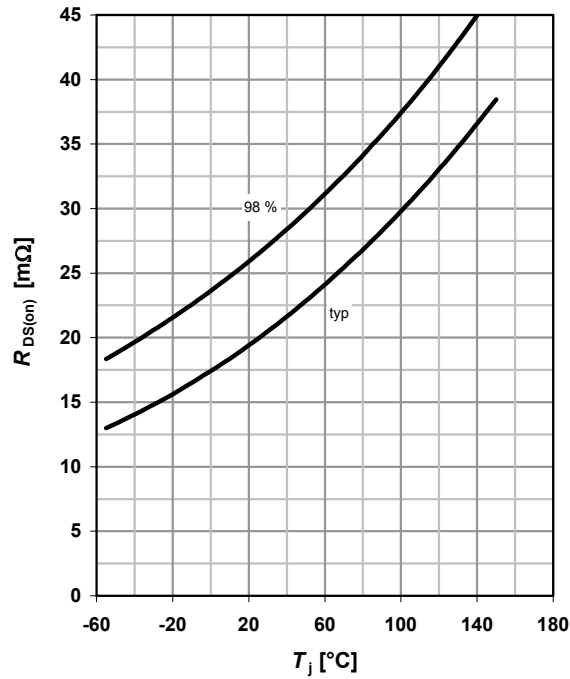
8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$



9 Drain-source on-state resistance

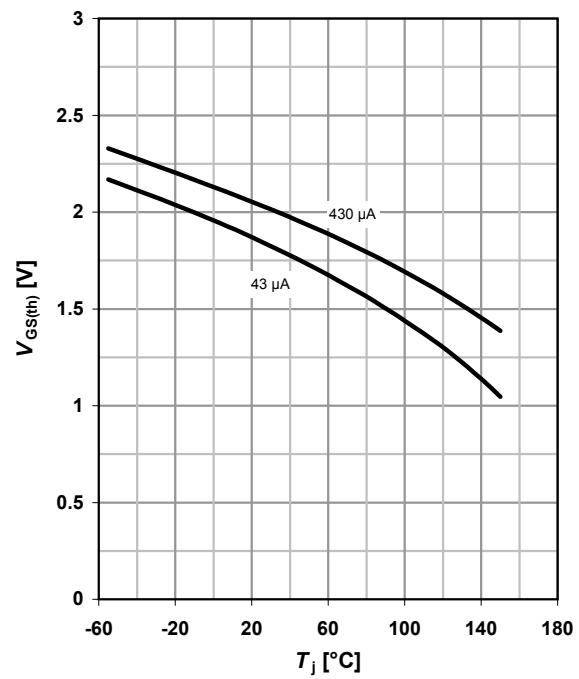
$$R_{DS(on)} = f(T_j); I_D = 40 \text{ A}; V_{GS} = 10 \text{ V}$$



10 Typ. gate threshold voltage

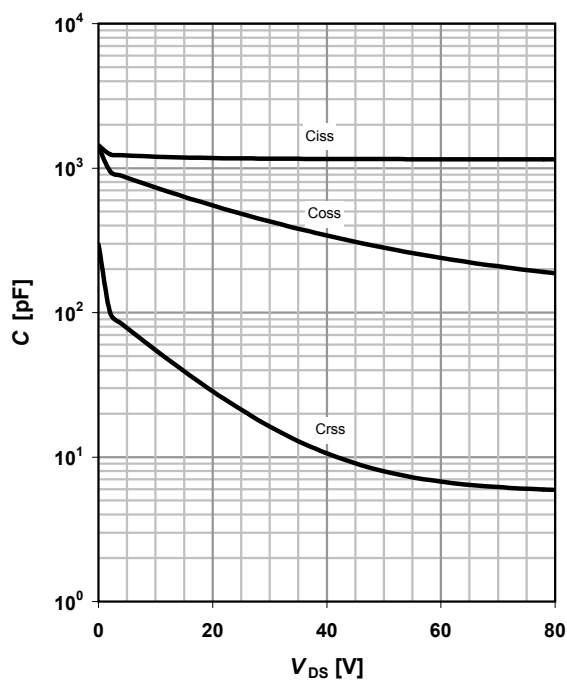
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



11 Typ. capacitances

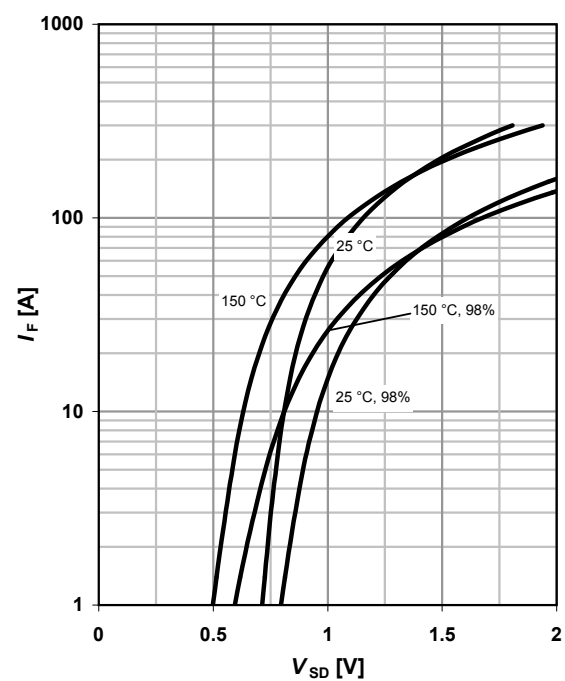
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

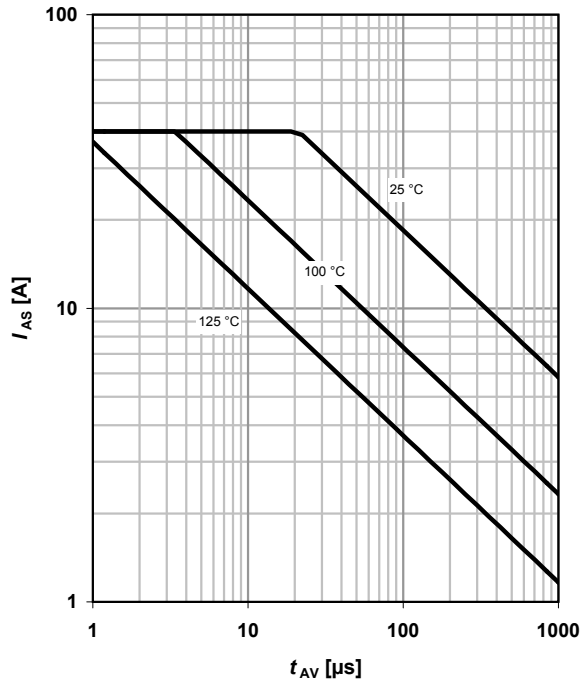
parameter: T_j



13 Avalanche characteristics

$$I_{AS} = f(t_{AV}); R_{GS} = 25 \, \Omega$$

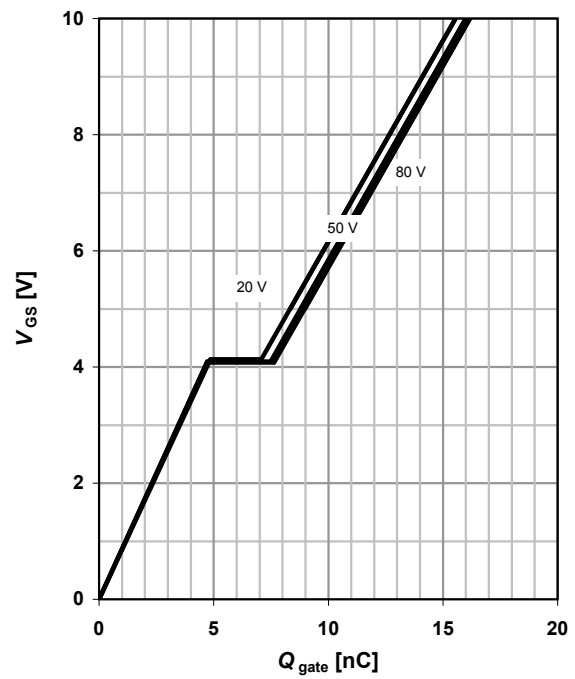
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

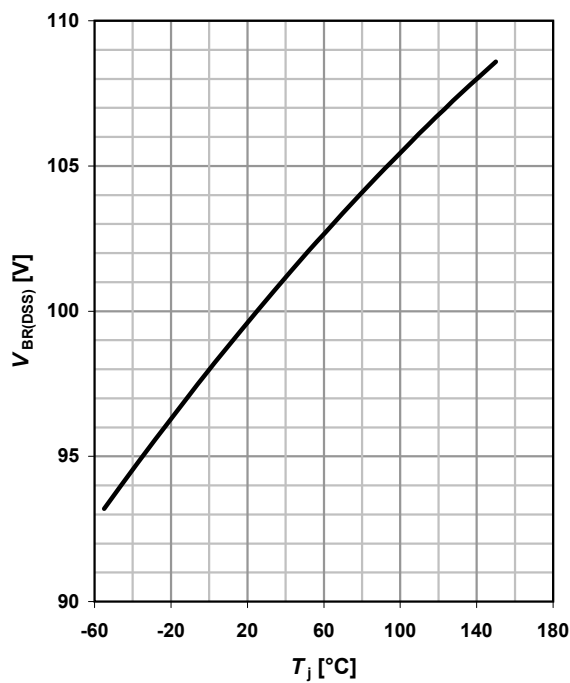
$$V_{GS} = f(Q_{\text{gate}}); I_D = 25 \, \text{A pulsed}$$

parameter: V_{DD}

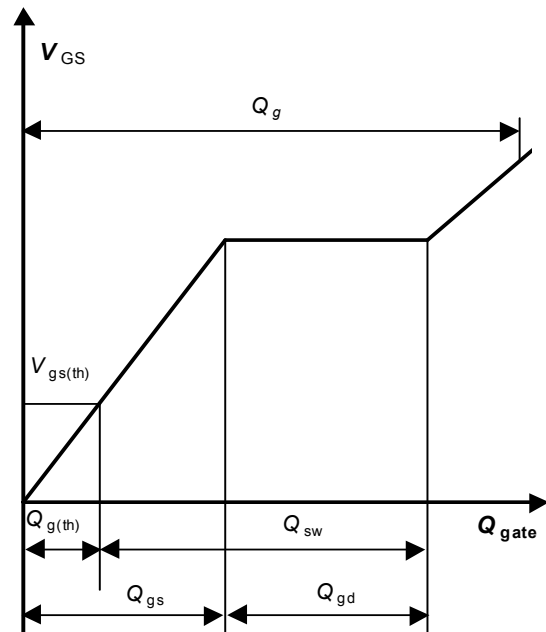


15 Drain-source breakdown voltage

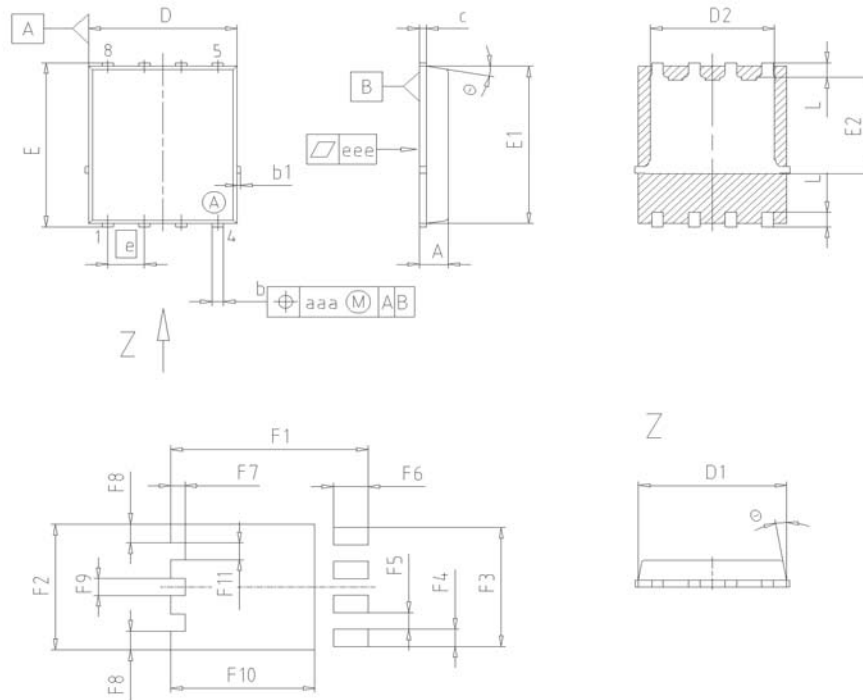
$$V_{BR(DSS)} = f(T_j); I_D = 1 \, \text{mA}$$



16 Gate charge waveforms

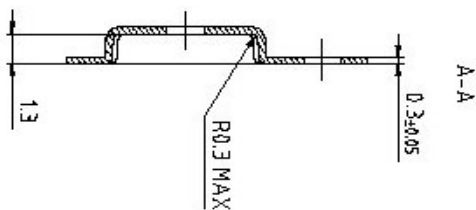


Package Outline: PG-TDSON-8



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.34	0.54	0.013	0.021
b1	0.02	0.22	0.001	0.008
c	0.15	0.35	0.006	0.014
D=D1	4.95	5.35	0.195	0.211
D2	4.20	4.40	0.165	0.173
E	5.95	6.35	0.234	0.250
E1	5.70	6.10	0.224	0.240
E2	3.40	3.80	0.134	0.150
e	1.27		0.050	
L	8		8	
□	0.45	0.65	0.018	0.026
□	8.5°	11.5°	8.5°	11.5°
aaa	0.25		0.010	
eee	0.05		0.002	
F1	6.75	6.95	0.266	0.274
F2	4.60	4.80	0.181	0.189
F3	4.36	4.56	0.172	0.180
F4	0.55	0.75	0.022	0.030
F5	0.52	0.72	0.020	0.028
F6	1.10	1.30	0.043	0.051
F7	0.40	0.60	0.016	0.024
F8	0.60	0.80	0.024	0.031
F9	0.53	0.73	0.021	0.029
F10	4.90	5.10	0.193	0.201
F11	0.53	0.73	0.021	0.029

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