

OptiMOS™ Power-MOSFET

Features

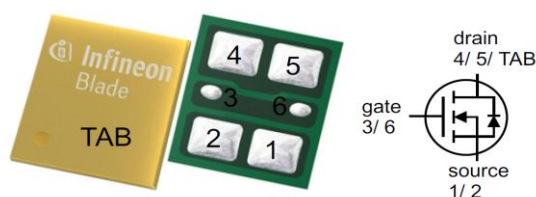
- Optimized for high performance Buck converter
- Very low parasitic inductance
- Low profile (<0.5 mm)
- Double side cooling
- N-channel
- 100% avalanche tested
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Qualified according to JEDEC¹⁾ for target applications



Product Summary

V_{DS}	25	V
$R_{DS(on),max}$	1.1	mΩ
I_D	50	A
Q_{OSS}	32	nC
$Q_G(0V..10V)$	54	nC

LG-USON-6-1



Type	Package	Marking
BSN011NE2LS	LG-USON-6-1	011NE2L

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$	50	A
		$V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$	50	
		$V_{GS}=4.5\text{ V}$, $T_C=25\text{ °C}$	50	
		$V_{GS}=4.5\text{ V}$, $T_C=100\text{ °C}$	50	
		$V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}^{2)}$	33	
Pulsed drain current ³⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	200	
Avalanche current, single pulse ⁴⁾	I_{AS}	$T_C=25\text{ °C}$	50	
Avalanche energy, single pulse	E_{AS}	$I_D=50\text{ A}$, $R_{GS}=25\text{ Ω}$	145	mJ
Gate source voltage	V_{GS}		±20	V

¹⁾ J-STD20 and JESD22

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	$T_c=25\text{ °C}$	78	W
		$T_A=25\text{ °C}$, $R_{\text{thJA}}=50\text{ K/W}^2)$	2.5	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}	bottom	-	-	1.6	K/W
		top	-	-	1	
Device on PCB	R_{thJA}	6 cm ² cooling area ²⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}$, $I_{\text{D}}=1\text{ mA}$	25	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{D}}=250\text{ }\mu\text{A}$	1.2	-	2	
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}}=30\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{\text{DS}}=30\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{\text{GS}}=20\text{ V}$, $V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}$, $I_{\text{D}}=30\text{ A}$	-	1.2	1.5	m Ω
		$V_{\text{GS}}=10\text{ V}$, $I_{\text{D}}=30\text{ A}$	-	0.9	1.1	
Gate resistance	R_{G}		0.3	0.5	1.0	Ω
Transconductance	g_{fs}	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}$, $I_{\text{D}}=30\text{ A}$	85	170	-	S

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See figure 3 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	3900	5200	pF
Output capacitance	C_{oss}		-	1200	1600	
Reverse transfer capacitance	C_{rss}		-	130	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=30\text{ A}, R_{G,ext}=1.6\text{ }\Omega$	-	3.9	-	ns
Rise time	t_r		-	7.8	-	
Turn-off delay time	$t_{d(off)}$		-	29	-	
Fall time	t_f		-	5.2	-	

Gate Charge Characteristics⁵⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	9.3	12	nC
Gate charge at threshold	$Q_{g(th)}$		-	6.2	-	
Gate to drain charge	Q_{gd}		-	6.3	9.5	
Switching charge	Q_{sw}		-	9.3	-	
Gate charge total	Q_g		-	26	35	
Gate plateau voltage	$V_{plateau}$		-	2.4	-	V
Gate charge total	Q_g	$V_{DD}=15\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	54	72	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	22	-	
Output charge	Q_{oss}	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	32	43	

Reverse Diode

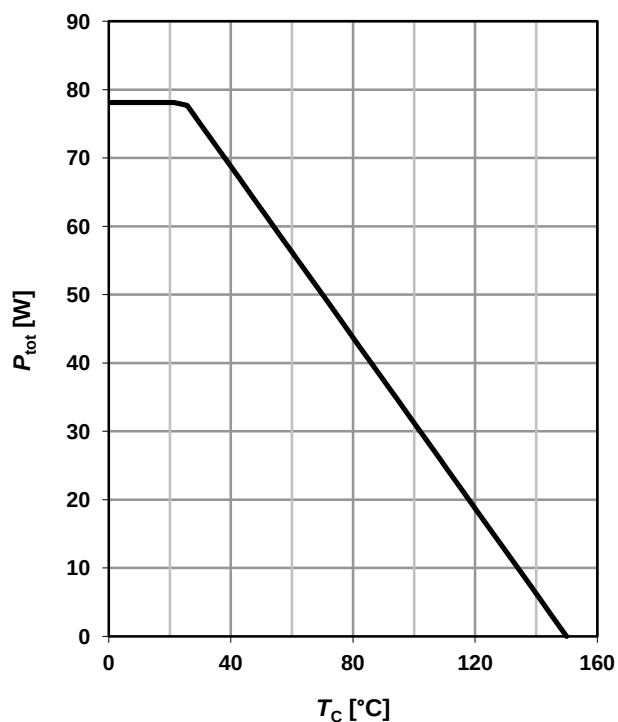
Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	87	A
Diode pulse current	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=30\text{ A},$ $T_J=25\text{ }^\circ\text{C}$	-	0.8	-	V
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	20	-	nC

⁴⁾ See figure 13 for more detailed information

⁵⁾ See figure 16 for gate charge parameter definition

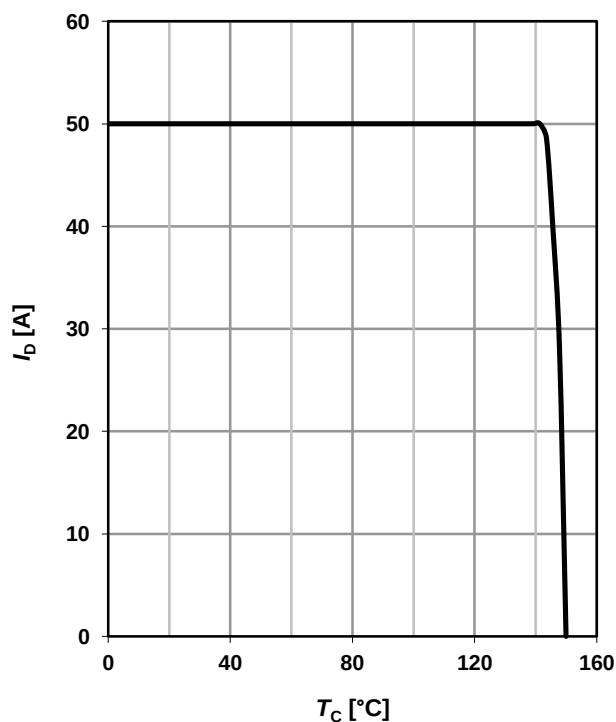
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

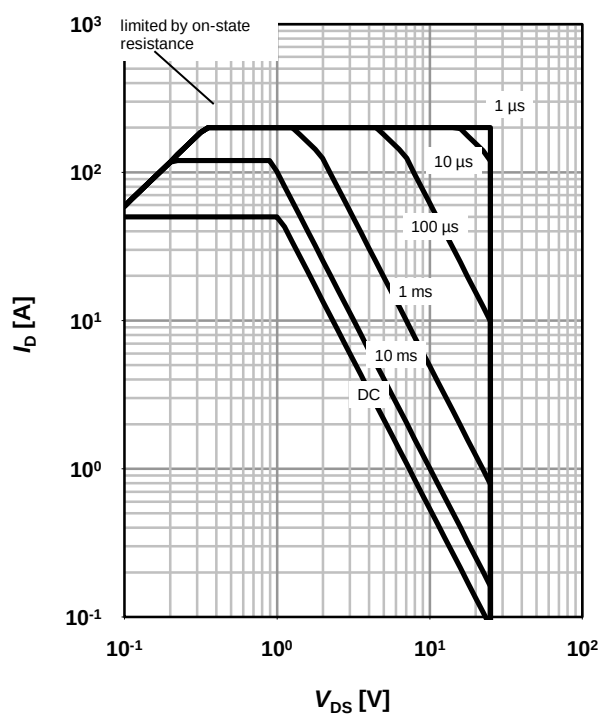
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

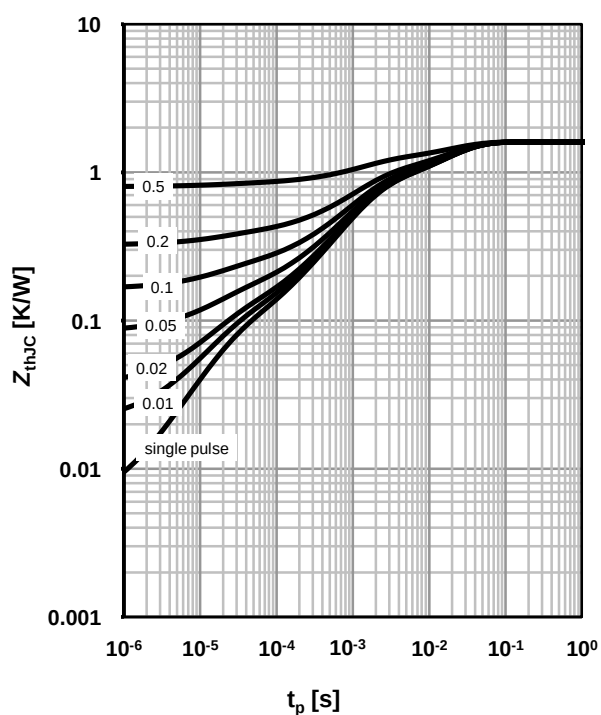
parameter: t_p



4 Max. transient thermal impedance

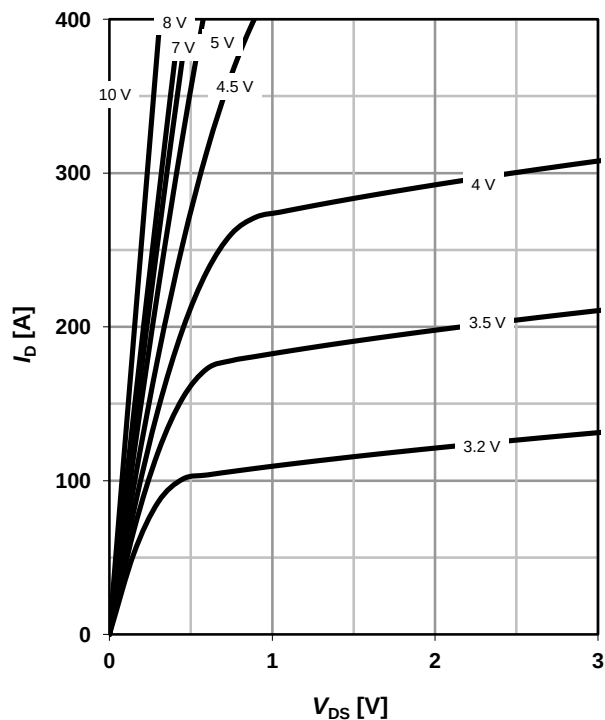
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



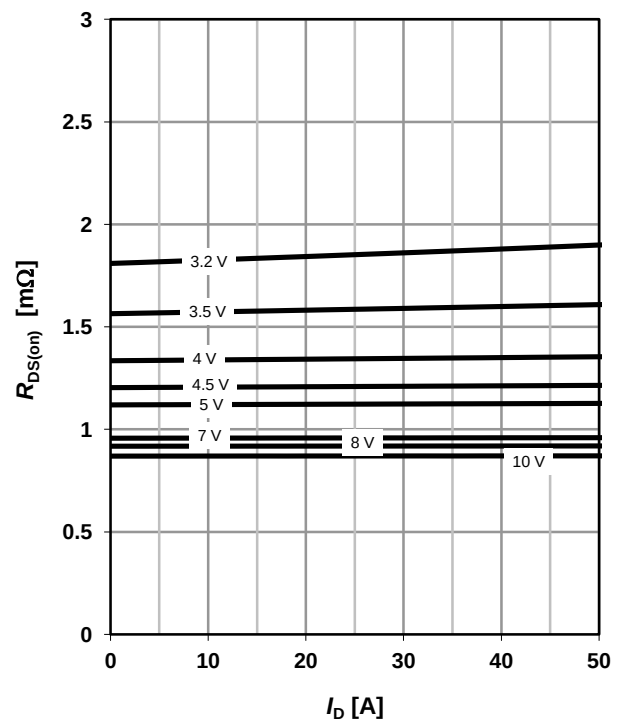
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


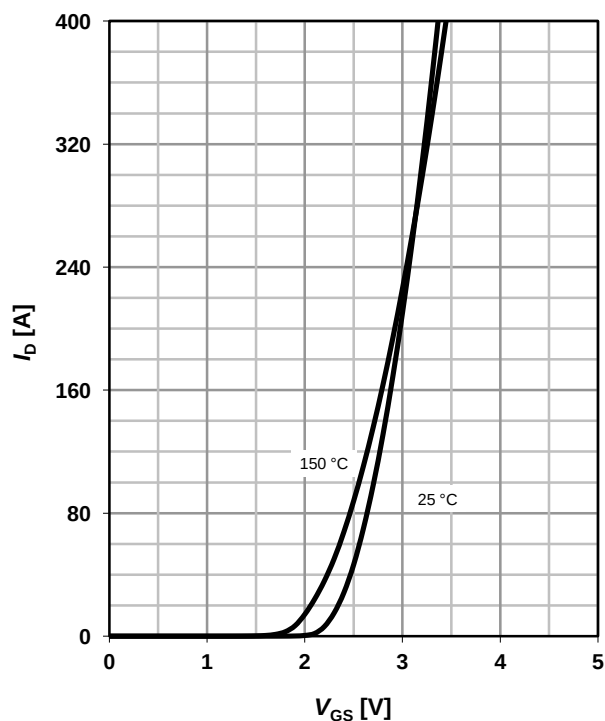
6 Typ. drain-source on resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

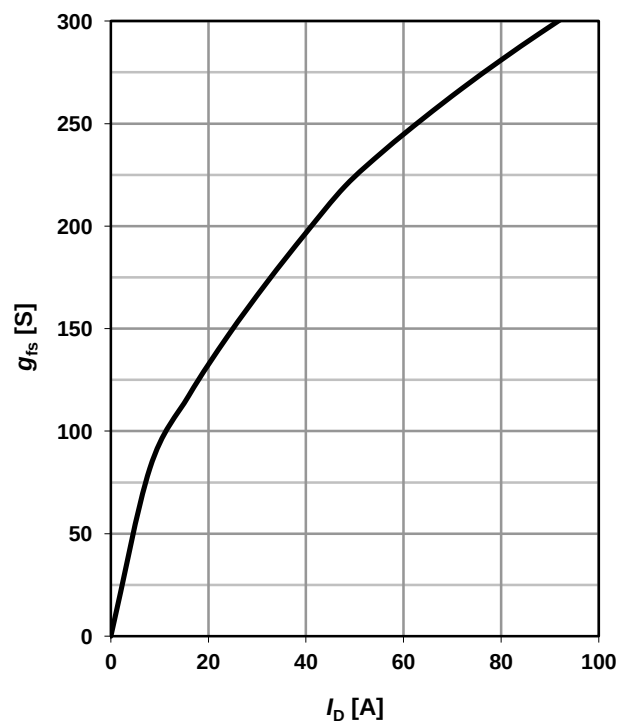
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D| R_{DS(on)max}$

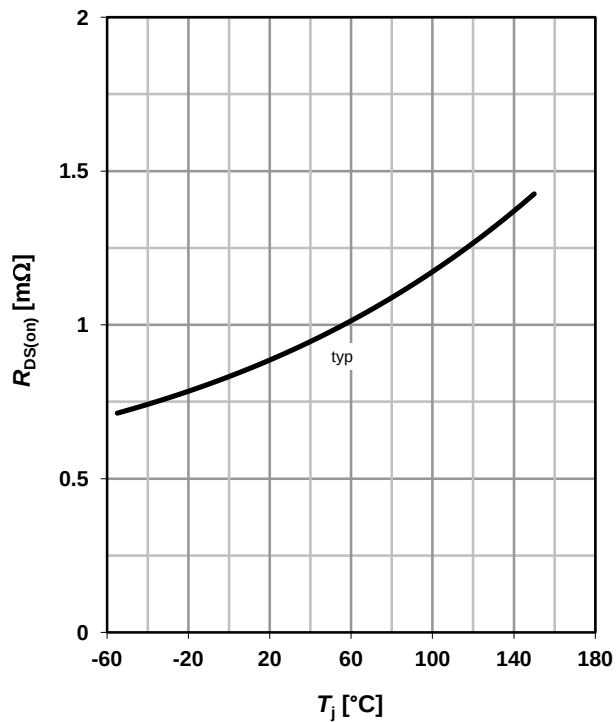
parameter: T_j


8 Typ. forward transconductance

 $g_{fs} = f(I_D); T_j = 25^\circ\text{C}$


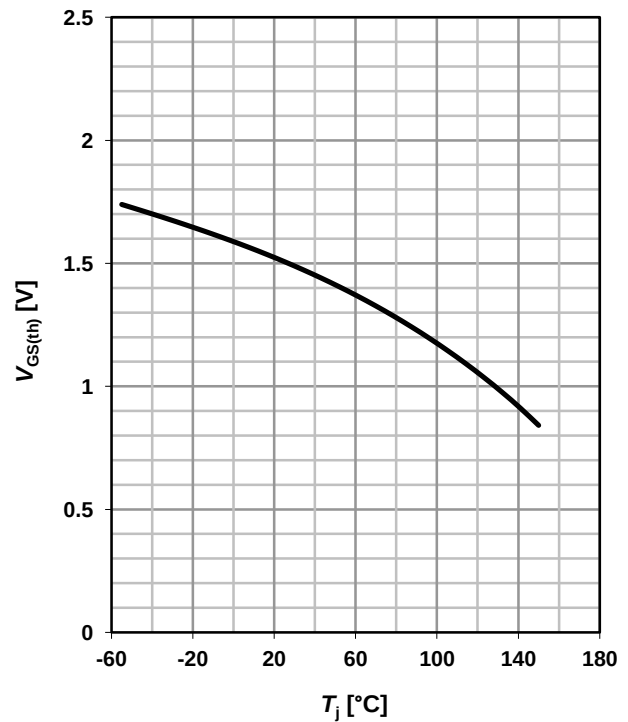
9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}$$



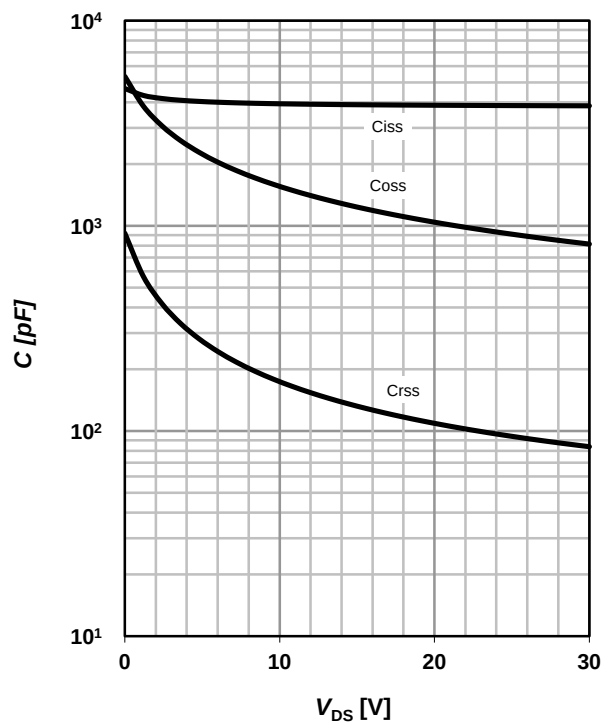
10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 250 \mu\text{A}$$



11 Typ. capacitances

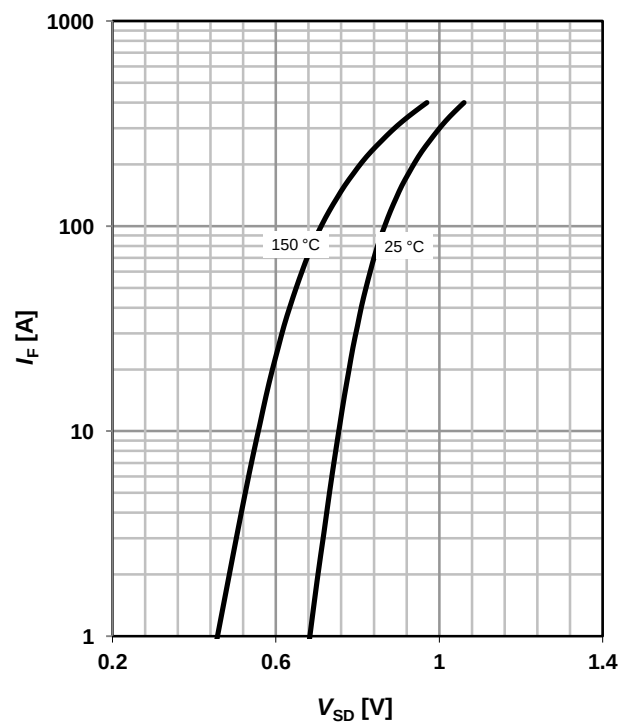
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

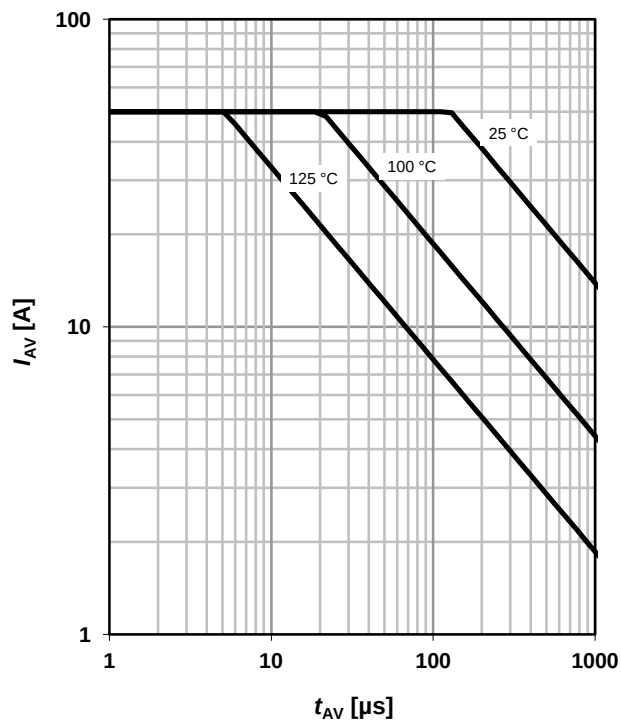
parameter: T_j



13 Avalanche characteristics

$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

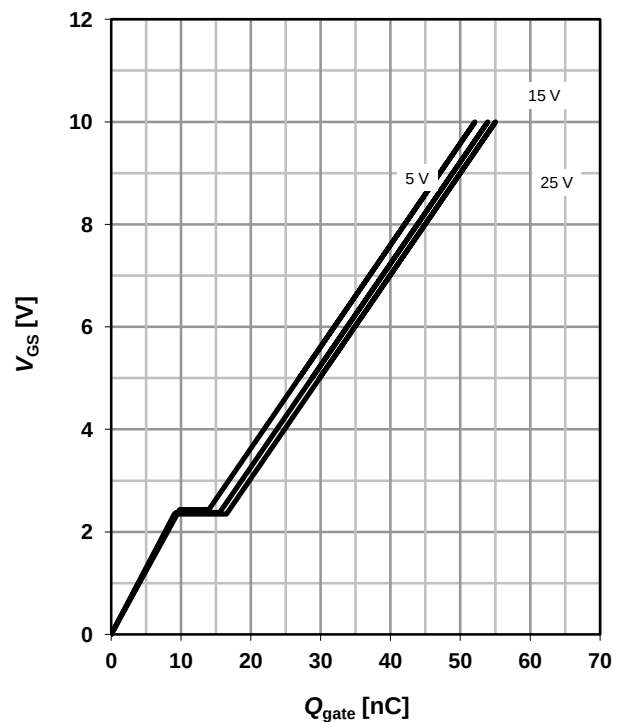
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

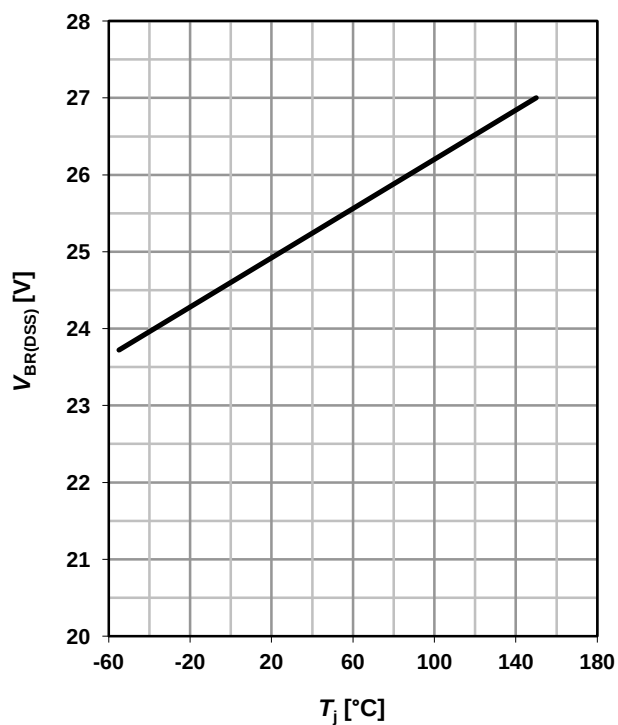
$$V_{GS}=f(Q_{\text{gate}}); I_D=30\ \text{A pulsed}$$

parameter: V_{DD}

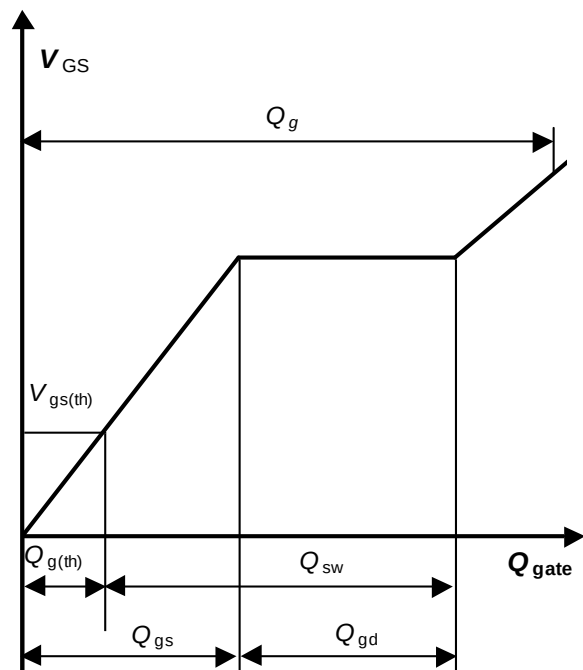


15 Drain-source breakdown voltage

$$V_{BR(DSS)}=f(T_j); I_D=1\ \text{mA}$$



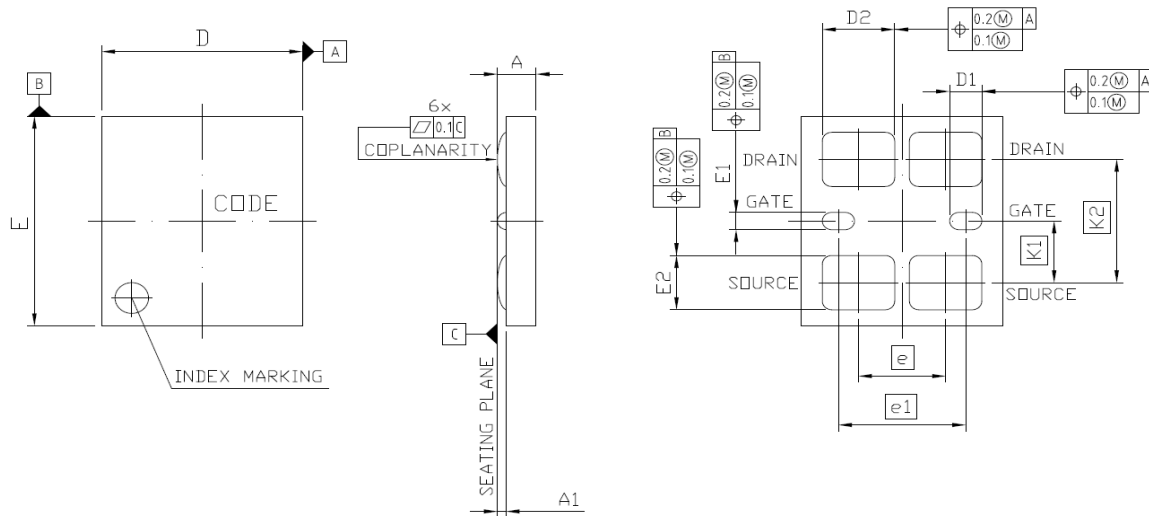
16 Gate charge waveforms



Package Outline

LG-USON-6-1

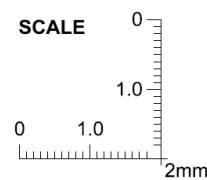
LG-USON-6-1: Outline



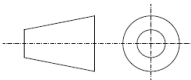
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	0.65	-	0.026
A1	0.08	-	0.003	-
D	2.90	3.10	0.114	0.122
D1	0.38	0.58	0.015	0.023
D2	0.98	1.18	0.039	0.046
e	1.30		0.051	
e1	1.90		0.075	
E	3.30	3.50	0.130	0.138
E1	0.18	0.38	0.007	0.015
E2	0.78	0.98	0.031	0.039
K1	1.00		0.039	
K2	2.00		0.079	

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