

## BSP122-VB Datasheet

### N-Channel 200 V (D-S) MOSFET

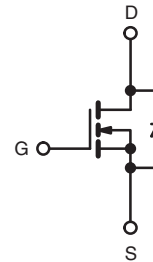
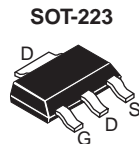
PRODUCT SUMMARY		
$V_{DS}$ (V)	200	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	1.2
$Q_g$ (Max.) (nC)	8.2	
$Q_{gs}$ (nC)	1.8	
$Q_{gd}$ (nC)	4.5	
Configuration	Single	

#### FEATURES

- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	$V_{DS}$	200	V		
Gate-Source Voltage	$V_{GS}$	$\pm 20$			
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25$ °C	1.0	A	
		$T_C = 100$ °C	0.8		
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	5.0	W/°C	
Linear Derating Factor			0.025		
Linear Derating Factor (PCB Mount) <sup>e</sup>			0.017		
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	50	mJ	
Repetitive Avalanche Current <sup>a</sup>		$I_{AR}$	0.96	A	
Repetitive Avalanche Energy <sup>a</sup>		$E_{AR}$	0.31	mJ	
Maximum Power Dissipation		$P_D$	$T_C = 25$ °C	3.1	W
			$T_A = 25$ °C	2.0	
Peak Diode Recovery dV/dt <sup>c</sup>		dV/dt	5.0	V/ns	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	°C	
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s		300		

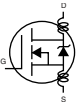
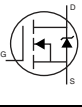
#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 81$  mH,  $R_G = 25$   $\Omega$ ,  $I_{AS} = 0.96$  A (see fig. 12).
- $I_{SD} \leq 3.3$  A,  $dI/dt \leq 70$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	R <sub>thJA</sub>	-	-	40	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	-	60	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

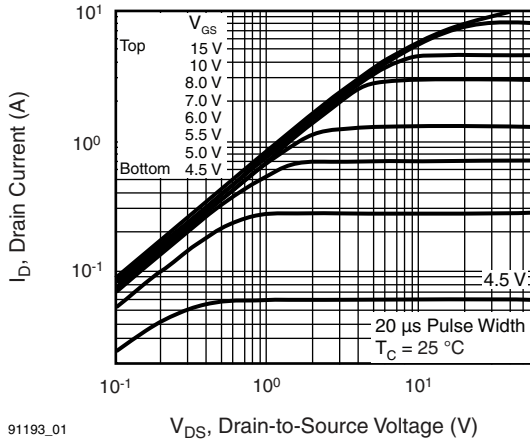
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		200	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.30	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 0.58 A <sup>b</sup>	-	1.2	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 0.58 A		0.51	-	-	S
<b>Dynamic</b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	140	-	pF
Output Capacitance	C <sub>oss</sub>			-	53	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	15	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.3 A, V <sub>DS</sub> = 160 V, see fig. 6 and 13 <sup>b</sup>	-	-	8.2	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	1.8	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	4.5	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 3.3 A, R <sub>g</sub> = 24 Ω, R <sub>D</sub> = 30 Ω, see fig. 10 <sup>b</sup>		-	8.2	-	ns
Rise Time	t <sub>r</sub>			-	17	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	14	-	
Fall Time	t <sub>f</sub>			-	8.9	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L <sub>S</sub>			-	6.0	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	0.96	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	7.7	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 0.96 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	2.0	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.3 A, dI/dt = 100 A/μs <sup>b</sup>		-	150	310	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	0.60	1.4	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

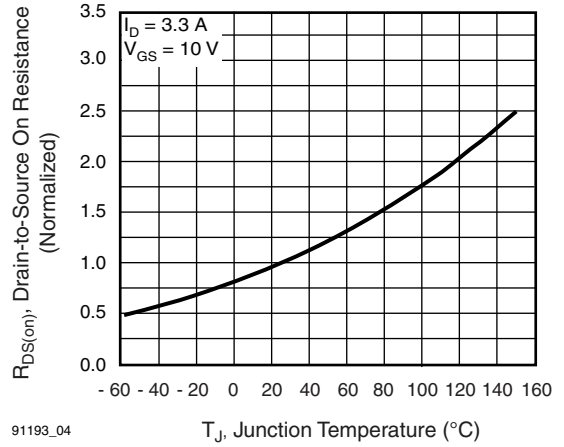
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

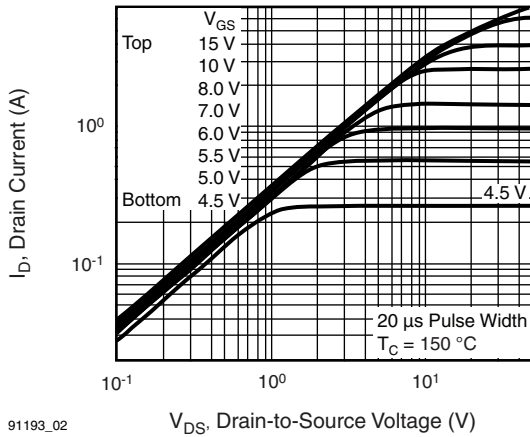
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



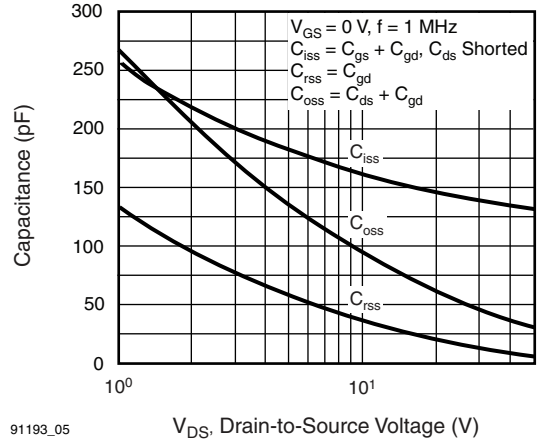
**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$**



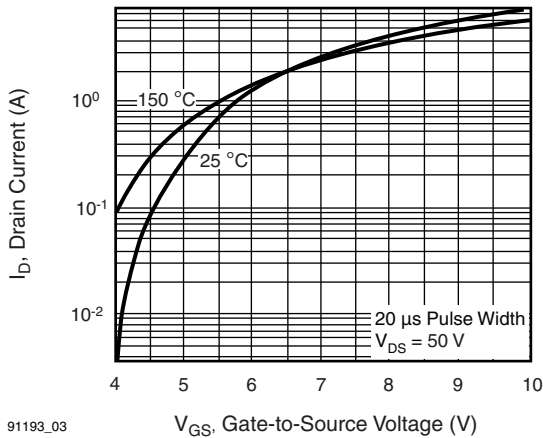
**Fig. 4 - Normalized On-Resistance vs. Temperature**



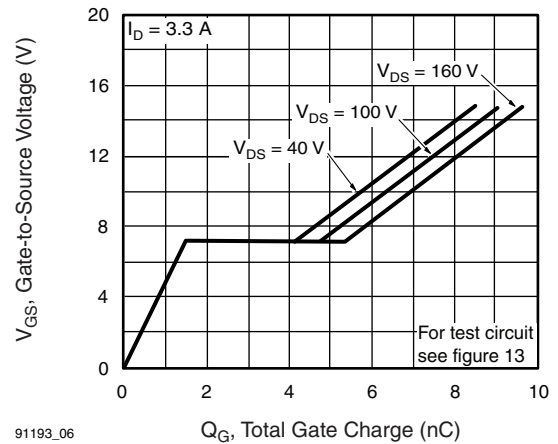
**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$**



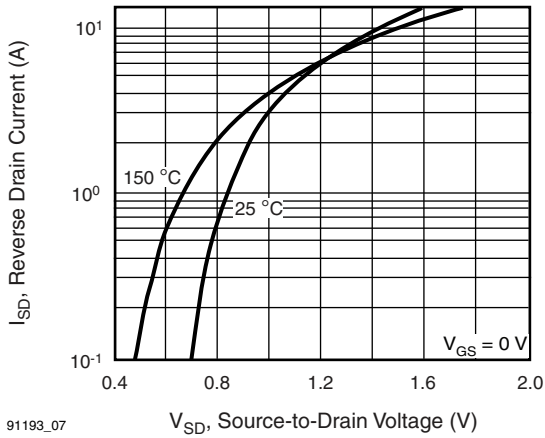
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**

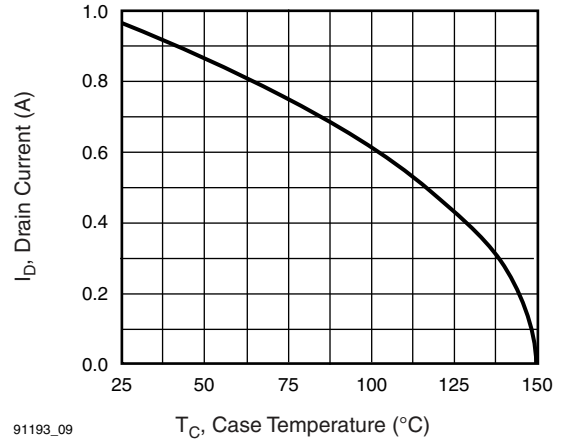


**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



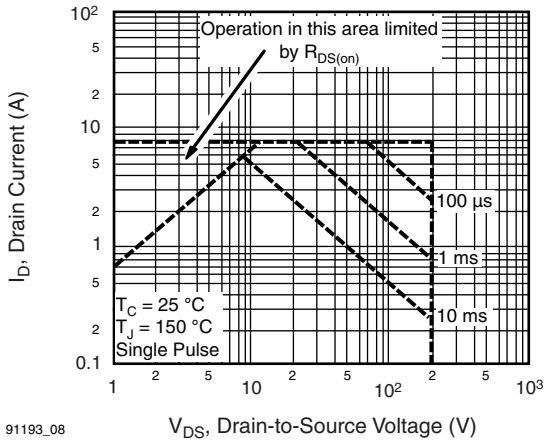
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 9 - Maximum Drain Current vs. Case Temperature



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Fig. 8 - Maximum Safe Operating Area

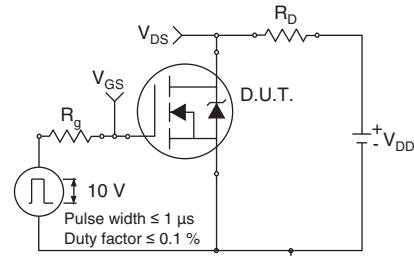


Fig. 10a - Switching Time Test Circuit

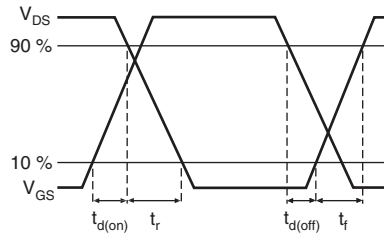
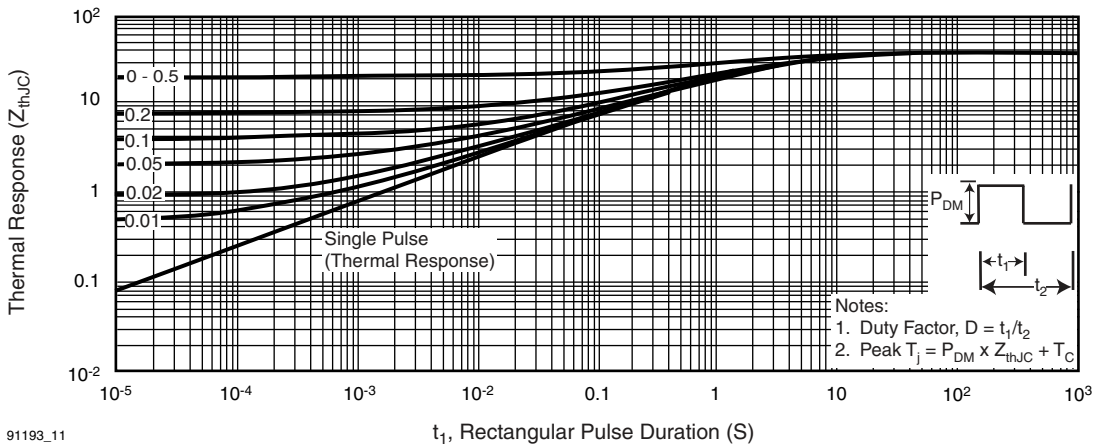


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

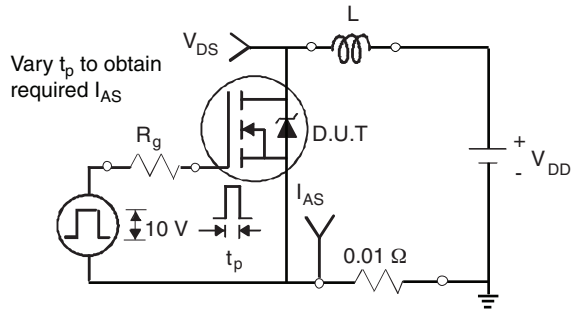


Fig. 12a - Unclamped Inductive Test Circuit

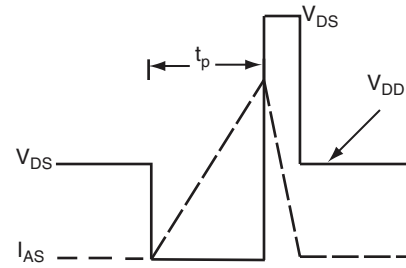
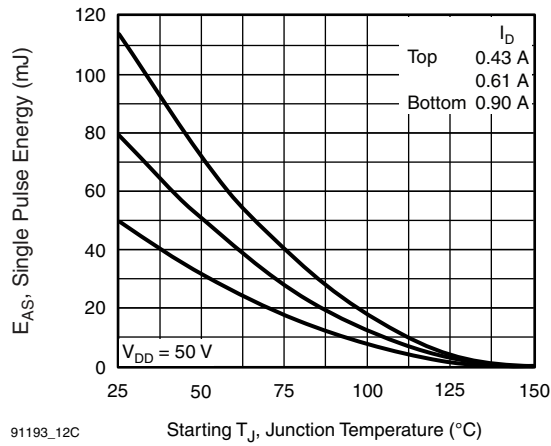


Fig. 12b - Unclamped Inductive Waveforms



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Fig. 12c - Maximum Avalanche Energy vs. Drain Current

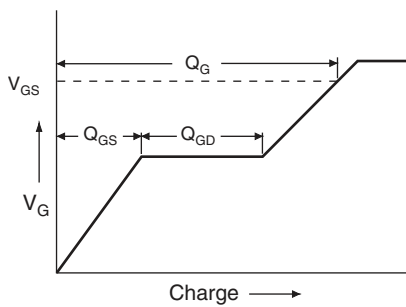


Fig. 13a - Basic Gate Charge Waveform

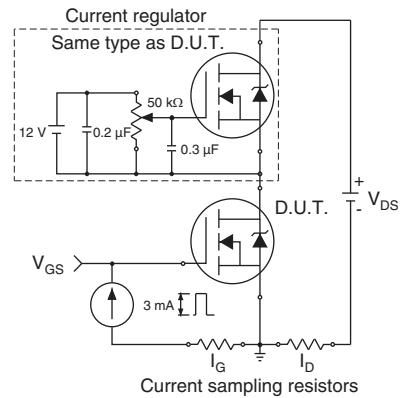
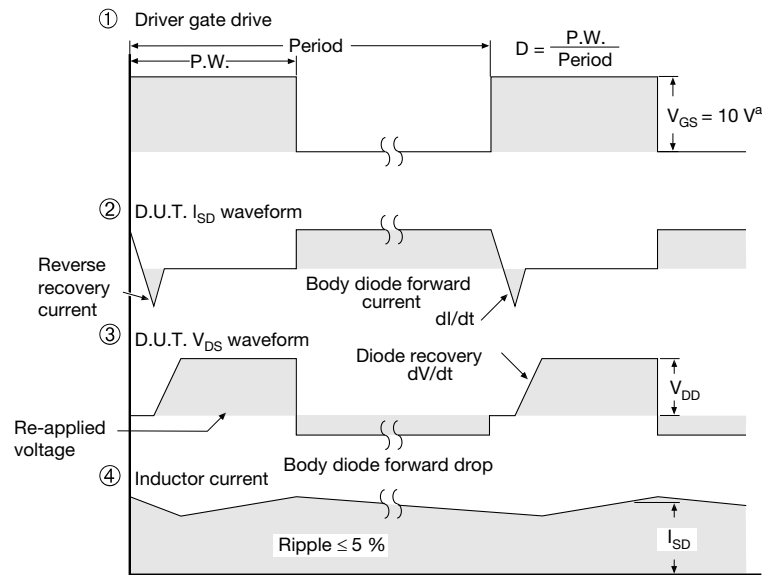
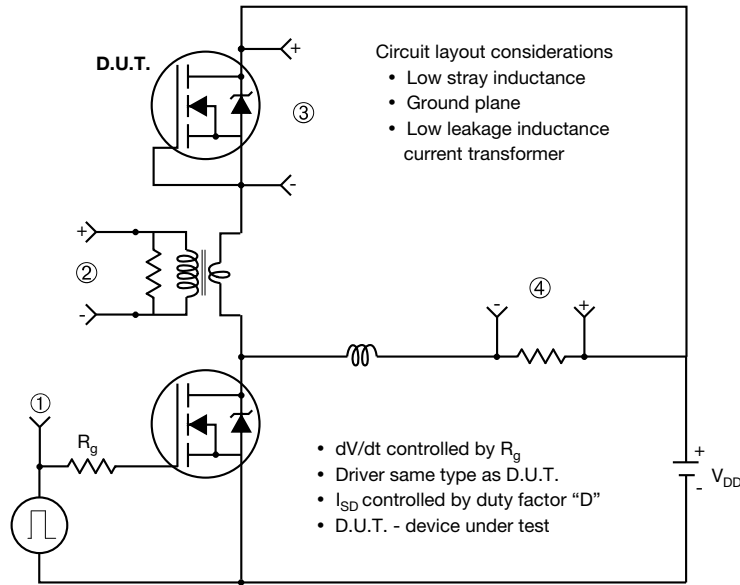


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**

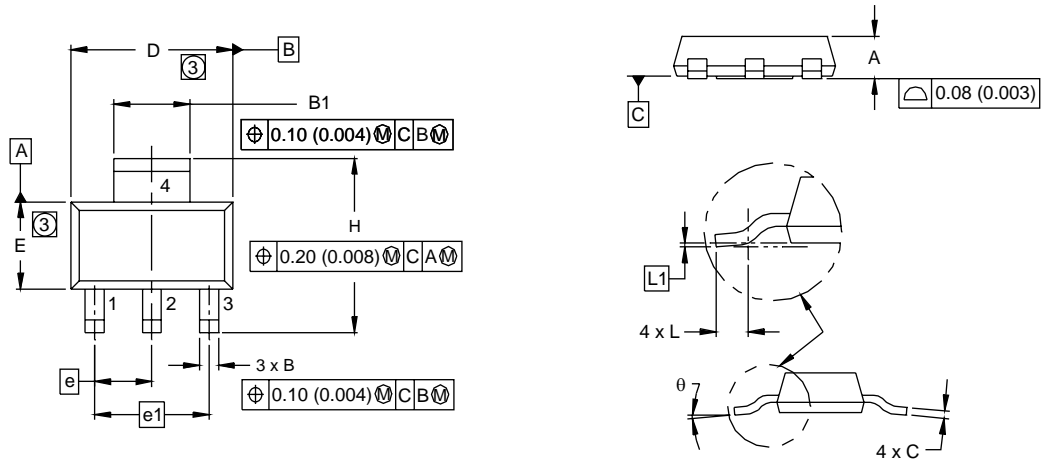


**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

**SOT-223**



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
$\theta$	-	10'	-	10'

ECN: S-82109-Rev. A, 15-Sep-08  
DWG: 5969

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.

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