Ver 1.1

A Scrubbing Circuit for Virtex

Datasheet

Part Number：BSV1

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1.0	2017.8		Initial release.	
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1、 Features

BSV1 is a kind of scrubbing circuit designed to work with SRAM-based FPGA. It supports Virtex platform FPGA such as XQVR300/XQVR600/XQVR1000 produced by Xilinx and BQVR300RH/BQVR300/BQVR600/BQVR1000 produced by BMTI. High reliability radiation hardened technique and triple modular redundancy (TMR) technique is adopted to insure BSV1 accuracy in space.

- **Scrubbing features**
  - The type of the object FPGA can be identified automatically.
  - The scrubed FPGA can adopt two configuration modes：Master serial、Slave serial.
  - JTAG ports are used to operate the scrubbing , more user IOs are reserved compared to use Select MAP ports.
  - Blind scrubbing mode is adopted , covering entire configuration bits except BRAM contents.
  - The operation is user-friend, only one clock and a few control signals are necessary, the connecting relationships among FPGA PROM and BSV1 are explicit and understandable.
  - Supported by Xilinx XC17/ XC18 and XCF serial PROMs
- **Electrical characteristics**
  - 3.3V supply voltage
  - frequency range：1MHz~20MHz
  - Power consumption：100mW under 10MHz frequency
- **Reliability features**
  - Operating temperature：-55℃ ～ +125℃
  - ESD feature（human body model）：2000V
  - Electrical latch up feature：100mA
  - Total ionizing dose：≥100Krad（Si）
  - Single event latch-up threshold：≥75MeV·cm2/mg
  - Single event upset threshold：≥37MeV·cm2/mg

2、 General Description

BSV1 is an ASIC for scrubbing configuration memories in SRAM based FPGAs. BSV1 can scrub Xilinx Virtex serial FPGAs shown as Table 2-1. BSV1 is SEU hardened and SEL immune.

Table 2-1. FPGAs supported by BSV1

Device	Bitstream size(bit)
XQVR300、XQV300	1，751，808
XQVR600、XQV600	3，607，968
XQVR1000、XQV1000	6，127，744
BQVR300	1，751，808
BQVR600	3，607，968
BQVR1000	6，127，744
BQVR300RH	1，751，808

3、 Packages and Pin Function Descriptions

The provided package is: CQFP44.

BSV1 CQFP44 pin configuration is shown in 3-1, the pins are arranged in anticlockwise order.

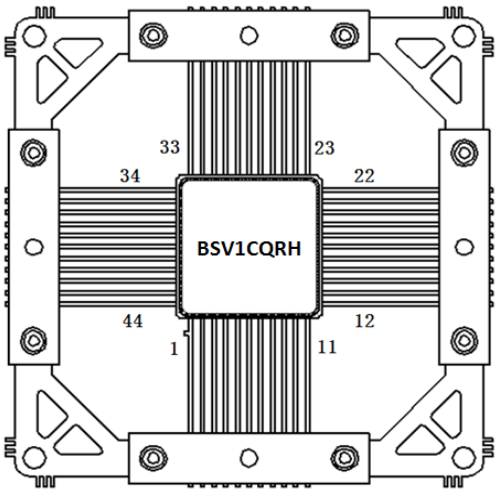


Figure 3-1 CQFP44 pin configuration

Talble 3-1 BSV1 Pin Function Descriptions

Signal name	direction	Function Description	connection
Control signals			
i_clk	I	System clock of BSV1.The entire function is driven by this clock pin, the maximum workable clock speed is 20MHz. A few clocks are necessary for BSV1 to enter the determined state when the chip is powered on, so a continuous and uninterrupted clock is recommended.	To external clock source
i_pause	I	Scrubbing enable signal of BSV1.When the signal is high the chip is workable and can accomplish the FPGA configuration or scrubbing under according to the demand; when the signal is low the chip is standby, all output pins are in high impedance sate, but FPGA configuration still can be performed.	To external control signal
FPGA Configuration Interface			
o_prog_fpga	O	In the procedure of configuration, BSV1 detects Done pin of FPGA. If the Done pin doesn't go high after the anticipated configuration time, it means the configuration is fail, and BSV1 imposes a low pulse on o_prog_fpga to start reconfiguration.	Float or connect to Program pin of FPGA
i_done_fpga	I	This pin is used to detect Done pin of FPGA to determine whether the state machine goes to configuration state or goes to scrubbing state. If Done pin is low, BSV1 goes to configuration state and waits for configuration to be accomplished; if Done pin goes high, BSV1 identifies the type of FPGA and than performs blind scrubbing operation.	connect to Done pin of FPGA

Signal name	direction	Function Description	connection
i_init_fpga	I	This pin is used to detect Initial pin of FPGA. When under configuration state, if the signal is high BSV1 enables the PROM data output and if the signal is low BSV1 disable the PROM data output.	connect to Initial pin of FPGA
o_din_fpga	O	When under configuration state, bit stream is sent to FPGA through this pin. After configuration, the pin is in high impedance state.	connect to Din pin of FPGA
i_cclk_fpga	I	When under configuration state, FPGA sends the configuration clock to BSV1 through this pin.	connect to Cclk pin of FPGA
JTAG Interface			
i_tdo_fpga	I	Dedicated pin, used to perform scrubbing.	connect to TDO pin of FPGA
o_tck_fpga	O	Dedicated pin, used to perform scrubbing.	connect to TCK pin of FPGA
o_tdi_fpga	O	Dedicated pin, used to perform scrubbing.	connect to TDI pin of FPGA
o_tms_fpga	O	Dedicated pin, used to perform scrubbing.	connect to TMS pin of FPGA
PROM Interface			
i_data_prom	I	Source of configuration data and scrubbing data. The PROM content must be generated by Xilinx corresponding tools, and the length of bit stream should keep the default state.	connect to data pin of PROM
o_clk_prom	O	Provide clock signal for PROM.	Connect to CLK pin of PROM
o_oe_prom	O	Provide output enable signal for PROM.	Connect to OE pin of PROM
o_ce_prom	O	Provide chip selct signal for PROM.	Connect to CE pin of PROM
Test purpose interface			

Signal name	direction	Function Description	connection
test1	I	For test purpose only	Connect to GND
test2	I	For test purpose only	Connect to GND
test3	I	For test purpose only	Connect to GND
scan_in	I	For test purpose only	Connect to GND
scan_out	O	For test purpose only	Connect to GND
test_se	I	For test purpose only	Connect to GND
Supply interface			
VCC	I		3.135V~3.465V
GND	I		Connect with GND of FPGA and PROM

4、 Pin List

BSV1-CQFP44 pin list is shown in table 4-1.

Table 4-1 BSV1-CQFP44 pin list

Pin number	Signal symbol	direction	Function description
P1	GND	IN	GND pin
P2	i_clk	IN	System clock
P3	VDD	IN	Supply pin
P4	test1	IN	Test pin
P5	test2	IN	Test pin
P6	GND	IN	GND pin
P7	test3	IN	Test pin
P8	scan_in	IN	Test pin
P9	VDD	IN	Supply pin
P10	scan_out	OUT	Test pin
P11	test_se	IN	Test pin

Pin number	Signal symbol	direction	Function description
P12	VDD	IN	Supply pin
P13	i_done_fpga	IN	Connect to done pin of FPGA
P14	GND	IN	GND pin
P15	o_prog_fpga	OUT	Connect to program pin of FPGA
P16	GND	IN	GND pin
P17	i_init_fpga	IN	Connect to initial pin of FPGA
P18	VDD	IN	Supply pin
P19	GND	IN	GND pin
P20	o_din_fpga	OUT	Connect to din pin of FPGA
P21	VDD	IN	Supply pin
P22	i_cclk_fpga	IN	Connect to cclk pin of FPGA
P23	GND	IN	GND pin
P24	o_tms_fpga	OUT	Connect to tms pin of FPGA
P25	VDD	IN	Supply pin
P26	GND	IN	GND pin
P27	o_tdi_fpga	OUT	Connect to tdi pin of FPGA
P28	VDD	IN	Supply pin
P29	GND	IN	GND pin
P30	o_tck_fpga	OUT	Connect to tck pin of FPGA
P31	VDD	IN	Supply pin
P32	i_tdo_fpga	IN	Connect to tdo pin of FPGA
P33	GND	IN	GND pin
P34	GND	IN	GND pin
P35	i_data_prom	IN	Connect to data pin of PROM
P36	VDD	IN	Supply pin
P37	o_clk_prom	OUT	Connect to clk pin of PROM
P38	VDD	IN	Supply pin
P39	GND	IN	GND pin
P40	o_oe_prom	OUT	Connect to oe pin of PROM
P41	VDD	IN	Supply pin
P42	o_ce_prom	OUT	Connect to ce pin of PROM
P43	GND	IN	GND pin

Pin number	Signal symbol	direction	Function description
P44	i_pause	IN	Pause control

5、 Detailed Description

5.1 Function Description

BSV1 is classified as aerospace grade product, which provides a timely scrubbing solution to mitigate single event upset(SEU) happened in space application SRAM FPGAs. The BSV1 chip significantly reduces the degree of difficulty and complexity in designing scrubbing system. BSV1 can scrub Xilinx Virtex serial FPGAs, as well as the BMTI fully compatible aerospace grade FPGAs. The chips supported by BSV1 are shown in table 5-1, but the FPGAs or PROMs not listed here are not supported.

Table 5-1 List of supported devices

FPGA Device	Number of configuration bits
XQVR300、XQV300	1，751，808
XQVR600、XQV600	3，607，968
XQVR1000、XQV1000	6，127，744
BQVR300	1，751，808
BQVR600	3，607，968
BQVR1000	6，127，744
BQVR300RH	1，751，808
XQ17V platform PROM (produced by Xilinx)	1、2、4、8、16M
XQ18V platform PROM (produced by Xilinx)	512K、1M、2M、4M
XCF platform PROM (produced by Xilinx)	1、2、4、8、16、32M
BQ18V04 (produced by BMTI)	4 M

The main functions of BSV1 are as follows:

1) FPGA configuration

After power on, BSV1 serially reads the configuration data from PROM, and puts the data on FPGA D0 pin straight away. The FPGA could be master serial mode or slave serial mode. The time token to configure FPGA through BSV1 is the same as

to configure FPGA directly with PROM.

2) Read back IDcode

After configuration, BSV1 reads back FPGA IDcode through JTAG ports. According to the acquired IDcode, BSV1 settles the parameter of scrubbing operation such as the length of scrubbing data.

3) Scrubbing configuration memory

After the FPGA IDcode is identified, BSV1 reads the configuration data from PROM, the data is processed to generate JTAG format scrubbing data. The scrubbing data refreshes the configuration memory except the BRAM content over and over again. The user function is not affected by the scrubbing operation if only SRL16 and LUTRAM are not used in the design.

4) Control signal descriptions

BSV1 is controlled by two pins: i_clk(clock pin),i_pause(enable pin). All signals of BSV1 are synchronized by i_clk, whose frequency range should be 0MHz to 20MHz and duty cycle should be 50%. The clock is recommended to constantly supply, so the scrubbing will be stable. If the user needs to pause the scrubbing, it will be realized by pulling down i_pause pin at any time, BSV1 will continue the current scrubbing, and finishing the entire cycle, than will go to standby state, all output pins will be in high impedance state; if the user needs to resume the scrubbing, just pull up i_pause pin at any time, and BSV1 will start to work.

5) Scrubbing period

The period of scrubbing is related to the size of bit stream and the clock frequency. The period calculation formula is :

T= size of bit stream× clock period ×2

The typical scrubbing periods are shown in table 5-2.

Table 5-2 BSV1 scrubbing period

Device	Size of bit stream	Clock frequency	Scrubbing period
BQV300RH XQVR300、BQVR300、	1，751，808	10 MHz	About 350 ms
XQVR600、BQVR600	3，607，968	10 MHz	About 720 ms
XQVR1000,BQVR1000	6，127，744	10 MHz	About 1.2 s

5.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 10℃～30℃ and relative humidity less than 70%. There should be no acid , alkali or other radiant gas in the environment,

5.3 Absolute Maximum Ratings

a) Supply voltage range to ground potential（V_{DD}）： -0.5 V ～3.6V
b) DC input voltage range（V_{in}）： -0.5 V ～3.6V
c) Storage temperature（T_{stg}）： -65℃～ 150℃
d) Lead temperature（T_h）： 260℃
e) Power dissipation（P_D）： 0.1W
f) Maximum frequency（fmax）： 20MHz

5.4 Recommended Operation Conditions

a) Supply voltage relative to ground（VDD）： 3.135V~3.465V
b) Case operation temperature range(TA) ： -55℃~125℃
c) Operation frequency（f）： 10MHz
d) Input low voltage range (V_{IL}) ： 0V~0.8V
e) Input hign voltage range (V_{IH}) ： 2V~3.465V

6、 Specifications

All electrical characteristics are shown in table 6-1.

Table 6-1 BSV1 electrical characteristics

Test	Symbol	Conditions （-55℃≦ T_A≤ 125℃ 3.135V≤V_{DD}≤3.465V）	Llimits		units
			min	max	
Output high voltage	V_{OH}	V_{DD}=3.135V， I_{OH}=-12 mA	2.4	—	V
Output low voltage	V_{OL}	V_{DD}=3.135V， I_{OL}=12 mA	—	0.4	V

Input high voltage	V_{IH}	V_{DD}=3.3V	2.0	—	V
Input low voltage	V_{IL}	V_{DD}=3.3V	—	0.8	V
Input high leakage current	I_{IH}	V_{DD}=3.465V，test i_cclk_fpga 、i_clk 、i_pause、i_data_prom 、i_done_fpga 、i_init_fpga、 i_tdo_fpga (don't test the pad with a pull down resistor)	—	0.6	nA
			—	1	μA
			—	1	μA
Input low leakage current	$\lvert I_{IL} \rvert$	V_{DD}=3.465V，test i_init_fpga、i_cclk_fpga、i_tdo_fpga、i_data_prom、i_paus、i_clk、test1、test2、test3、scan_in、test_se、i_done_fpga(don't test the pad with a pull up resistor)	—	0.6	nA
			—	1	μA
			—	1	μA
Quiescent supply current	I_{DDS}	V_{DD}=3.465V	—	2	mA
				3	mA
				1	mA
Input output capacitance	$C_{in/out}$	f=1.0MHz, T_A =25℃	—	15	pF
Function test	—	f =10MHz/20MHz	—	—	—
Output delay: o_tck_fpga relative to i_clk	t_{c2d_tck}	V_{DD}=3.125V, f =10MHz	—	30	ns
Output delay: o_tms_fpga relative to i_clk	t_{c2d_tms}		—	30	ns
Output delay: o_tdi_fpga relative to i_clk	t_{c2d_tdi}		—	30	ns

Output delay: o_din_fpga relative to i_data_prom	t_{dd}		—	30	ns

7、 Package Specifications

The specifications of CQFP44 package are shown in figure 7-1.

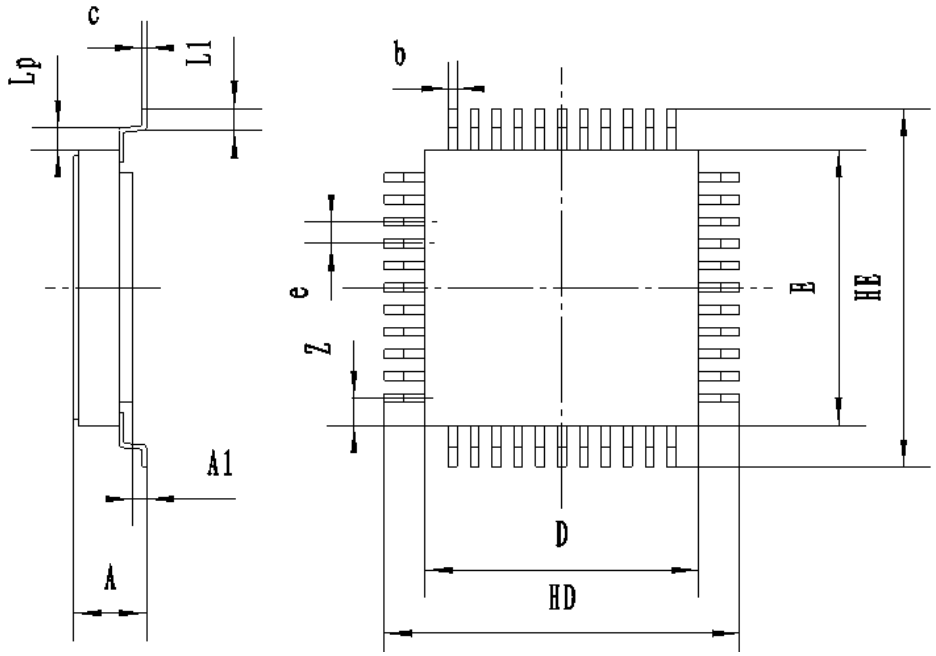


Figure 7-1 CQFP44 package specifications

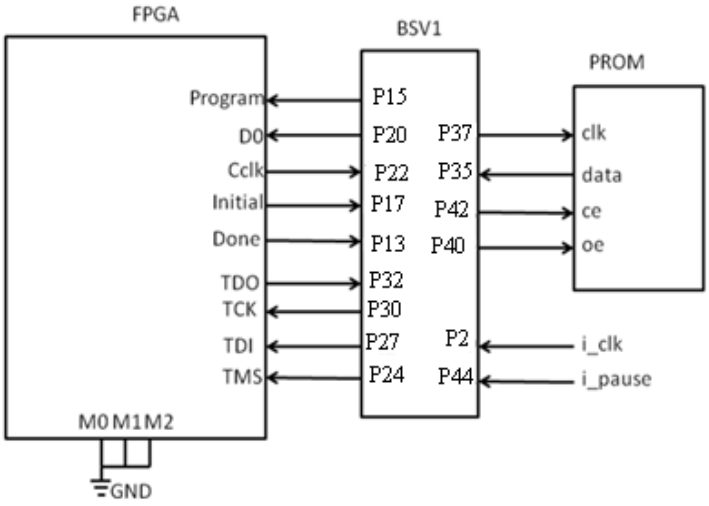
Table 7-1 size symbol list

Size symbol	Value （unit：mm）		
	min	typical	max
A	2.9		4.0
A1	0.50	0.75	1.01
b		0.32	
c		0.15	
e		0.8	
Z		1.0	
D/E	9.80	10	10.20
HD/HE	14.20	15	15.65

Lp	1.0	1.0	1.15
L1	1.25	1.5	1.75

8、 Appendix I Typical Application Example

BSV1 can configure FPGA in serial mode and scrub FPGA in JTAG mode. BSV1 is placed between FPGA and configuration PROM , it works as a data Exchange Bridge. Master serial mode is shown in appendix figure 8-1. Where the FPGA pins program and initial are pulled up with 4.7KΩ resistance, done pin is pulled up with 330Ω resistance. Slave serial mode is similar, the difference is the CCLK source isn't FPGA but some external device.



Appendix figure 8-1 master serial configuration mode

Attentions：

- The signal i_clk should connect to active clock source, the clock frequency should below 20MHz(room temperature). When the temperature is high , frequency should be reduced , 10MHz is recommended.
- Configuration bit stream and the PROM mcs format file should be generated by a Xilinx software.
- Because BSV1 will use the JTAG ports when it work , the JTAG chain of FPGA and PROM should be independent ,in case the tdo pin of PROM may disturb the scrubbing operation.
- The i_done_fpga pin must not connect to diode, in case the voltage of pin i_done_fpga is pulled down. If the voltage loss did happened, BSV1 may

reconfigure FPGA, which is unexpected.

Taboo issues：

- Keep the default size of bit stream; do not use any options that could change the default size, such as bit compression.
- Do not use disable readback option or disable reconfiguration option in ISE.
- Do not use LUT-RAM or LUT-shifter, unless enable i_half signal.

The influence on FPGA:

- The first configuration time after power on: unchanged
- Influence on user function：none
- The core supply current is increased when scrubbing.

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