Ver 1.1

A Scrubbing Circuit for Virtex2

Datasheet

Part Number：BSV2CQRH

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1. Features

- **Scrubbing features**
  - The type of the object FPGA can be identified automatically
  - The scrubbed FPGA can adopt two configuration modes：Master serial、Slave serial
  - JTAG ports are used to operate the scrubbing，more user IOs are reserved compared to use Select MAP ports.
  - Blind scrubbing mode is adopted，covering entire configuration bits except BRAM contents.
  - POR SEFI can be repaired automatically.
  - The operation is user-friend，only one clock and a few control signals are necessary, the connecting relationships among FPGA PROM and BSV2CQRH are explicit and understandable.
  - Supported by Xilinx XC17 XC18 and XCF serial PROMs
- **Electrical characteristics**
  - 3.3V supply voltage
  - frequency range：1MHz~20MHz
  - Power consumption：400mW under 10MHz frequency
- **Reliability features**
  - Operating temperature：-55℃ ～ +125℃
  - ESD feature（human body model）：2000V
  - Electrical latch up feature：200mA
  - Total ionizing dose：≥100Krad（Si）
  - Single event latch-up threshold：≥75MeV·cm2/mg
  - Single event upset threshold：≥37MeV·cm2/mg

2. General Description

BSV2CQRH is an ASIC for scrubbing configuration memories in SRAM based FPGAs. BSV2CQRH can scrub Xilinx Virtex2 serial FPASs XQR2V1000, XQR2V3000, XQR2V6000, as well as the BMTI fully compatible aerospace grade FPGAs BQR2V1000, BQR2V3000, BQR2V6000. BSV2CQRH is SEU hardened and SEL immune.

3. Function Block Diagram

BSV2CQRH function block diagram is shown in figure 3-1.

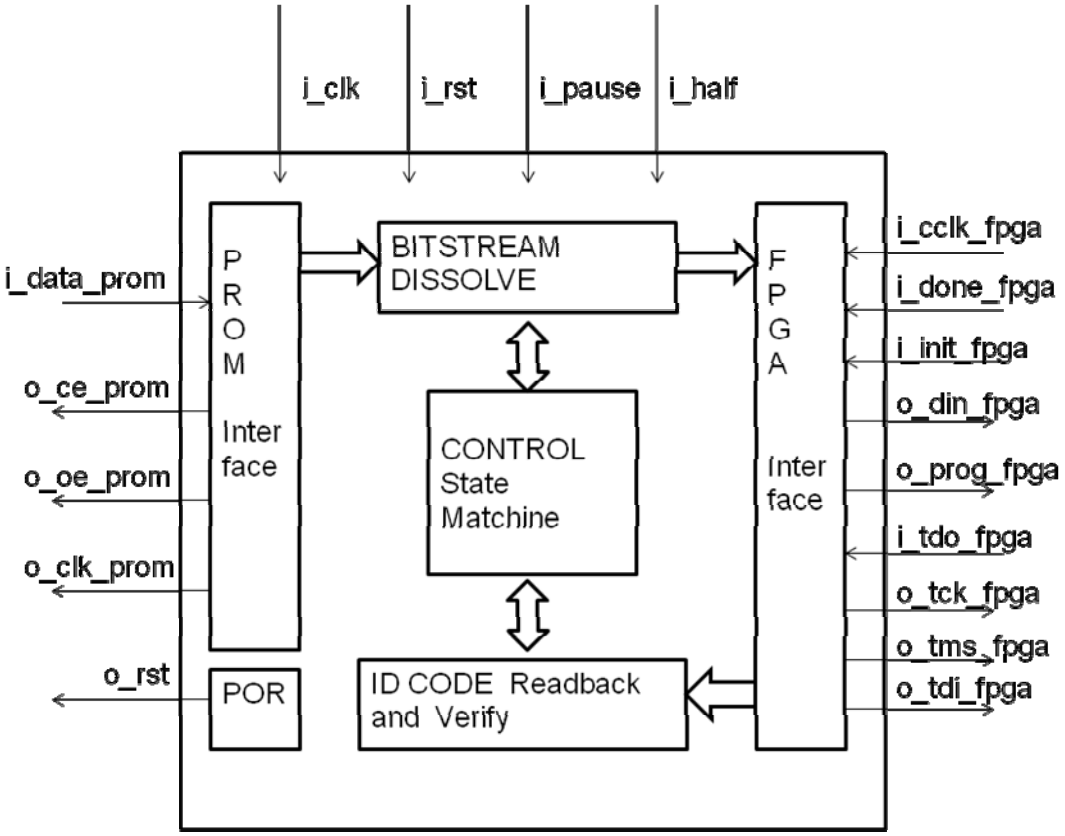


Figure 3-1 BSV2CQRH function block digram

4. Packages and Pin Function Descriptions

The provided package is: CQFP48.

BSV2CQRH CQFP48 pin configuration is shown in 4-1, in top view the pin P1 is in the middle of the left side, the pins are arranged in anticlockwise order.

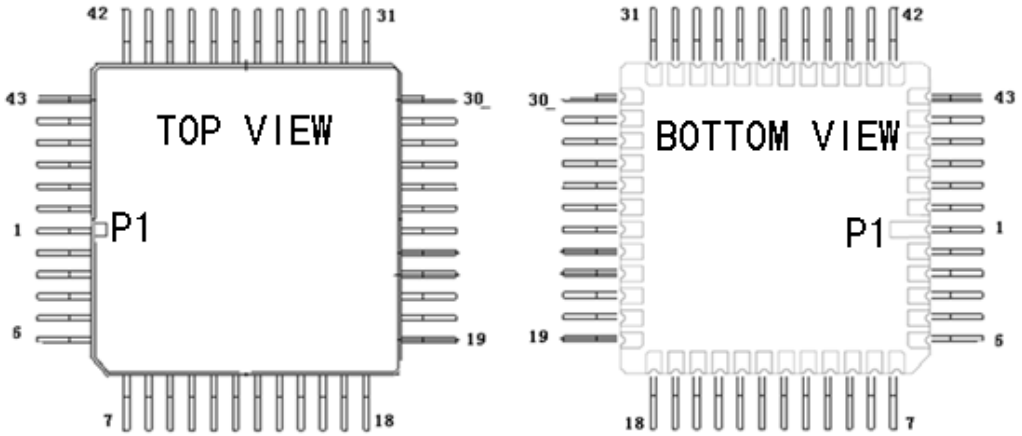


Figure 4-1 CQFP48 pin configuration

Talble 4-1 BSV2CQRH Pin Function Descriptions

Signal name	direction	Function Description	connection
Control signals			
i_clk	I	System clock of BSV2CQRH.The entire function is driven by this clock pin, the maximum workable clock speed is 20MHz. A few clocks are necessary for BSV2CQRH to enter the determined state when the chip is powered on, so a continuous and uninterrupted clock is recommended.	To external clock source
i_pause	I	Scrubbing enable signal of BSV2CQRH.When the signal is high the chip is workable and can accomplish the FPGA configuration or scrubbing under according to the demand; when the signal is low the chip is standby, all output pins are in high impedance sate, but FPGA configuration still can be performed.	To external control signal
i_rst	I	Reset signal of BSV2CQRH, active low, when it is active, BSV2CQRH returns to configuration state, and the chip only performs FPGA	To external control signal

Signal name	direction	Function Description	connection
		configuration function.	
i_half	I	Control signal of BSV2CQRH, active low, when it is active, BSV2CQRH only scrubs the left half part of FPGA configuration memories, and when it is invalid BSV2CQRH scrubs the whole FPGA.	To external control signal
o_rst	O	The signal indicates if the chip is reset or not. The low level shows BSV2CQRH is reset, while the high level shows BSV2CQRH is not reset.	
FPGA Configuration Interface			
o_prog_fpga	O	In the procedure of configuration, BSV2CQRH detects Done pin of FPGA. If the Done pin doesn't go high after the anticipated configuration time, it means the configuration is fail, and BSV2CQRH imposes a low pulse on o_prog_fpga to start reconfiguration. In the procedure of scrubbing, BSV2CQRH detects Done pin of FPGA as well. If the Done pin turns to low level, it means the POR SEFI occurred, and BSV2CQRH imposes a low pulse on o_prog_fpga to start reconfiguration. If BSV2CQRH is used in 2V6000 scrubbing， this pin shall not connect with 2V6000.	Float or connect to Program pin of FPGA
i_done_fpga	I	This pin is used to detect Done pin of FPGA to determine whether the state machine goes to configuration state or goes to scrubbing state. If Done pin is low, BSV2CQRH goes to configuration state and waits for configuration to be accomplished; if Done pin goes high, BSV2CQRH identifies the type of FPGA and than performs blind scrubbing operation.	connect to Done pin of FPGA
i_init_fpga	I	This pin is used to detect Initial pin of FPGA. When under configuration state, if the signal is	connect to Initial pin of FPGA

Signal name	direction	Function Description	connection
		high BSV2CQRH enables the PROM data output and if the signal is low BSV2CQRH disable the PROM data output.	
o_din_fpga	O	When under configuration state, bit stream is sent to FPGA through this pin. After configuration, the pin is in high impedance state.	connect to Din pin of FPGA
i_cclk_fpga	I	When under configuration state, FPGA sends the configuration clock to BSV2CQRH through this pin.	connect to Cclk pin of FPGA
JTAG Interface			
i_tdo_fpga	I	Dedicated pin, used to perform scrubbing.	connect to TDO pin of FPGA
o_tck_fpga	O	Dedicated pin, used to perform scrubbing.	connect to TCK pin of FPGA
o_tdi_fpga	O	Dedicated pin, used to perform scrubbing.	connect to TDI pin of FPGA
o_tms_fpga	O	Dedicated pin, used to perform scrubbing.	connect to TMS pin of FPGA
PROM Interface			
i_data_prom	I	Source of configuration data and scrubbing data. The PROM content must be generated by Xilinx corresponding tools, and the length of bit stream should keep the default state.	connect to data pin of PROM
o_clk_prom	O	Provide clock signal for PROM.	Connect to CLK pin of PROM
o_oe_prom	O	Provide output enable signal for PROM.	Connect to OE pin of PROM
o_ce_prom	O	Provide chip selct signal for PROM.	Connect to CE pin of PROM
Test purpose interface			
test1	I	For test purpose only	Connect to GND
test2	I	For test purpose only	Connect to GND

Signal name	direction	Function Description	connection
test3	I	For test purpose only	Connect to GND
scan_en	I	For test purpose only	Connect to GND
Supply interface			
VCC	I		3.135V~3.465V
GND	I		Connect with GND of FPGA and PROM

5. Pin List

BSV2CQRH-CQFP48 pin list is shown in table 5-1.

Table 5-1 BSV2CQRH-CQFP48 pin list

Pin Number	Signal symbol	Direction	Function Description
P1	o_oe_prom	OUT	Connect to oe pin of PROM
P2	VDD	IN	Supply pin
P3	o_ce_prom	OUT	Connect to ce pin of PROM
P4	i_pause	IN	Pause control
P5	GND	IN	GND pin
P6	VDD	IN	Supply pin
P7	VDD	IN	Supply pin
P8	GND	IN	GND pin
P9	i_clk	IN	System clock
P10	test1	IN	Test pin
P11	test2	IN	Test pin
P12	GND	IN	GND pin
P13	test3	IN	Test pin
P14	scan_en	IN	Test pin
P15	VDD	IN	Supply pin
P16	o_rst	OUT	Reset output pin
P17	i_rst	IN	External reset pin

Pin Number	Signal symbol	Direction	Function Description
P18	GND	IN	GND pin
P19	VDD	IN	Supply pin
P20	GND	IN	GND pin
P21	i_done_fpga	IN	Connect to done pin of FPGA
P22	i_half	IN	Half scrub mode select pin
P23	o_prog_fpga	OUT	Connect to program pin of FPGA EXCEPT 2V6000
P24	i_init_fpga	IN	Connect to initial pin of FPGA
P25	VDD	IN	Supply pin
P26	GND	IN	GND pin
P27	o_din_fpga	OUT	Connect to din pin of FPGA
P28	i_cclk_fpga	IN	Connect to cclk pin of FPGA
P29	GND	IN	GND pin
P30	VDD	IN	Supply pin
P31	GND	IN	GND pin
P32	VDD	IN	Supply pin
P33	o_tms_fpga	OUT	Connect to tms pin of FPGA
P34	GND	IN	GND pin
P35	o_tdi_fpga	OUT	Connect to tdi pin of FPGA
P36	VDD	IN	Supply pin
P37	GND	IN	GND pin
P38	o_tck_fpga	OUT	Connect to tck pin of FPGA
P39	i_tdo_fpga	IN	Connect to tdo pin of FPGA
P40	GND	IN	GND pin
P41	VDD	IN	Supply pin
P42	GND	IN	GND pin
P43	GND	IN	GND pin
P44	GND	IN	GND pin
P45	i_data_prom	IN	Connect to data pin of PROM
P46	o_clk_prom	OUT	Connect to clk pin of PROM
P47	VDD	IN	Supply pin
P48	GND	IN	GND pin

6. Detailed Description

6.1 Function Description

BSV2CQRH is classified as aerospace grade product, which provides a timely scrubbing solution to mitigate single event upset(SEU) happened in space application SRAM FPGAs. The BSV2CQRH chip significantly reduces the degree of difficulty and complexity in designing scrubbing system. BSV2CQRH can scrub Xilinx Virtex2 serial FPASs XQR21000, XQR2V3000, XQR2V6000, as well as the BMTI fully compatible aerospace grade FPGAs BQR2V1000, BQR2V3000, BQR2V6000. The chips supported by BSV2CQRH are shown in table 6-1, but the FPGAs or PROMs not listed here are not supported.

Table 6-1 List of supported devices

FPGA Device	**Number of configuration bits**
Xilinx XQ2VR1000、XQ2V1000、XC2V1000	4，082，592
Xilinx XQ2VR3000、XQ2V3000、XC2V3000	10，494，368
Xilinx XQ2VR6000、XQ2V6000、XC2V6000	21，849，504
BMTI BQ2VR1000、BQ2V1000	4，082，592
BMTI BQ2VR3000、BQ2V3000	10，494，368
BMTI BQ2VR6000、BQ2V6000	21，849，504
PROM Device	**Storage capacity**
Xilinx 17 serial PROM	1、2、4、8、16M
Xilinx 18 serial PROM	512K、1M、2M、4M
Xilinx XCF serial PROM	1、2、4、8、16、32M
BMTI BQ18V04ECQ	4 M

The main functions of BSV2CQRH are as follows:

1) FPGA configuration

After power on, BSV2CQRH serially reads the configuration data from PROM, and puts the data on FPGA D0 pin straight away. The FPGA could be master serial mode or slave serial mode. The time token to configure FPGA through BSV2CQRH is the same as to configure FPGA directly with PROM.

2) Read back IDcode

After configuration, BSV2CQRH reads back FPGA IDcode through JTAG ports. According to the acquired IDcode, BSV2CQRH settles the parameter of scrubbing operation such as the length of scrubbing data.

3) Scrubbing configuration memory

After the FPGA IDcode is identified, BSV2CQRH reads the configuration data from PROM, the data is processed to generate JTAG format scrubbing data. The scrubbing data refreshes the configuration memory except the BRAM content over and over again. The user function is not affected by the scrubbing operation if only SRL16 and LUTRAM are not used in the design.

4) FPGA reconfiguration

If a single event function interruption (SEFI) happened to FPGA, BSV2CQRH then checks FPGA Done pin to decide if the FPGA should be reconfigured. If the done pin is low, BSV2CQRH pulls down Program pin to reconfigure FPGA.

5) Control signal descriptions

BSV2CQRH is controlled by four pins: i_rst(reset pin),i_clk(clock pin),i_pause(enable pin),i_half(half scrubbing switch pin). Where, i_rst is a global reset signal, if i_rst is low BSV2CQRH will stop any scrubbing operation and go to configuring state, then the chip only could perform configuring function, All signals of BSV2CQRH are synchronized by i_clk, whose frequency range should be 1MHz to 20MHz and duty cycle should be 50%. The clock is recommended to constantly supply, so the scrubbing will be stable. If the user needs to pause the scrubbing, it will be realized by pulling down i_pause pin at any time, BSV2CQRH will continue the current scrubbing, and finishing the entire cycle, than will go to standby state, all output pins will be in high impedance state; if the user needs to resume the scrubbing, just pull up i_pause pin at any time, and BSV2CQRH will either scrub or configure FPGA according to the level of Done pin. If i_half is low, BSV2CQRH will only scrub the left half of FPGA configuration memories, and if i_half is high, BSV2CQRH still will scrub the whole memories. This half scrubbing function makes users has the chance to use LUT RAM, if they constraint the RAM in the right half of FPGA.

6) Scrubbing period

The period of scrubbing is related to the size of bit stream and the clock frequency. The period calculation formula is :

T= size of bit stream× clock period ×2

The typical scrubbing periods are shown in table 6-2.

Table 6-2 BSV2CQRH scrubbing period

Device	Size of bit stream	Clock frequency	Scrubbing period
XQ2VR1000、BQ2VR1000	4，082，592	10MHz	About 800 ms
XQ2VR3000、BQ2VR1000	10，494，368	10MHz	About 2 s
XQ2VR6000、BQ2VR1000	21，849，504	10MHz	About 4 s

6.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 10℃～30℃ and relative humidity less than 70%. There should be no acid , alkali or other radiant gas in the environment,

6.3 Absolute Maximum Ratings

a) Supply voltage range to ground potential（V_{DD}）： -0.5 V ～3.6V
b) DC input voltage range（V_{in}）： -0.5 V ～3.6V
c) Storage temperature（T_{stg}）： -65℃～ 150℃
d) Lead temperature（T_h）： 260℃
e) Thermal resistance（$R_{th(J-C)}$）： 4.2℃/W
f) Power dissipation（P_D）： 0.5W
g) Maximum frequency（fmax）： 20MHz

6.4 Recommended Operation Conditions

a) Supply voltage relative to ground（VDD）： 3.135V~3.465V
b) Case operation temperature range(TA) ： -55℃~125℃
c) Operation frequency（f）： 10MHz

7. Specifications

All electrical characteristics are shown in table 7-1.

Table 7-1 BSV2CQRH electrical characteristics

Test	Symbol	Conditions	Llimits	units

		（-55℃≦ T_A≤ 125℃ 3.135V≤V_{DD}≤3.465V）	min	max	
Output high voltage	V_{OH}	V_{DD}=3.135V， I_{OH}=-12 ma，test o_ce_prom 、o_clk_prom、o_tck_fpga、o_tdi_fpga、o_tms_fpga、o_rst 、o_din_fpga	2.4	—	V
Output low voltage	V_{OL}	V_{DD}=3.135V， I_{OL}=12 mA，test o_rst 、o_ce_prom、o_oe_prom、o_clk_prom、o_tck_fpga、o_tms_fpga、o_tdi_fpga、o_din_fpga	—	0.4	V
Input high voltage	V_{IH}	V_{DD}=3.3V	2.0	—	V
Input low voltage	V_{IL}	V_{DD}=3.3V	—	0.8	V
Input high leakage current	I_{IH}	V_{DD}=3.465V，test i_cclk_fpga 、i_clk 、 i_data_prom 、i_done_fpga 、i_init_fpga、 i_tdo_fpga	—	100	nA
			—	1	μA
			—	1	μA
Input low leakage current	$\lvert I_{IL} \rvert$	V_{DD}=3.465V，test i_cclk_fpga、i_clk、、i_data_prom、i_done_fpga、i_init_fpga、i_tdo_fpga	—	100	nA
			—	1	μA
			—	1	μA
Pad pull up leakage current	I_{RPU}	V_{DD}=3.465V，test i_pause 、i_rst 、i_half	—	400	nA
			—	1	μA
			—	1	μA
Pad pull down leakage current	I_{RPD}	V_{DD}=3.465V，test test1、test2、test3、scan_en	—	400	nA
			—	1	μA
			—	1	μA

Quiescent supply current	I_{DDS}	V_{DD}=3.465V	—	0.2	mA
Dynamical supply current	I_{DDD}	V_{DD}=3.465V, f =20MHz	—	120	mA
Input output capacitance	$C_{in/out}$	f=1.0MHz, T_A =25℃	—	15	pF
Function test	—	V_{DD}=3.3V, f =10MHz/20MHz	—	—	—
Output delay: o_tck_fpga relative to i_clk	t_{c2d_tck}	V_{DD}=3.135V, f =20MHz	—	30	ns
Output delay: o_tms_fpga relative to i_clk	t_{c2d_tms}		—	30	ns
Output delay: o_tdi_fpga relative to i_clk	t_{c2d_tdi}		—	30	ns
Output delay: o_din_fpga relative to i_data_prom	t_{dd}		—	30	ns

8. Package Specifications

The specifications of CQFP48 package are shown in figure9-1.

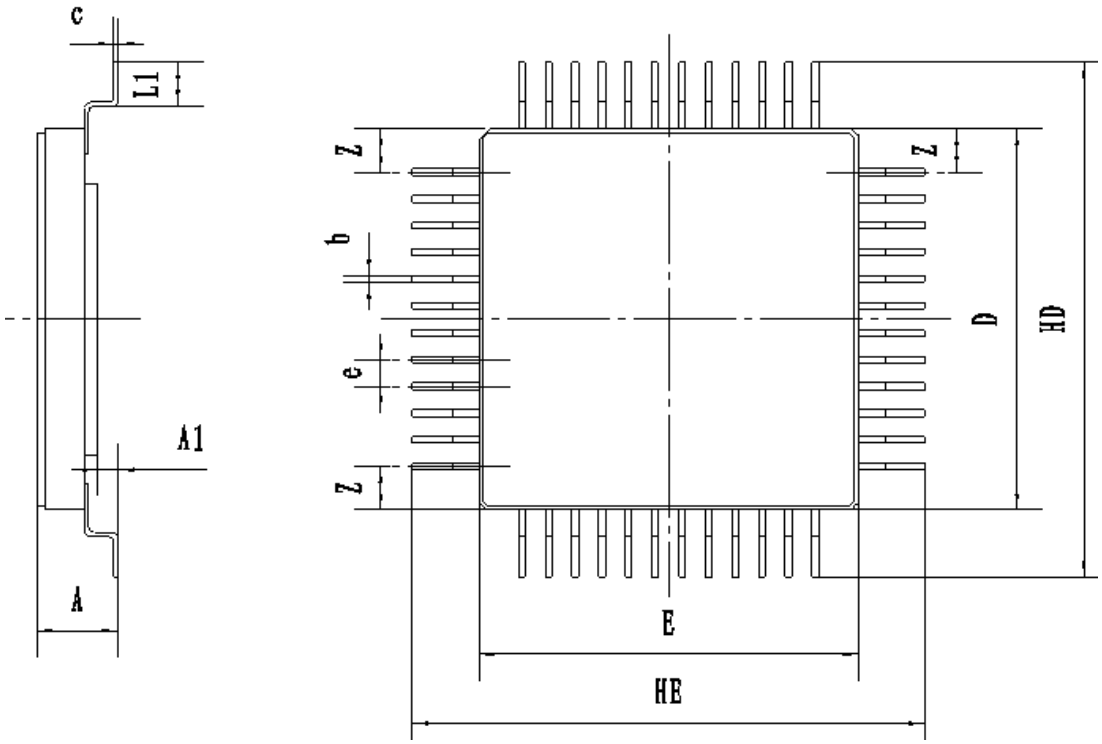


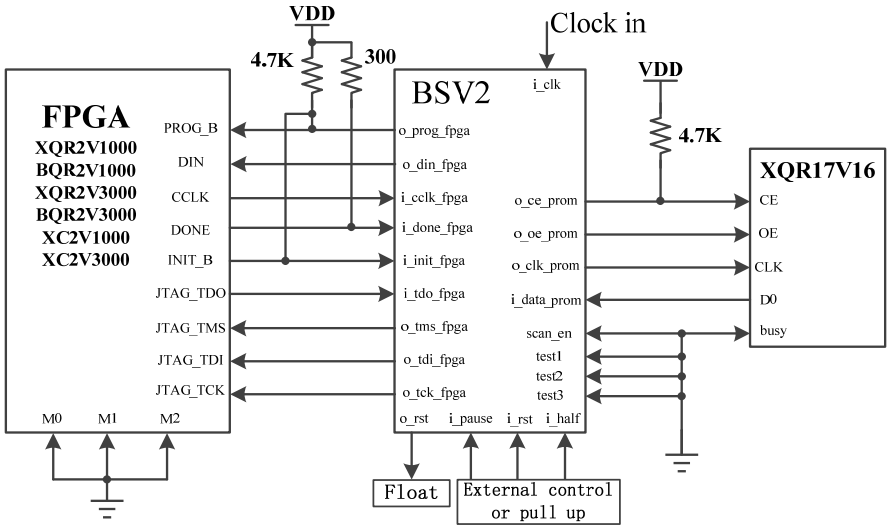
Figure 9-1 CQFP48 package specifications

Table 9-1 size symbol list

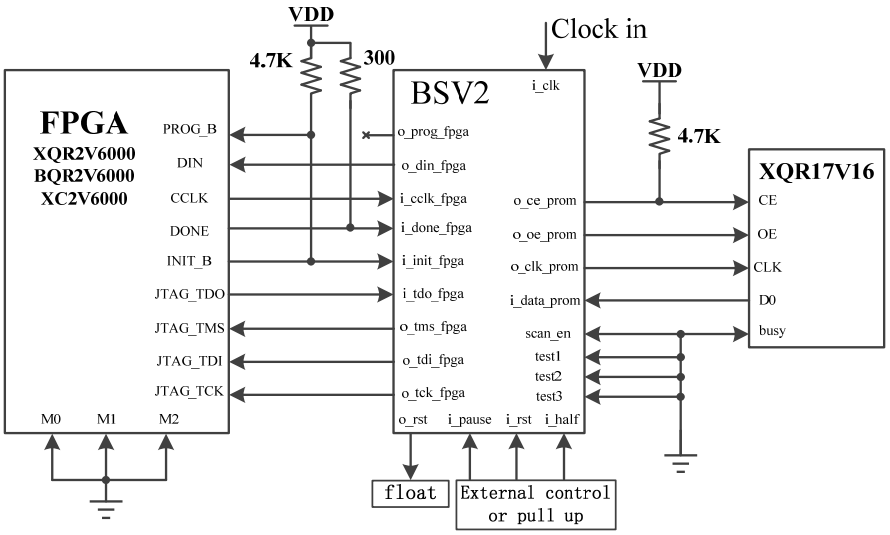
Size symbol	Value （unit：mm）		
	min	typical	max
A	2.5		3.5
A1	0.5	0.75	1.0
b		0.38	
c		0.15	
e		1.02	
Z		1.52	
D/E	14.09	14.22	14.52
HD/HE	18.6	19.2	20.1
L1	1.25	1.5	1．8

9. Appendix I Typical Application Example

BSV2CQRH can configure FPGA in serial mode and scrub FPGA in JTAG mode. BSV2CQRH is placed between FPGA and configuration PROM; it works as data Exchange Bridge. Master serial mode is shown in appendix figure 1-1. Where the FPGA pins program and initial are pulled up with 4.7KΩ resistance, done pin is pulled up with 330Ω resistance. Slave serial mode is similar, the difference is the CCLK source isn't FPGA but some external device.



（a）used in 2V1000 and 2V3000



（b）used in 2V6000

Appendix figure 1-1 master serial configuration mode

Attentions：

- The signal i_clk should connect to active clock source, the clock frequency should below 20MHz(room temperature). The frequency should be reduced , 10MHz is recommended.
- The signal o_oe_prom is open drain，should be pulled up with 4.7KΩ resistance.
- Configuration bit stream and the PROM mcs format file should be generated by a Xilinx software.
- If BSV2CQRH is used in 2V6000 scrubbing，this pin shall not connect with 2V6000.
- During the scrubbing process, avoid restarting the configuration of FPGA after i_rst is changed to low level.
- Because BSV2CQRH will use the JTAG ports when it work , the JTAG chain of FPGA and PROM should be independent ,in case the tdo pin of PROM may disturb the scrubbing operation.

Taboo issues：

- This pin must not connect to diode, in case the voltage of pin i_done_fpga is cut down. If the voltage loss did happened, BSV2CQRH may reconfiguring FPGA, which is unexpected.
- Keep the default size of bit stream; do not use any options that could change the default size, such as bit compression.
- Do not use disable readback option or disable reconfiguration option in ISE.
- Do not use LUT-RAM or LUT-shifter, unless enable i_half signal.

The influence on FPGA:

- The first configuration time after power on: unchanged
- Influence on user function：none
- The core supply current is increased when scrubbing.
- The POR single event function interruption (SEFI) could be repaired.

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