MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™

OptiMOS™ Power-MOSFET, 40V

BSZ023N04LS

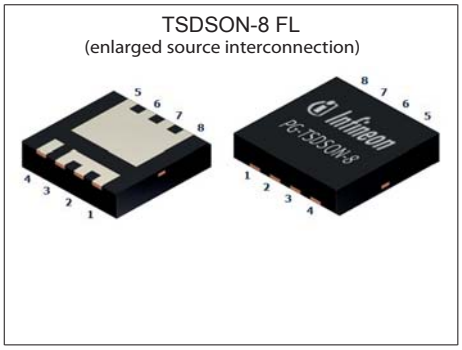
Data Sheet

Rev. 2.0
Final

Power Management & Multimarket

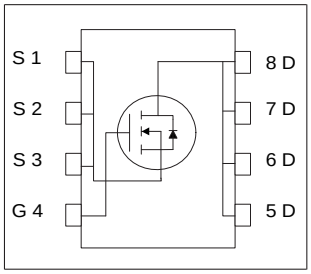
1 Description

This N-channel MOSFET is optimized for low on-state resistance, gate charge and reverse recovery charge which make it a perfect choice for synchronous rectification in switch mode power supplies such as in servers.



Features

- Optimized for synchronous rectification
- Very low on-resistance $R_{DS(on)}$
- 100% avalanche tested
- Superior thermal resistance
- N-channel, logic level
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Qualified according to JEDEC for target applications
- Higher solder joint reliability due to enlarged source interconnection



Applications

- Synchronous rectification
- Isolated DC/DC converters
- Motor control for 12-24V systems
- Or-ing switches

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40.0	V
$R_{DS(on),max}$	2.35	mΩ
I_D	40.0	A
Q_{OSS}	33.0	nC
Q_G(0V..10V)	37.0	nC

Type / Ordering Code	Package	Marking	Related Links
BSZ023N04LS	PG-TSDSON-8 FL	023N04L	-

Table of Contents

2 Maximum ratings

at T_j = 25 °C, unless otherwise specified

Table 2 Maximum ratings

at 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - - - -	- - - - -	40 40 40 40 22	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=60 K/W
Pulsed drain current[1]	$I_{D,pulse}$	-	-	160	A	T_C=25 °C
Avalanche current, single pulse[2]	I_{AS}	-	-	20	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	130	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	69	W	T_C=25 °C
Power dissipation (for PCB version)[3]	P_{tot}	-	-	2.1	W	T_A=25 °C, R_{thJA}=60 K/W
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.8	K/W	-
Device on PCB[4]	R_{thJA}	-	-	60	K/W	6 cm² cooling area

[1] See diagram 3 for more detailed information
[2] See diagram 13 for more detailed information
[3] See diagram 3 for more detailed information
[4] Refered to condition: Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2.0	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1.0 100	µA	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	2.4 2.0	3.2 2.35	mΩ	V_{GS}=4.5 V, I_D=20 A V_{GS}=10 V, I_D=20 A
Gate resistance	R_G	-	1.1	-	Ω	-
Transconductance	g_{fs}	55	110	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=20 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2630	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance	C_{oss}	-	750	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	60	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	38	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	42	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	8.0	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics

see table 16 for more details

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	6.3	-	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	4.2	-	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	6.0	-	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	8.1	-	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	37	-	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	2.4	-	V	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	19	-	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	32	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	33	-	nC	V_{DD}=20 V, V_{GS}=0 V

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	40	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	160	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.8	1.0	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	24	-	ns	V_R=20 V, I_F=20A, di_F/dt=400 A/µs
Reverse recovery charge	Q_{rr}	-	20	-	nC	V_R=20 V, I_F=20A, di_F/dt=400 A/µs

5 Electrical characteristics diagrams

Table 8

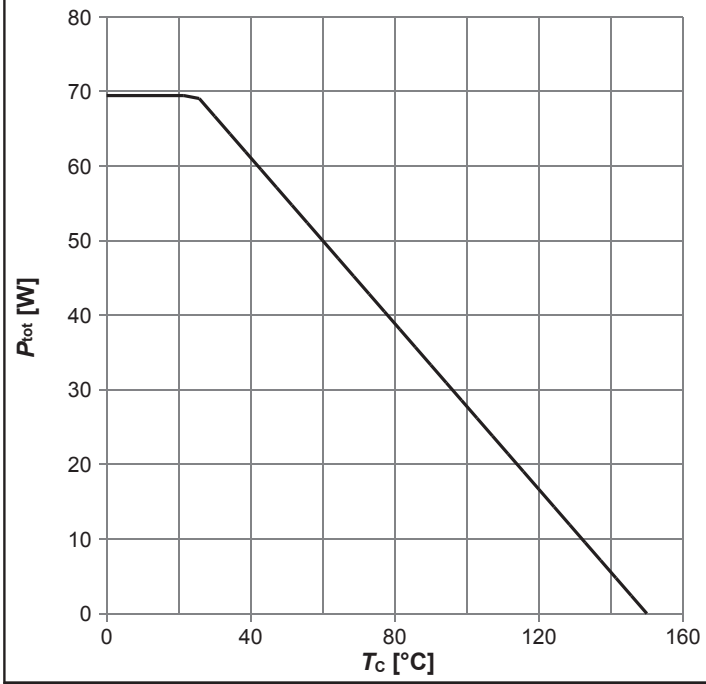
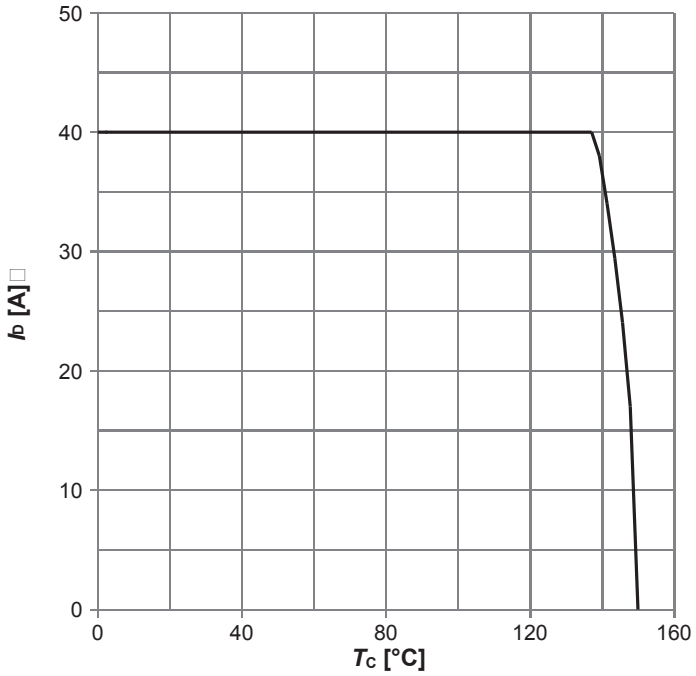
Diagram 1: Power dissipation	Diagram 2: Drain current
	
$P_{tot}=f(T_C)$	$I_D=f(T_C)$; $V_{GS}=10$ V

Table 9

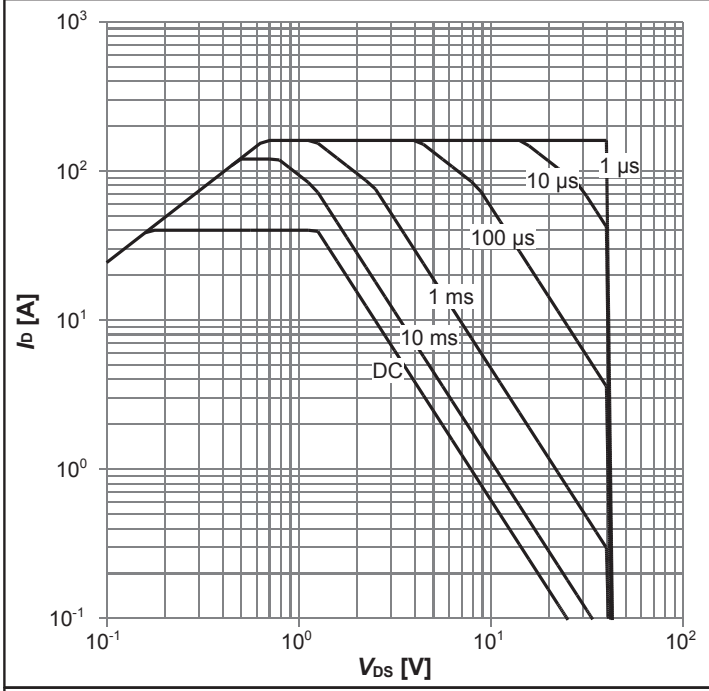
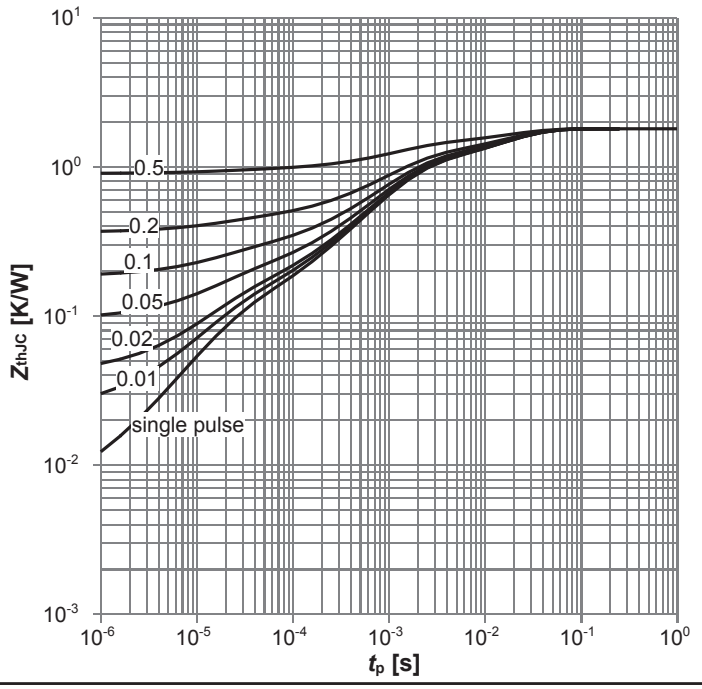
Diagram 3: Safe operating area	Diagram 4: Max. transient thermal impedance
	
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p	$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Table 10

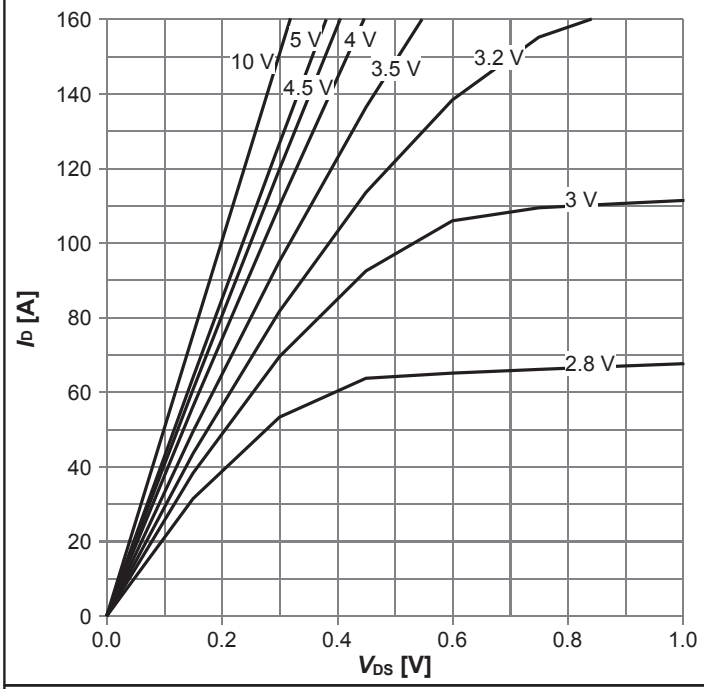
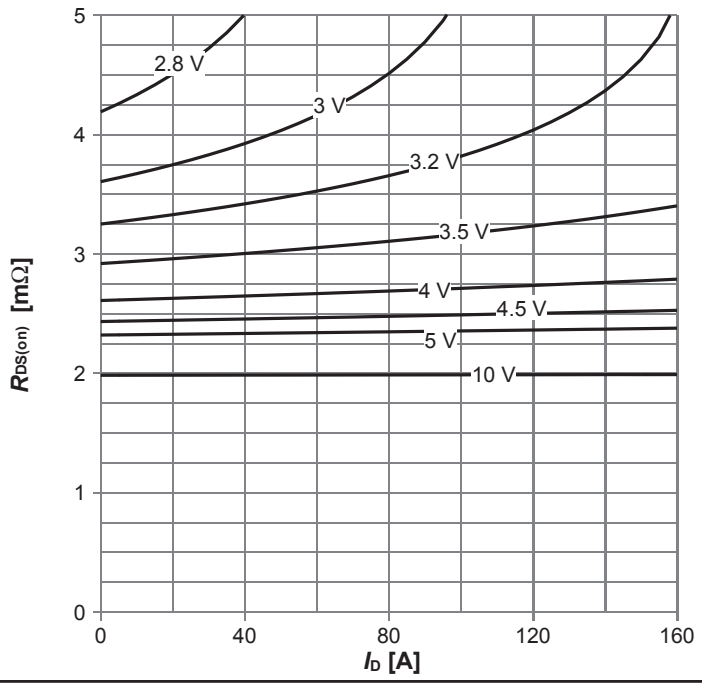
Diagram 5: Typ. output characteristics	Diagram 6: Typ. drain-source on resistance
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Table 11

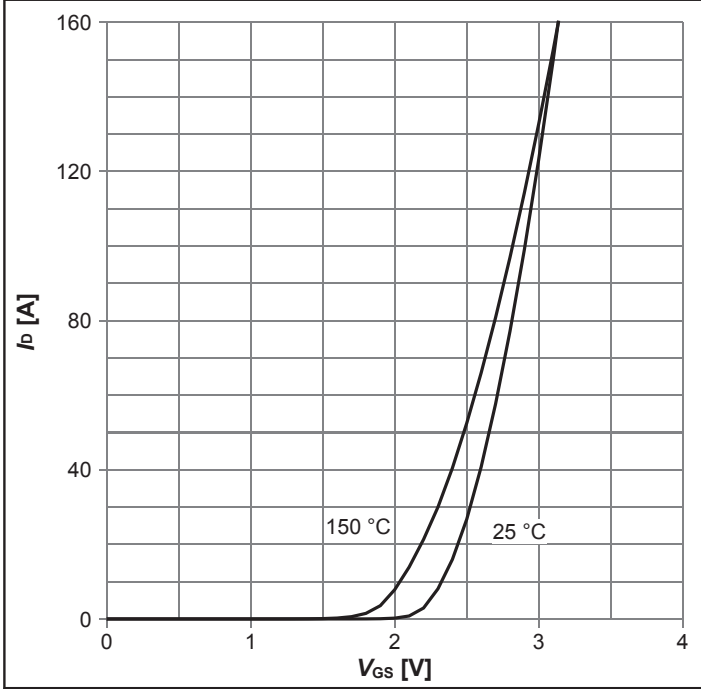
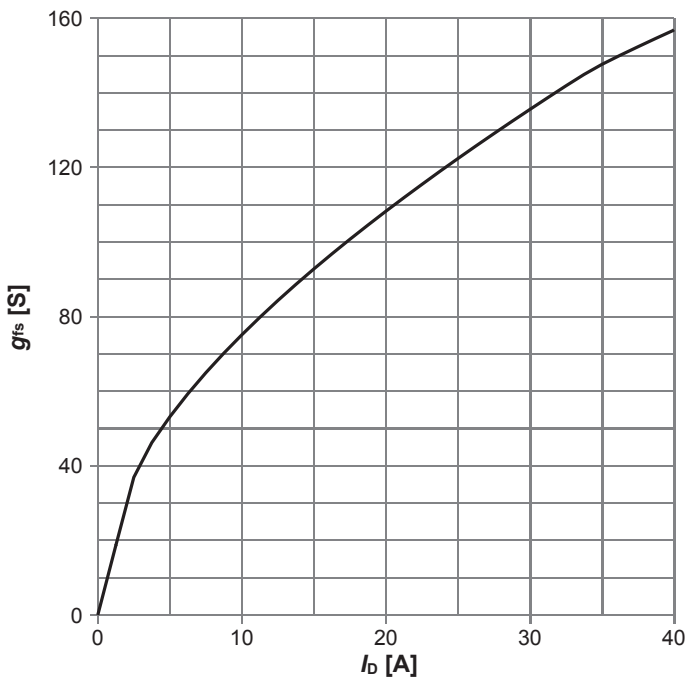
Diagram 7: Typ. transfer characteristics	Diagram 8: Typ. forward transconductance
	
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j	g_{fs}=f(I_D); T_j=25 °C

Table 12

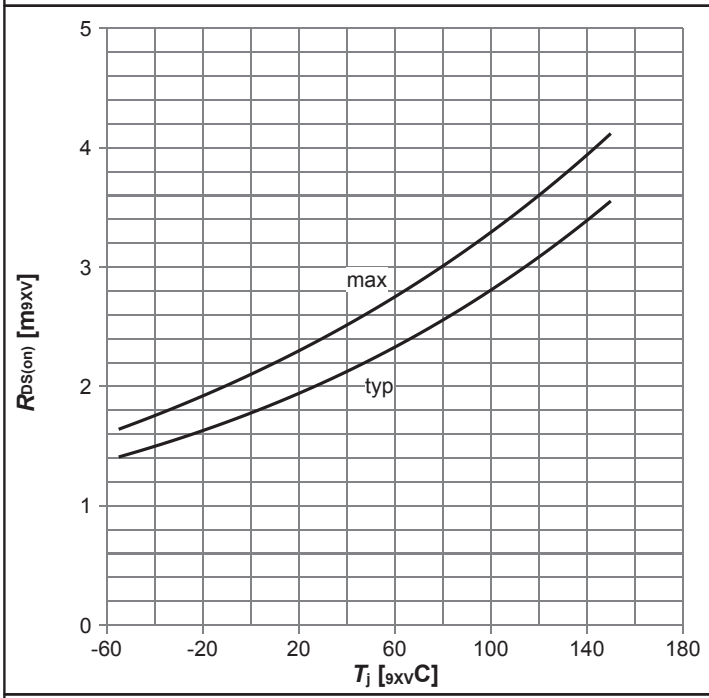
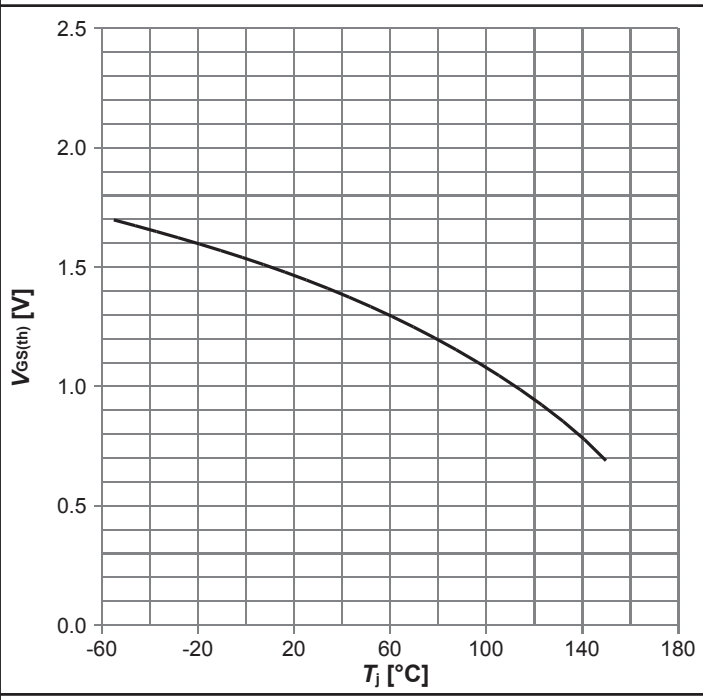
Diagram 9: Drain-source on-state resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}=f(T_j)$; I_D=20 A; V_{GS}=10 V	$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; I_D=250 µA

Table 13

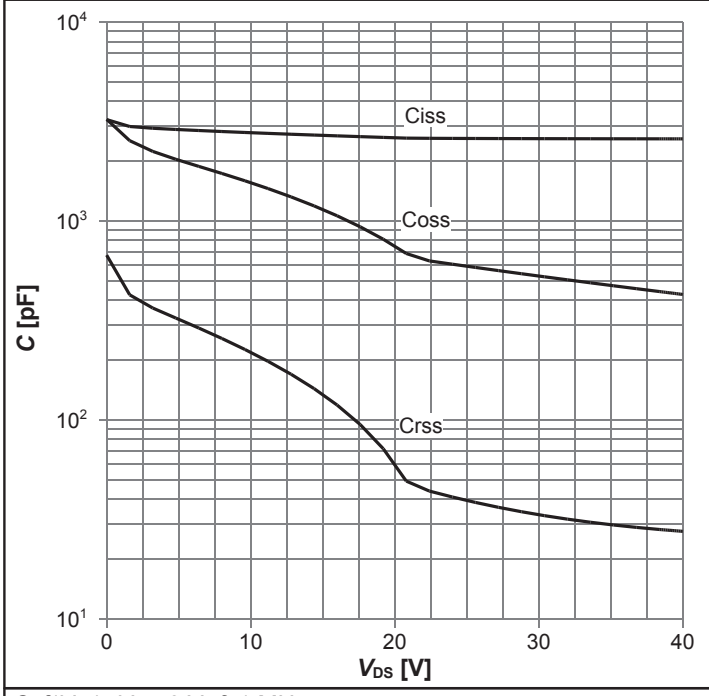
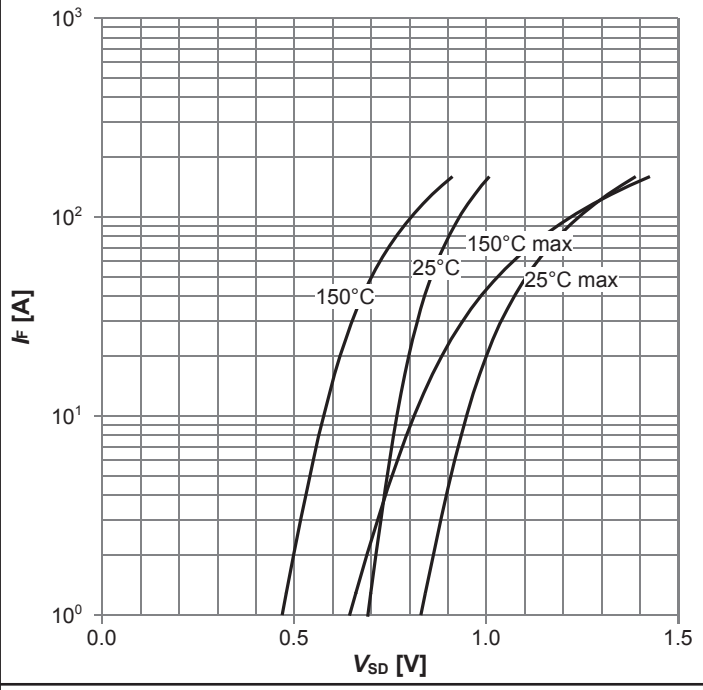
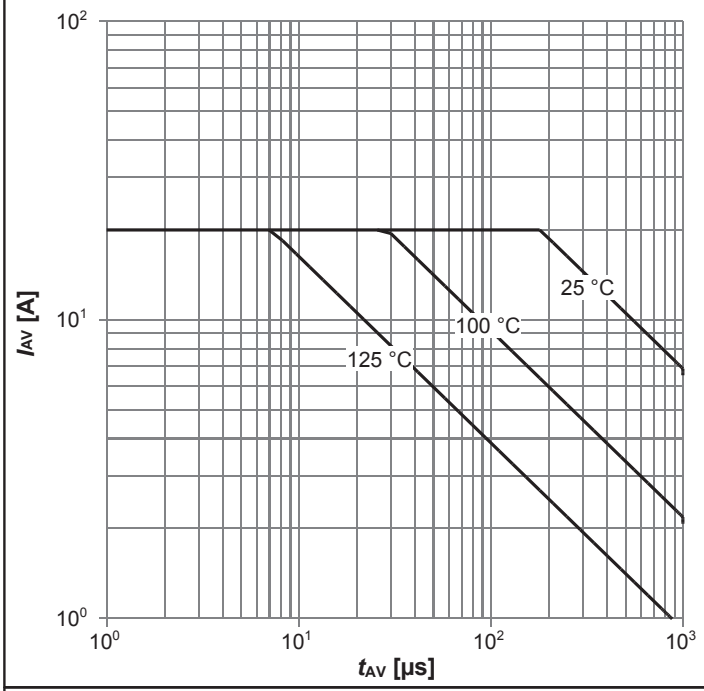
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz	$I_F=f(V_{SD})$; parameter: T_j

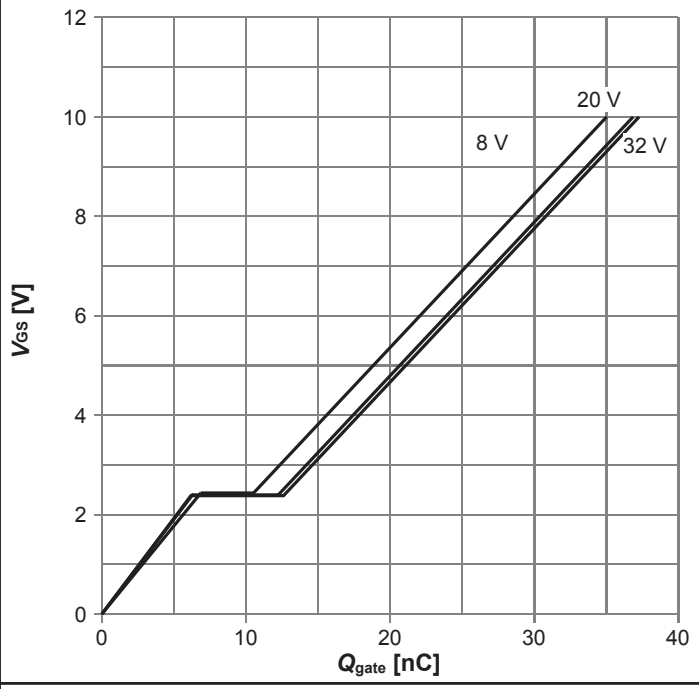
Table 14

Diagram 13: Avalanche characteristics



I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

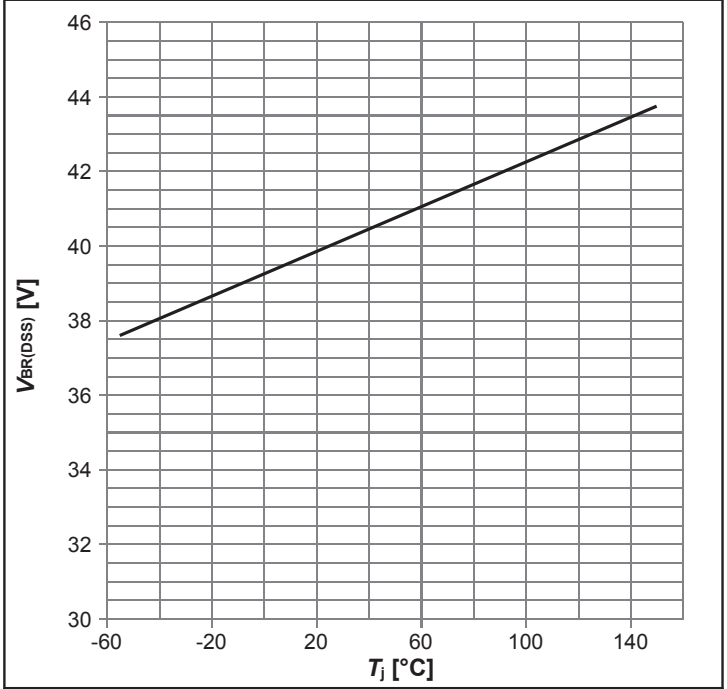
Diagram 14: Typ. gate charge



V_{GS}=f(Q_{gate}); I_D=20 A pulsed; parameter: V_{DD}

Table 15

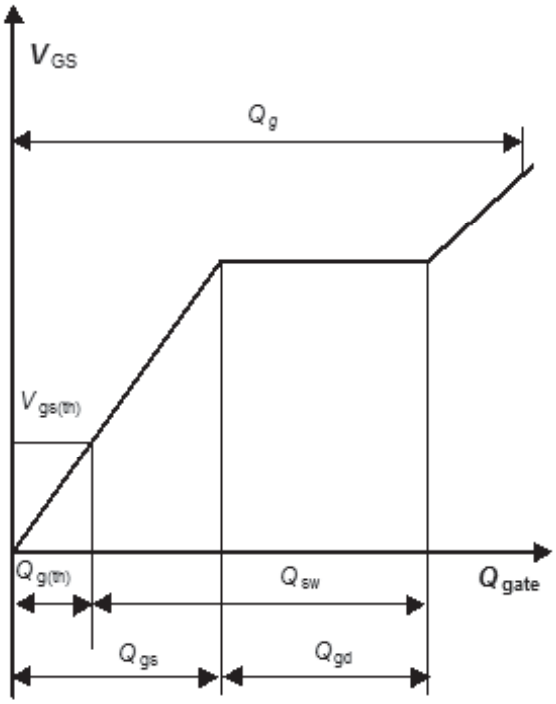
Diagram 15: Drain-source breakdown voltage



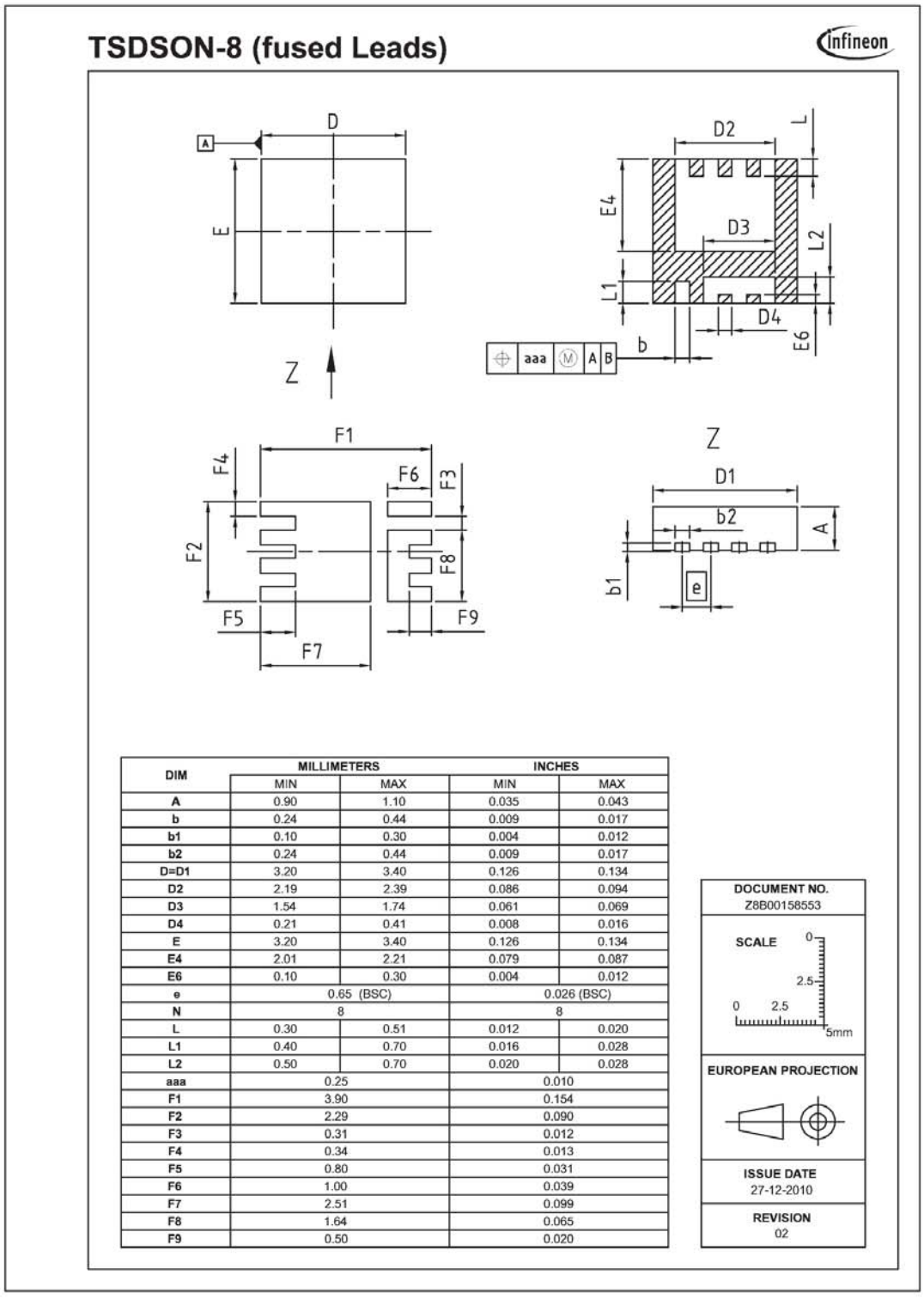
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

6 Test Circuits

Table 16 Gate Charge Waveform



7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.24	0.44	0.009	0.017
b1	0.10	0.30	0.004	0.012
b2	0.24	0.44	0.009	0.017
D=D1	3.20	3.40	0.126	0.134
D2	2.19	2.39	0.086	0.094
D3	1.54	1.74	0.061	0.069
D4	0.21	0.41	0.008	0.016
E	3.20	3.40	0.126	0.134
E4	2.01	2.21	0.079	0.087
E6	0.10	0.30	0.004	0.012
e	0.65 (BSC)		0.026 (BSC)	
N	8		8	
L	0.30	0.51	0.012	0.020
L1	0.40	0.70	0.016	0.028
L2	0.50	0.70	0.020	0.028
aaa	0.25		0.010	
F1	3.90		0.154	
F2	2.29		0.090	
F3	0.31		0.012	
F4	0.34		0.013	
F5	0.80		0.031	
F6	1.00		0.039	
F7	2.51		0.099	
F8	1.64		0.065	
F9	0.50		0.020	

DOCUMENT NO.
Z8B00158553

SCALE
0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
27-12-2010

REVISION
02

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm/inches

Revision History

BSZ023N04LS

Revision: 2012-11-22, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2012-11-22	Release of final version

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