

1. General description

Planar passivated very sensitive gate four quadrant triac in a TO92 plastic package intended for interfacing with low power drivers including microcontrollers.

2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing with low power gate drivers and microcontrollers
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- Air conditioner indoor fan
- General purpose low power motor control
- General purpose switching and phase control

4. Quick reference data

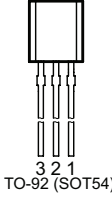
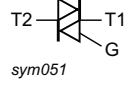
Table 1. Quick reference data

Symbol	Parameter	Conditions	Values			Unit
Absolute maximum rating						
V_{DRM}	repetitive peak off-state voltage		800			V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 51\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	1			A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(initial)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	12.5			A
		full sine wave; $T_{j(initial)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	13.7			A
T_j	junction temperature		125			°C
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	-	0.4	3	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	-	1.3	3	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7	-	1.4	3	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 7	-	3.8	7	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	1.3	5	mA
V_T	on-state voltage	$I_T = 1.4\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.2	1	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; $R_{GT1(ext)} = 1\text{ k}\Omega$; Fig. 12	10	20	-	V/ μ s
dV_{com}/dt	rate of change of commutating voltage	$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $dI_{com}/dt = 0.5\text{ A/ms}$; $I_T = 1\text{ A}$; gate open circuit	2	-	-	V/ μ s

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2	 <p>TO-92 (SOT54)</p>	 <p>sym051</p>
2	G	gate		
3	T1	main terminal 1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT131-800	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

7. Marking

Table 4. Marking codes

Type number	Marking codes
BT131-800	131-8

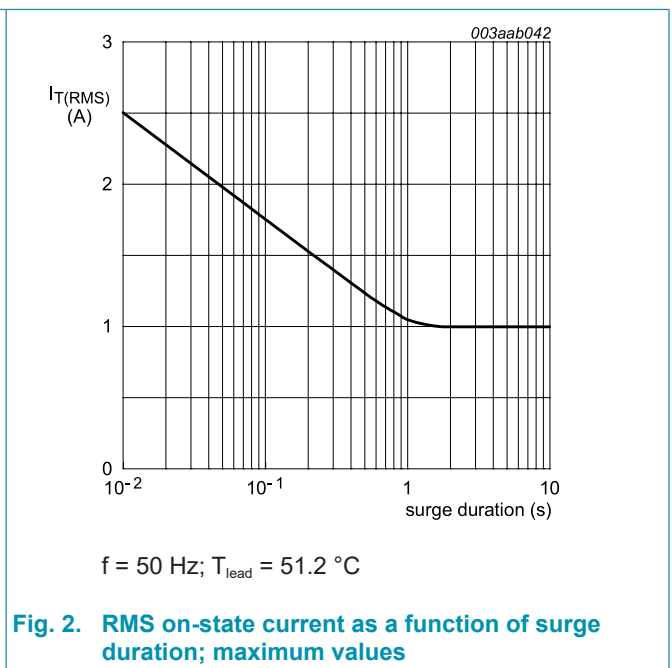
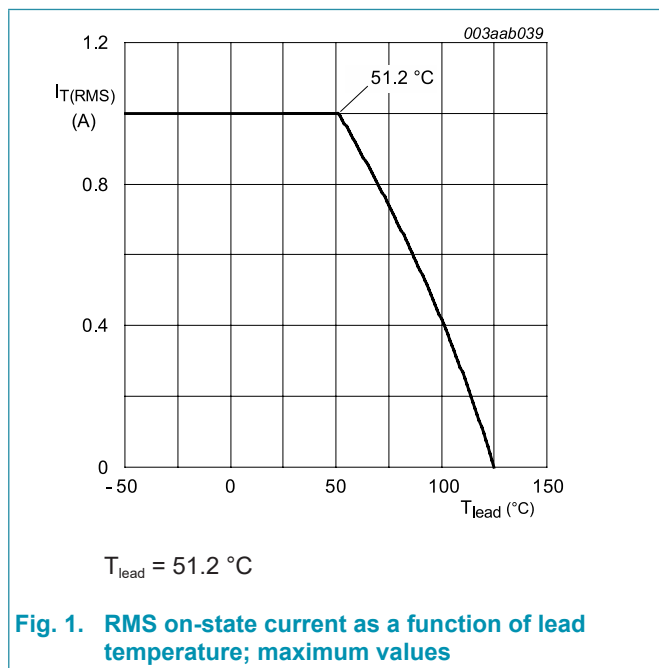
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{DRM}	repetitive peak off-state voltage [1]		800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 51\text{ °C}$; Fig 1; Fig 2; Fig 3	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig 4; Fig 5	12.5	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	13.7	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	0.78	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 6\text{ mA}$; T2+ G+	50	$A/\mu s$
		$I_G = 6\text{ mA}$; T2+ G-	50	$A/\mu s$
		$I_G = 6\text{ mA}$; T2- G-	50	$A/\mu s$
		$I_G = 14\text{ mA}$; T2- G+	10	$A/\mu s$
I_{GM}	peak gate current		2	A
P_{GM}	peak gate power		5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.1	W
T_{stg}	storage temperature		-40 to 150	$^{\circ}C$
T_j	junction temperature		125	$^{\circ}C$

[1] Although not recommended, off-state voltage up to V_{DRM} may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed $3A/\mu s$.



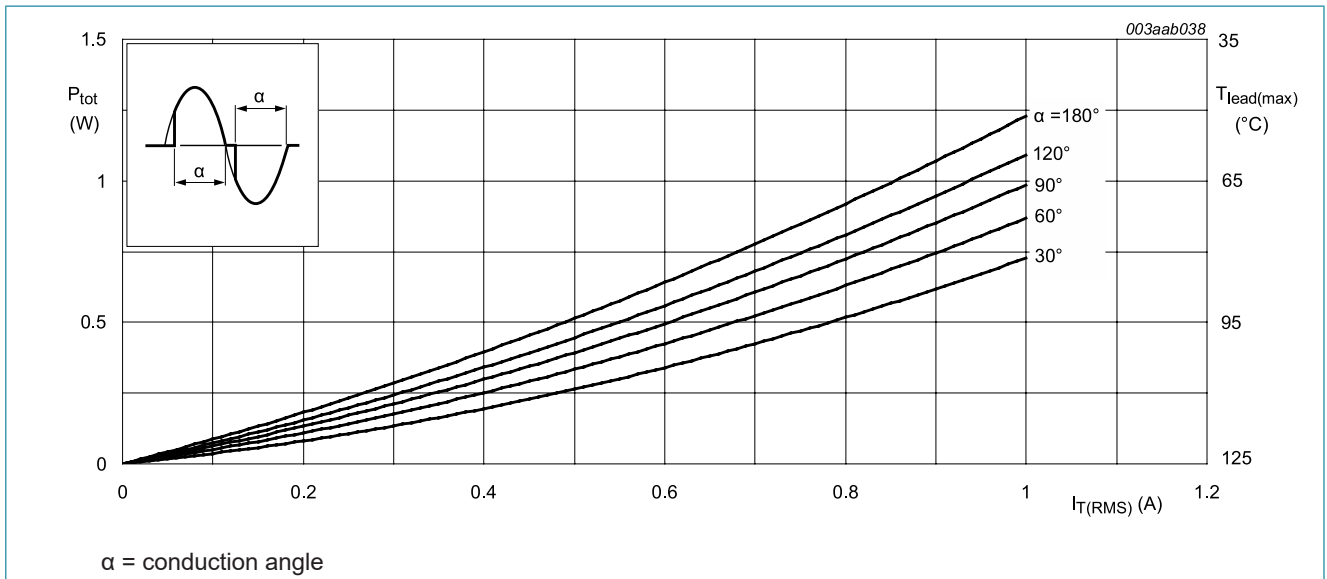


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

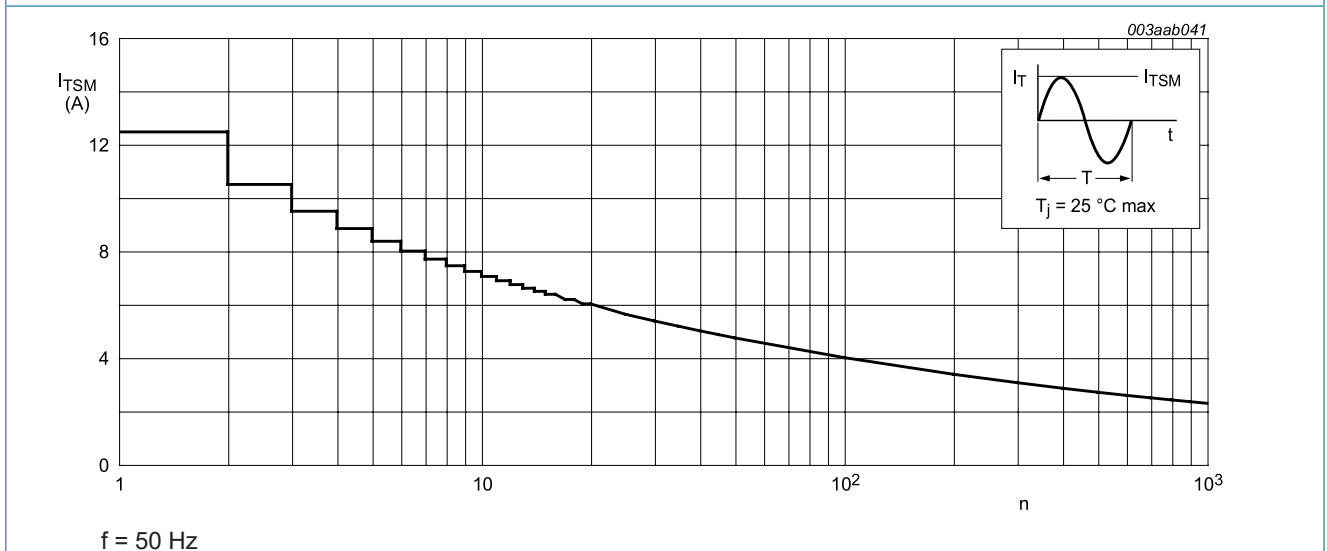
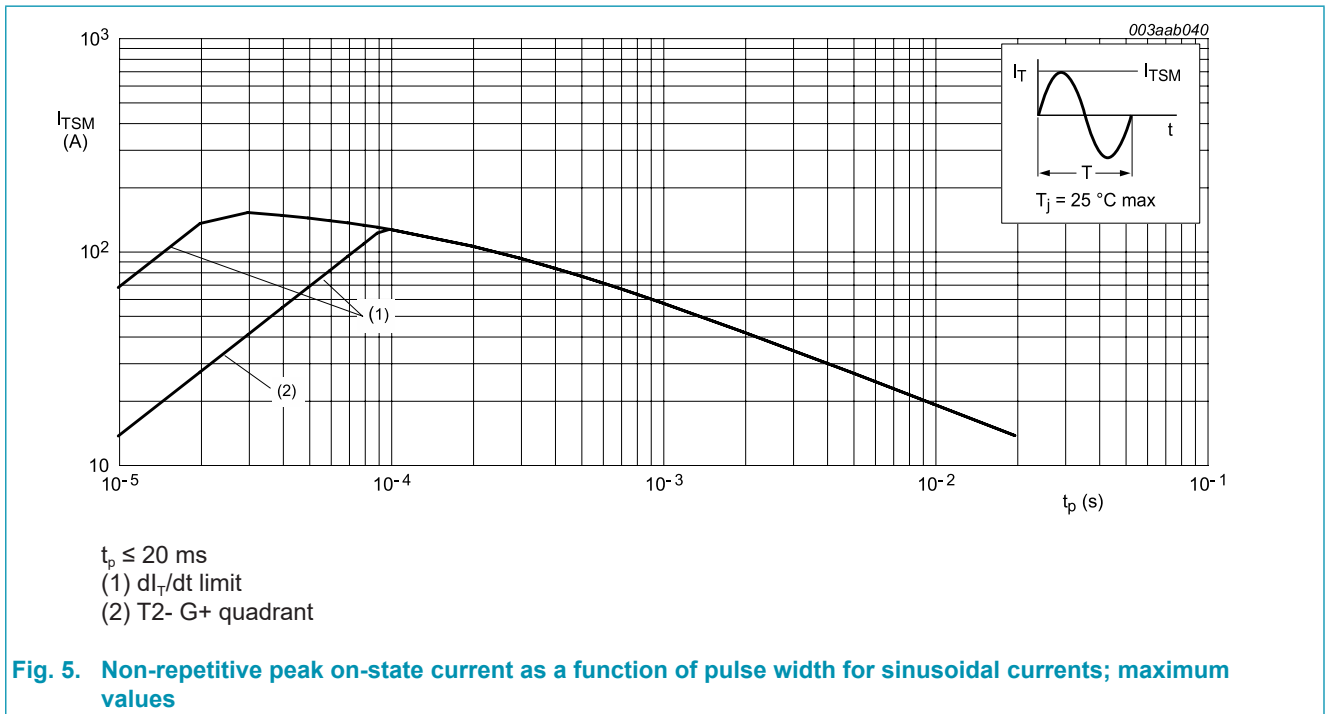


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle; Fig 6	-	-	60	K/W
		half cycle; Fig 6	-	-	80	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W

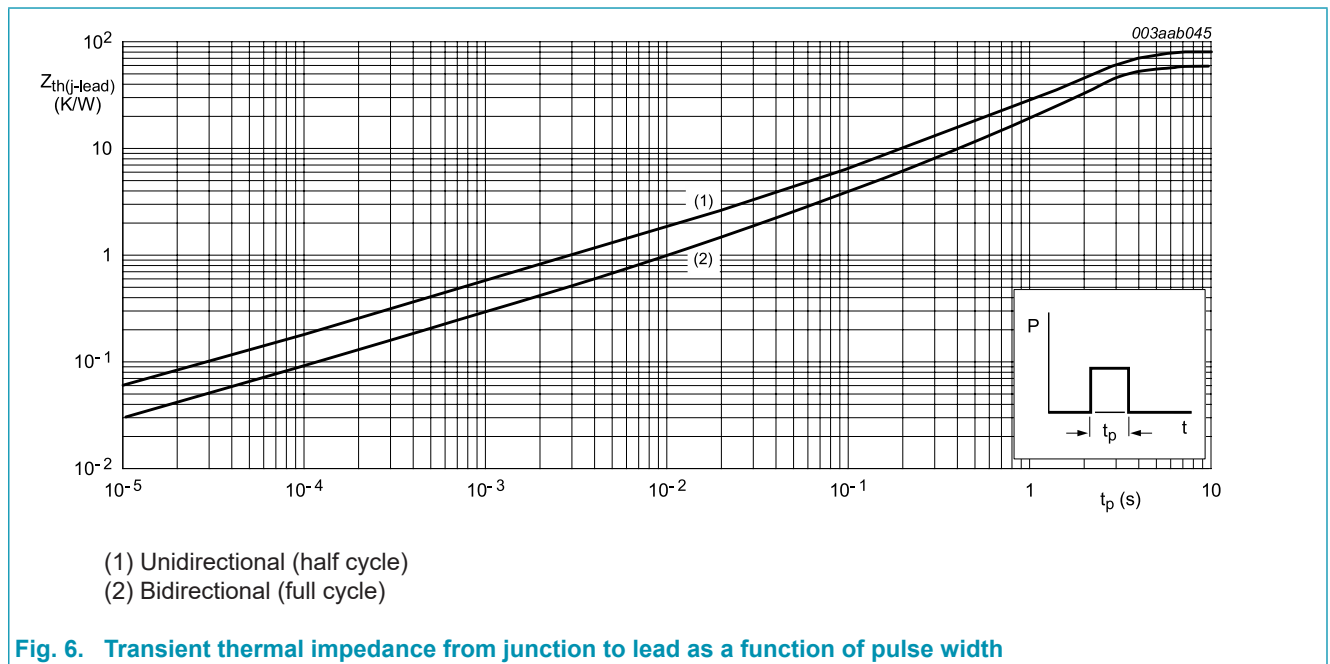
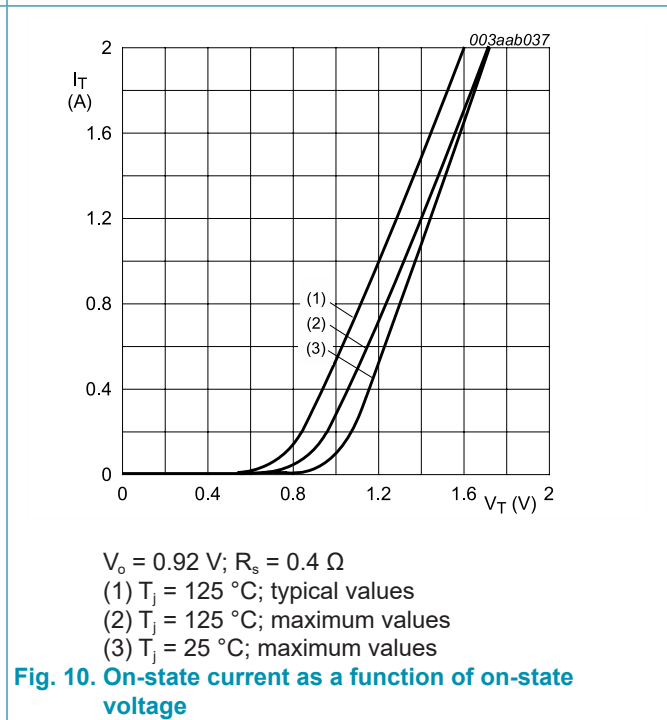
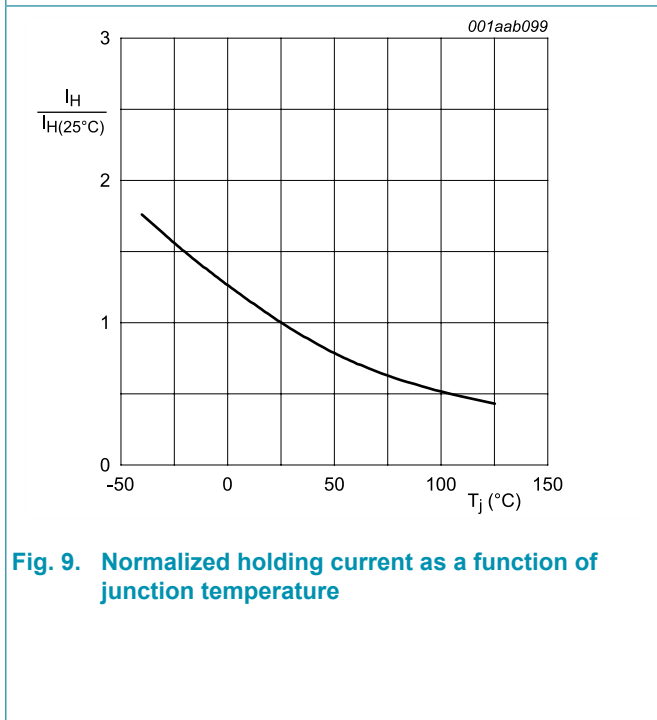
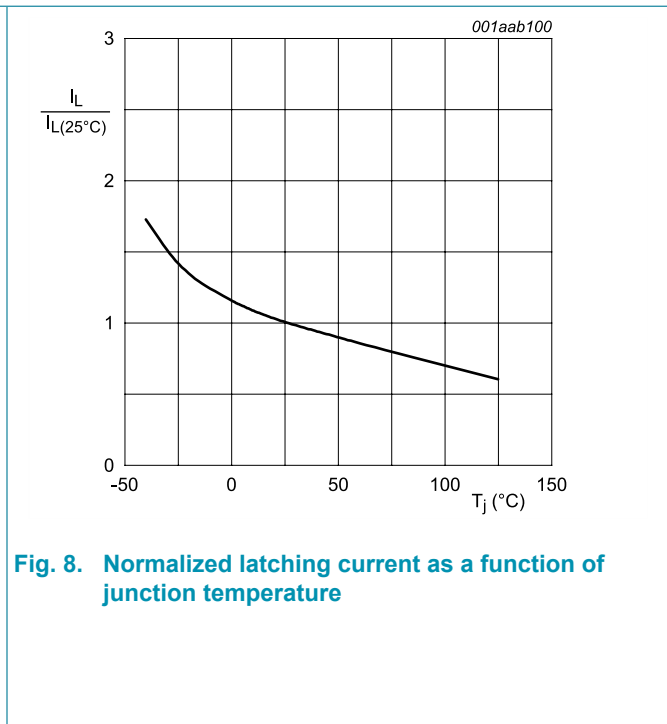
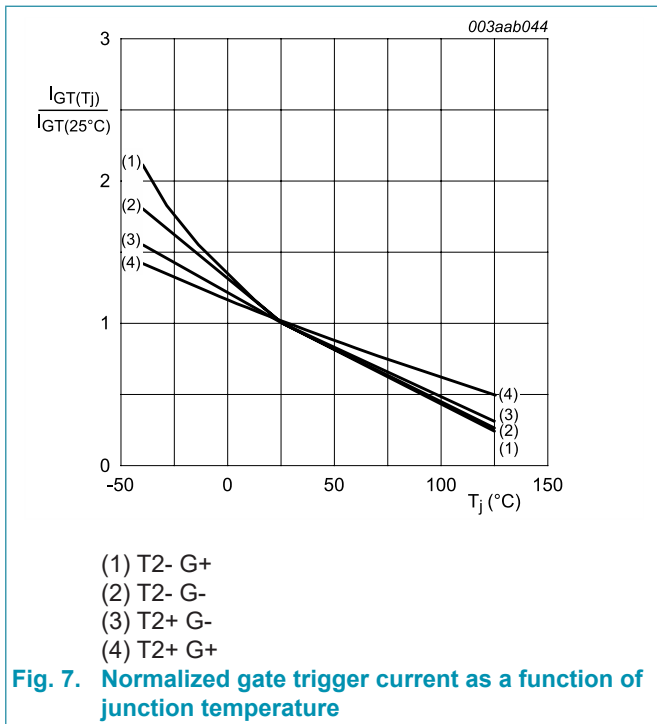


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_J = 25\text{ °C}$; Fig. 7	-	0.4	3	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_J = 25\text{ °C}$; Fig. 7	-	1.3	3	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_J = 25\text{ °C}$; Fig. 7	-	1.4	3	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_J = 25\text{ °C}$; Fig. 7	-	3.8	7	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_J = 25\text{ °C}$; Fig. 8	-	1.2	5	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_J = 25\text{ °C}$; Fig. 8	-	4	8	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_J = 25\text{ °C}$; Fig. 8	-	1	5	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_J = 25\text{ °C}$; Fig. 8	-	2.5	8	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_J = 25\text{ °C}$; Fig. 9	-	1.3	5	mA
V_T	on-state voltage	$I_T = 1.4\text{ A}$; $T_J = 25\text{ °C}$; Fig. 10	-	1.2	1	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_J = 25\text{ °C}$; Fig. 11	-	0.7	1	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_J = 125\text{ °C}$; Fig. 11	0.2	0.3	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_J = 125\text{ °C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_J = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; $R_{GT1(ext)} = 1\text{ k}\Omega$; Fig. 12	10	20	-	V/ μ s
dV_{com}/dt	rate of change of commutating voltage	$V_D = 400\text{ V}$; $T_J = 125\text{ °C}$; $dI_{com}/dt = 0.5\text{ A/ms}$; $I_T = 1\text{ A}$; gate open circuit	2	-	-	V/ μ s
t_{gt}	gate-controlled turn-on time	$I_{TM} = 1.5\text{ A}$; $V_D = 800\text{ V}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu$ s	-	2	-	μ s



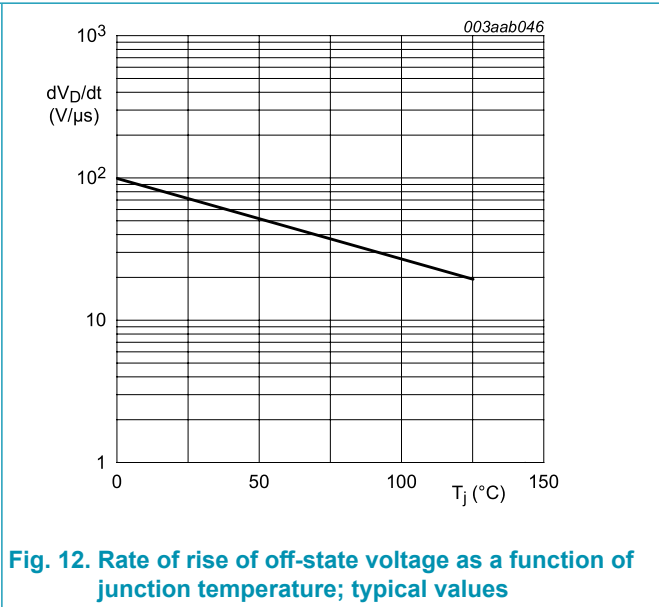
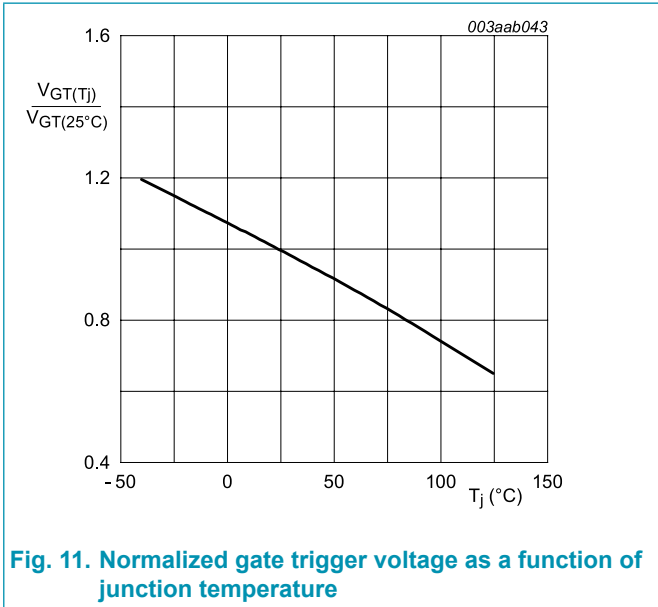
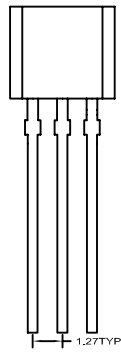


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

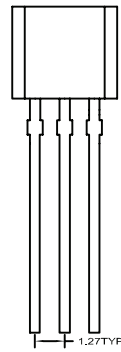
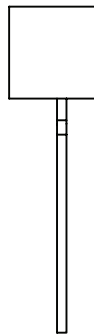
Fig. 12. Rate of rise of off-state voltage as a function of junction temperature; typical values

11. Package outline

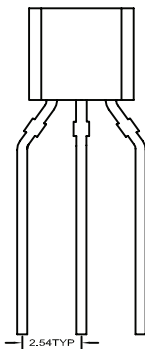
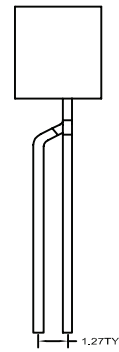
SOT54 PACKAGE OUTLINE



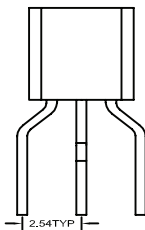
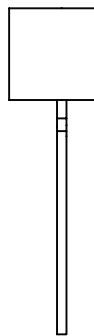
SOT54
Bulk Pack - 412



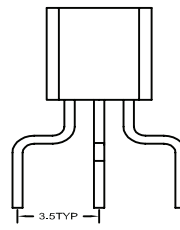
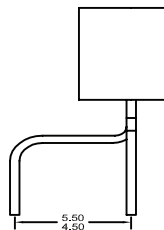
SOT54 LEADS ON CIRCLE
Bulk Pack - 112



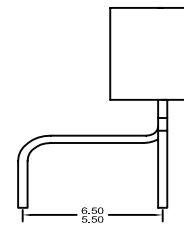
SOT54 WIDE PITCH
Tape/ Reel Pack - 116
Ammo Pack - 126



SOT54 LEAD BEND L01
Bulk Pack - 412



SOT54 LEAD BEND L02
Bulk Pack - 412



Remark: Detailed dimensions refer to POD drawing.

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