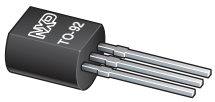


BT131 series

Triacs logic level

Rev. 9 — 9 November 2011 Product data sheet

1. Product profile

1.1 General description

Passivated, sensitive gate triacs in a SOT54 plastic package

1.2 Features and benefits

- Designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

1.3 Applications

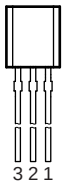
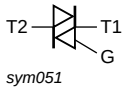
- General purpose switching and phase control

1.4 Quick reference data

- $V_{DRM} \leq 600$ V (BT131-600)
- $V_{DRM} \leq 800$ V (BT131-800)
- $I_{T(RMS)} \leq 1$ A
- $I_{TSM} \leq 12.5$ A

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	main terminal 2 (T2)	 SOT54 (TO-92)	 *sym051*
2	gate (G)		
3	main terminal 1 (T1)		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BT131-600	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54
BT131-800			

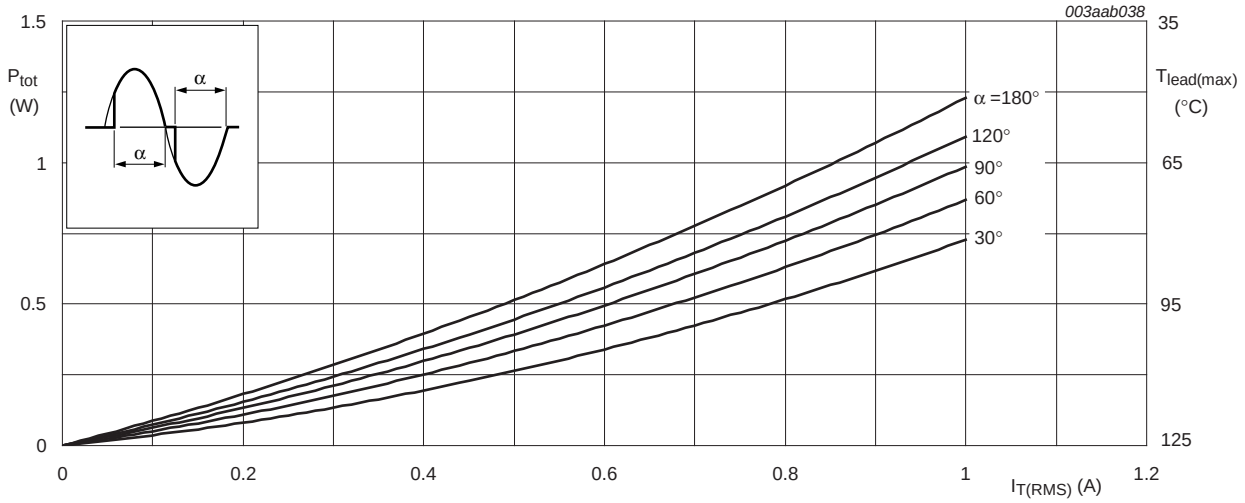
4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

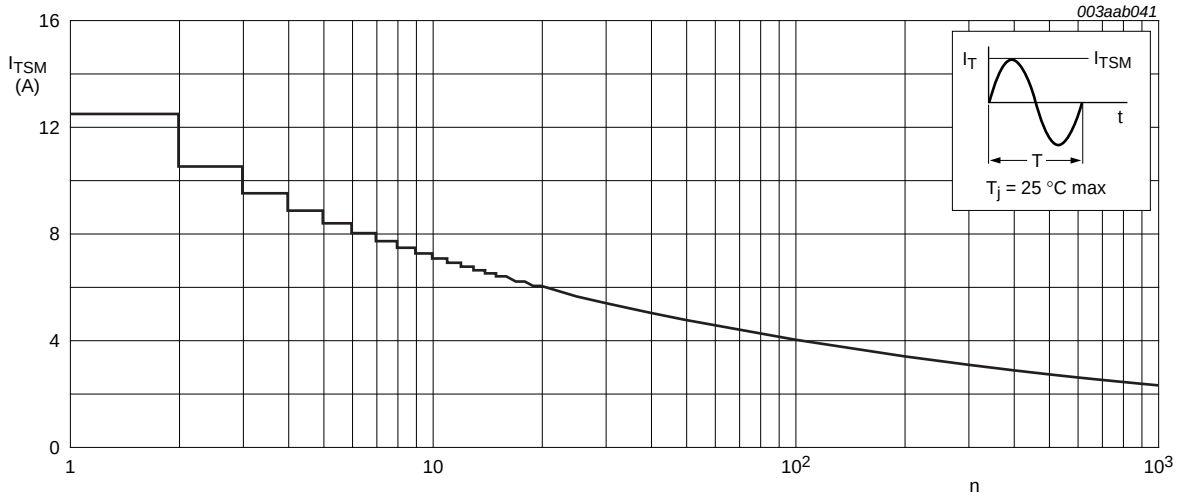
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage					
	BT131-600		[1]	-	600	V
	BT131-800			-	800	V
$I_{T(RMS)}$	RMS on-state current	all conduction angles; T_{lead} = 51.2 °C; see Figure 1, 4 and 5		-	1	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; T_j = 25 °C prior to surge; see Figure 2 and 3				
		t = 20 ms		-	12.5	A
		t = 16.7 ms		-	13.8	A
I^2t	I^2t for fusing	t = 10 ms		-	1.28	A^2s
dI_T/dt	rate of rise of on-state current	I_{TM} = 1.5 A; I_G = 20 mA; dI_G/dt = 200 mA/µs				
		T2+ G+		-	50	A/µs
		T2+ G–		-	50	A/µs
		T2– G–		-	50	A/µs
		T2– G+		-	10	A/µs
I_{GM}	peak gate current			-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.1	W
T_{stg}	storage temperature			–40	+150	°C
T_j	junction temperature			-	125	°C

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.



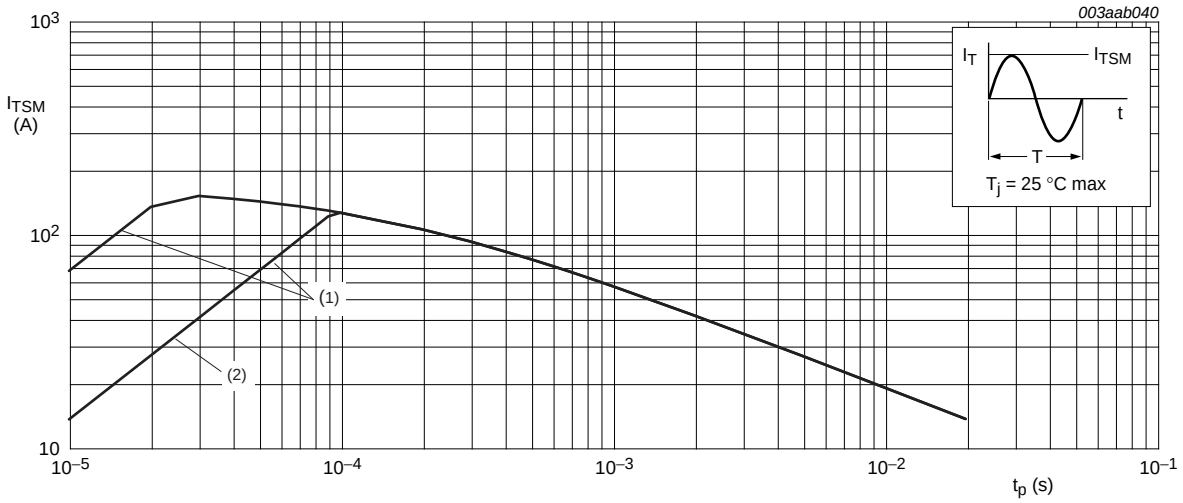
a = form factor = $I_{T(RMS)}/I_{T(AV)}$

Fig 1. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

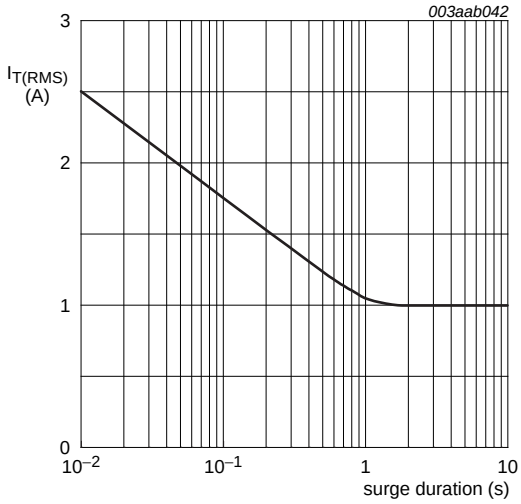


$t_p \leq 20$ ms

(1) dI_T/dt limit

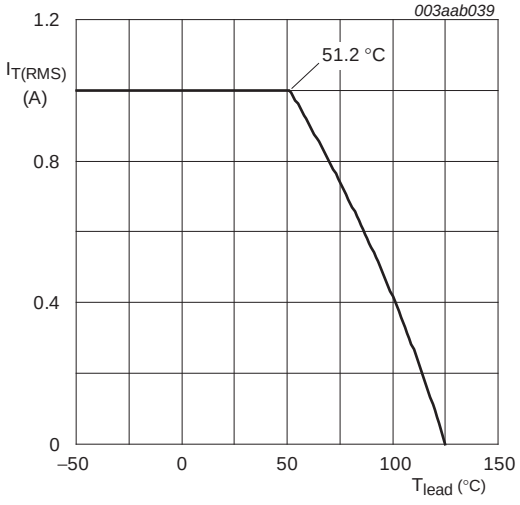
(2) T2– G+ quadrant

Fig 3. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values



f = 50 Hz; $T_{lead} \leq 51.2$ °C

Fig 4. RMS on-state current as a function of surge duration, for sinusoidal currents; maximum values



(1) $T_{lead} = 51.2$ °C

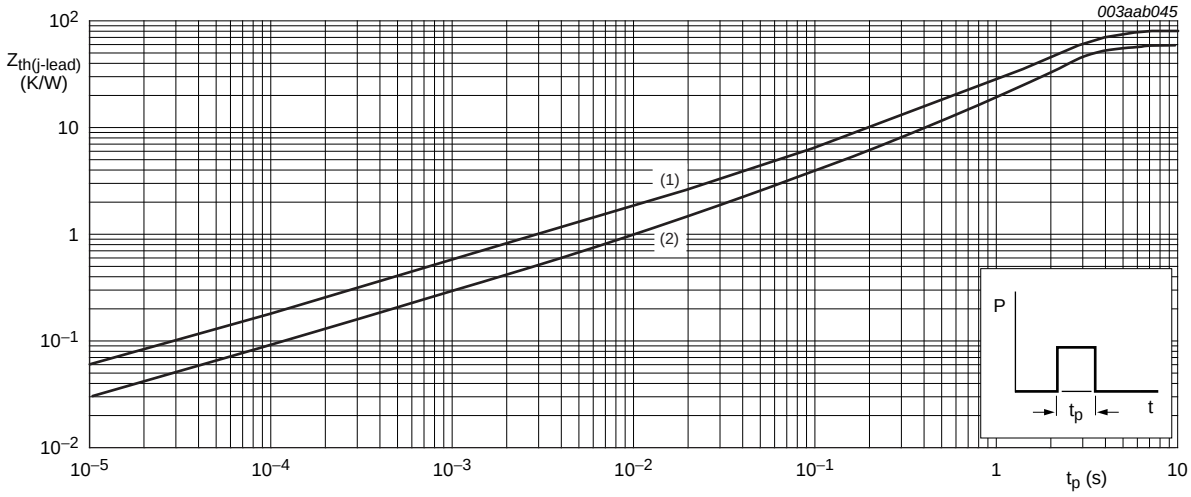
Fig 5. RMS on-state current as a function of lead temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}lead)}$	thermal resistance from junction to lead	full cycle		-	-	60	K/W
		half cycle		-	-	80	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	see Figure 6	[1]	-	150	-	K/W

[1] Mounted on a printed-circuit board; lead length = 4 mm



(1) half cycle

(2) full cycle

Fig 6. Transient thermal impedance as a function of pulse width

6. Characteristics

Table 5. Characteristics

T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; see Figure 8				
		T2+ G+	-	0.4	3	mA
		T2+ G–	-	1.3	3	mA
		T2– G–	-	1.4	3	mA
		T2– G+	-	3.8	7	mA
I_L	latching current	V_D = 12 V; I_{GT} = 100 mA; see Figure 10				
		T2+ G+	-	1.2	5	mA
		T2+ G–	-	4	8	mA
		T2– G–	-	1	5	mA
		T2– G+	-	2.5	8	mA
I_H	holding current	V_D = 12 V; I_{GT} = 100 mA; see Figure 11	-	1.3	5	mA
V_T	on-state voltage	I_T = 1.4 A; see Figure 9	-	1.2	1.5	V
V_{GT}	gate trigger voltage	I_T = 10 mA; gate open circuit; see Figure 7				
		V_D = 12 V; I_{GT} = 100 mA	-	0.7	1.5	V
		V_D = 400 V; I_{GT} = 100 mA; T_j = 125 °C	0.2	0.3	-	V
I_D	off-state current	$V_D = V_{DRM(max)}$; T_j = 125 °C	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 67 % $V_{DRM(max)}$; T_j = 125 °C; exponential waveform; R_{GK} = 1 kΩ; see Figure 12	10	20	-	V/µs
dV_{com}/dt	rate of change of commutating current	V_{DM} = 400 V; T_j = 125 °C; dI_{com}/dt = 0.5 A/ms	2	-	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 1.5 A; $V_D = V_{DRM(max)}$; I_G = 100 mA; dI_G/dt = 5 A/µs	-	2	-	µs

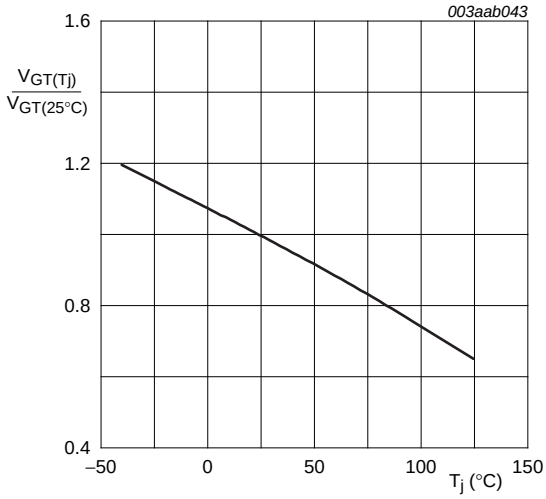
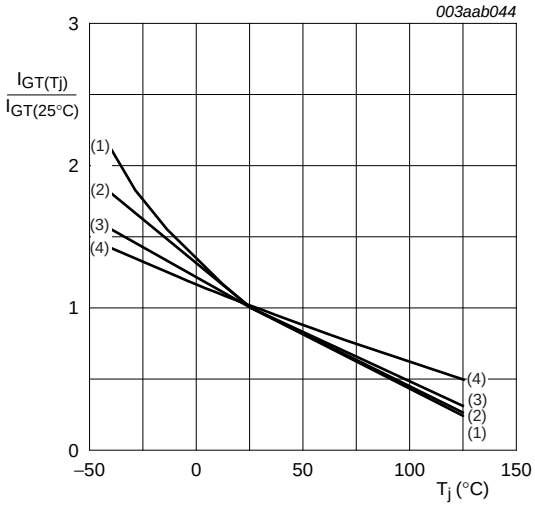
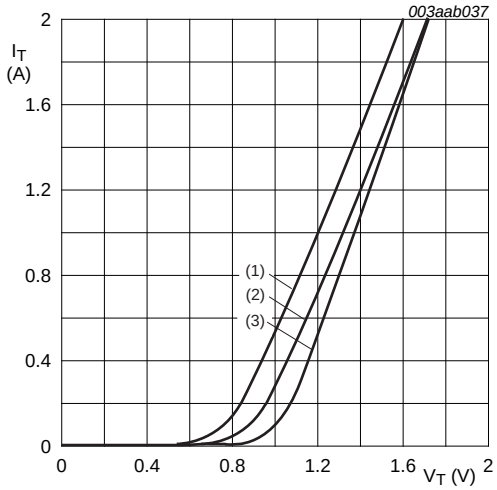


Fig 7. Normalized gate trigger voltage as a function of junction temperature



(1) T2– G+
(2) T2– G–
(3) T2+ G–
(4) T2+ G+

Fig 8. Normalized gate trigger current as a function of junction temperature



V_o = 0.92 V

R_s = 0.4 Ω.

(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig 9. On-state current characteristics

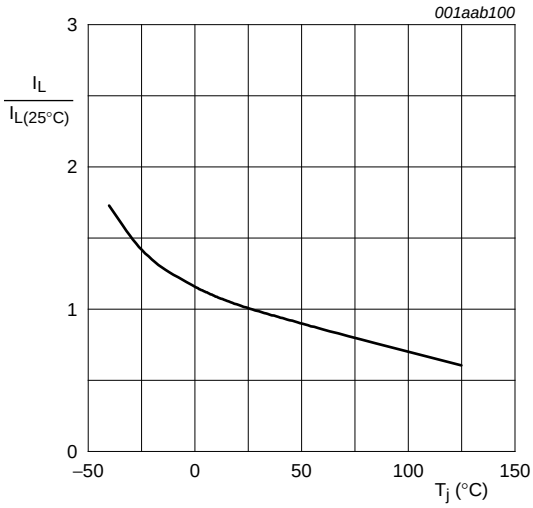


Fig 10. Normalized latching current as a function of junction temperature

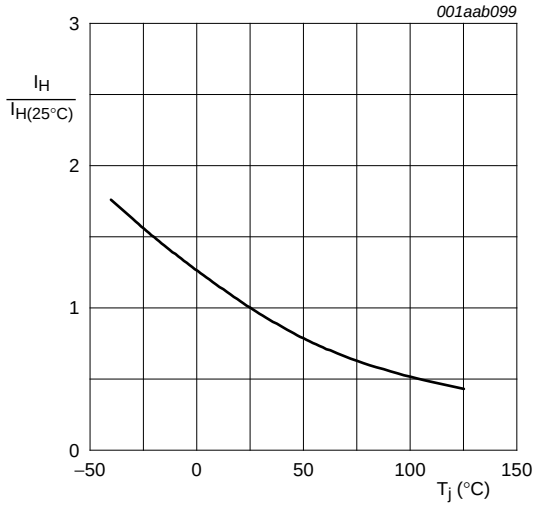


Fig 11. Normalized holding current as a function of junction temperature

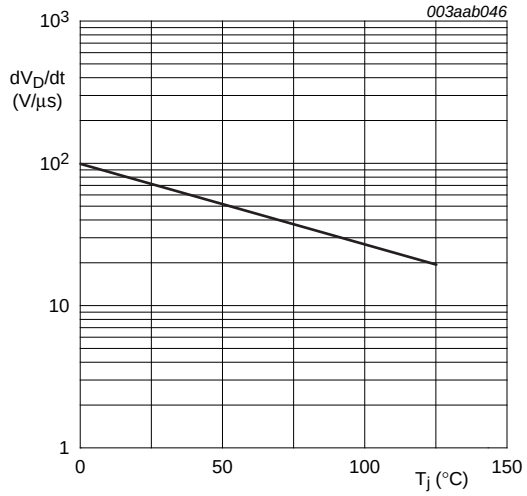


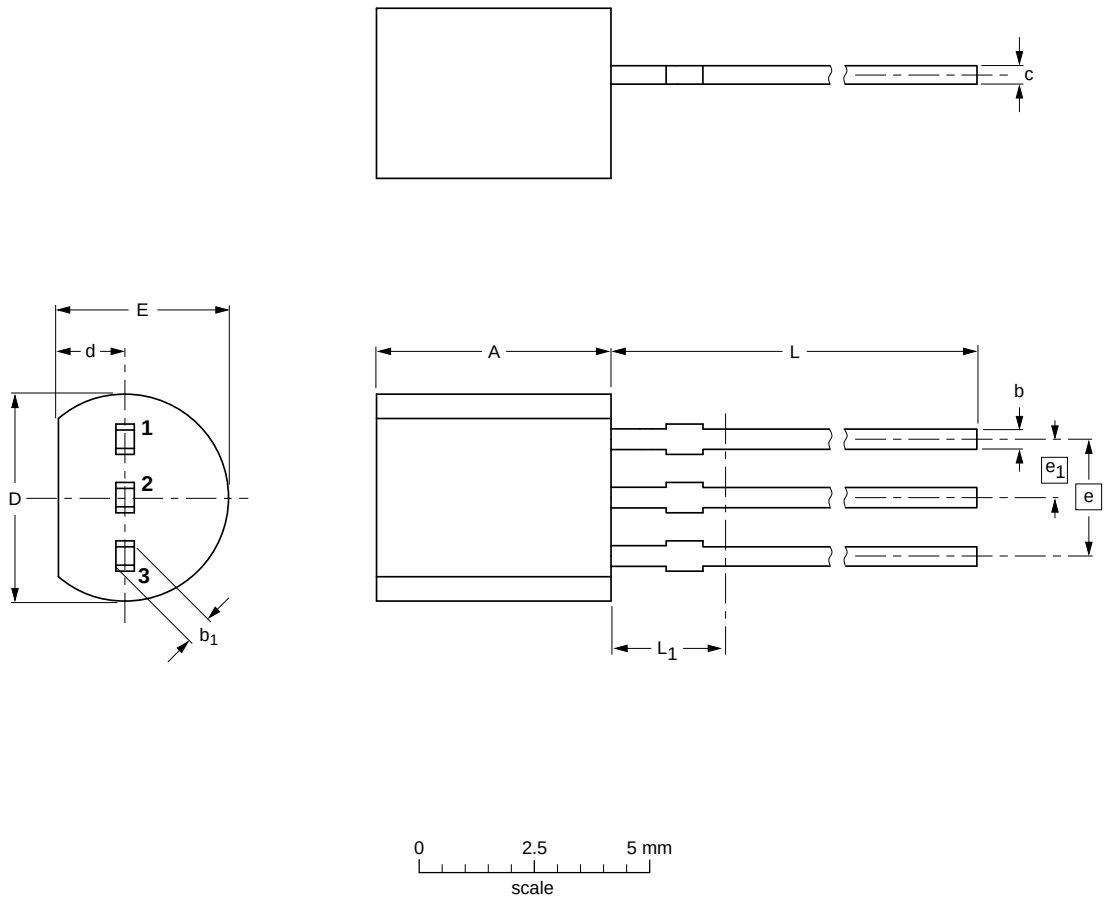
Fig 12. Rate of rise of off-state voltage as a function of junction temperature; minimum values

7. Package information

Epoxy meets requirements of UL94 V-0 at $\frac{1}{8}$ inch.

8. Package outline

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

Fig 13. Package outline SOT54 (TO-92)

9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT131_SER v.9	20111109	Product data sheet	-	BT131_SER v.8
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
BT131_SER v.8	20050909	Product data sheet	-	BT131_SERIES v.7
BT131_SERIES v.7	20040101	Product specification	-	BT131_SERIES v.6
BT131_SERIES v.6	20030801	Product specification	-	BT131_SERIES v.5
BT131_SERIES v.5	20001201	Product specification	-	BT131_SERIES v.4
BT131_SERIES v.4	20000501	Product specification	-	BT131_SERIES v.3
BT131_SERIES v.3	19980401	Product specification	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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12. Contents

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Document identifier: BT131_SER