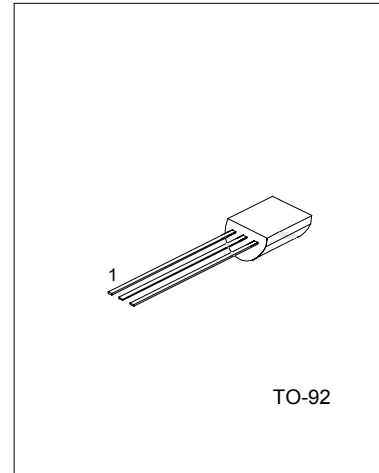
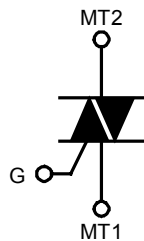


TRIACS LOGIC LEVEL

DESCRIPTION

Passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

SYMBOL



TO-92

1:MT1 2:GATE 3:MT2

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Repetitive Peak Off-State Voltage BT131-500 BT131-600 BT131-800	<a href="http://www.DataSheet4U.com">www.DataSheet4U.com</a> V <sub>DRM</sub>	500* 600* 800*	V
RMS On-State Current Full Sine Wave; T <sub>lead</sub> ≤ 51°C	I <sub>T(RMS)</sub>	1	A
Non-Repetitive Peak On-State Current (Full Sine Wave; T <sub>j</sub> = 25°C prior to surge) t = 20ms t = 16.7ms	I <sub>TSM</sub>	16 17.6	A
Circuit Fusing (t = 10ms)	I <sup>2</sup> t	1.28	A <sup>2</sup> s
Repetitive Rate of Rise of On-State Current after Triggering I <sub>TM</sub> = 1.5A, I <sub>G</sub> = 0.2A, dI <sub>G</sub> /dt = 0.2A/μs	dI <sub>T</sub> /dt	50 50 50 10	A/μs
		T2+G+ T2+G- T2-G- T2-G+	
Peak Gate Voltage	V <sub>GM</sub>	5	V
Peak Gate Current	I <sub>GM</sub>	2	A
Peak Gate Power	P <sub>GM</sub>	5	W
Average Gate Power (over any 20ms period)	P <sub>G(AV)</sub>	0.5	W
Operating Junction Temperature	T <sub>j</sub>	125	°C
Storage temperature	T <sub>stg</sub>	-40~150	°C

\*Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/μs.

## THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal Resistance Junction to Lead Full Cycle Half Cycle	Rth j-lead			60 80	K/W
Thermal Resistance junction to Ambient (PCB mounted ;lead length=4mm)	Rth j-lead		150		K/W

ELECTRICAL CHARACTERISTICS (T<sub>j</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
Gate Trigger Current	I <sub>GT</sub>	V <sub>D</sub> =12V, I <sub>T</sub> =0.1A T2+G+ T2+G- T2-G- T2-G+		0.4 1.3 1.4 3.8	3 3 3 7	mA
Latching Current	I <sub>L</sub>	V <sub>D</sub> =12V, I <sub>GT</sub> =0.1A T2+G+ T2+G- T2-G- T2-G+		1.2 4.0 1.0 2.5	5 8 5 8	mA
On-State Voltage Latching Current	V <sub>T</sub>	I <sub>T</sub> =2.0A		1.2	1.5	V
Gate Trigger Voltage	V <sub>GT</sub>	V <sub>D</sub> =12V, I <sub>T</sub> =0.1A V <sub>D</sub> =400V, I <sub>T</sub> =0.1A, T <sub>j</sub> =125°C	0.2	0.7 0.3	1.5	V
Off-state Leakage Current	I <sub>D</sub>	V <sub>D</sub> =V <sub>DRM(max)</sub> , T <sub>j</sub> =125°C		0.1	0.5	mA
<b>DYNAMIC CHARACTERISTICS</b>						
Holding Current	I <sub>H</sub>	V <sub>D</sub> =12V, I <sub>GT</sub> =0.1A		1.3	5	mA
Critical Rate of Rise of off-state Voltage	dV <sub>D</sub> /dt	V <sub>DM</sub> =67% V <sub>DRM(max)</sub> , T <sub>j</sub> =125°C Exponential waveform, R <sub>GK</sub> =1kΩ	5	15		V/μs
Gate Controlled Turn-on Time	t <sub>gt</sub>	I <sub>TM</sub> =1.5A, V <sub>D</sub> =V <sub>DRM(max)</sub> , I <sub>G</sub> =0.1A dI <sub>G</sub> /dt=5A/μs		2		μs

TYPICAL CHARACTERISTICS

Figure 1. Maximum on-state Dissipation,  $P_{tot}$  vs RMS On-state Current,  $I_T(RMS)$ , Where  $\alpha$  = conduction Angle.

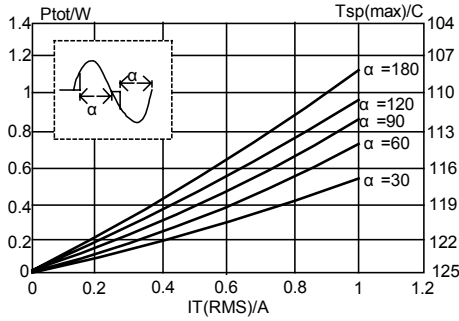


Figure 4. Maximum Permissible RMS Current  $I_T(RMS)$  vs Lead Temperature  $T_{lead}$

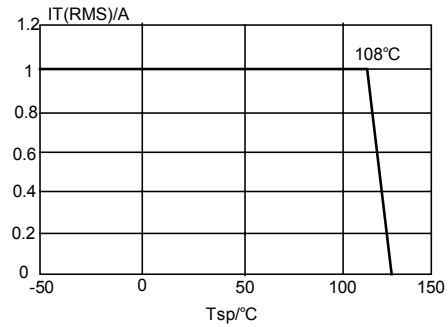


Figure 2. Maximum Permissible Non-repetitive Peak On-state Current  $I_{TSM}$ , vs Pulse Width  $t_p$ , for Sinusoidal Currents,  $t_p \leq 20ms$

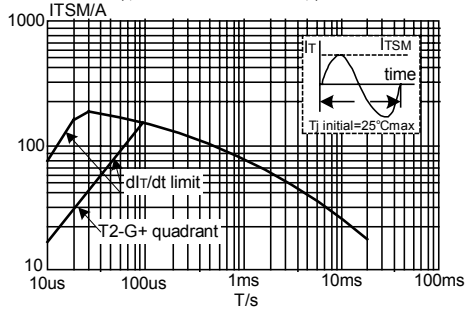


Figure 5. Maximum Permissible Repetitive RMS on-state Current  $I_T(RMS)$ , vs Surge Duration, for Sinusoidal Currents,  $f=50Hz$ ;  $T_{lead} \leq 51^\circ C$

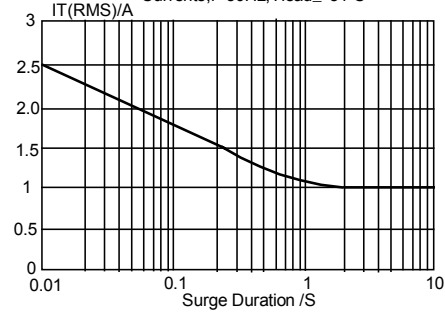


Figure 3. Maximum Permissible Non-Repetitive peak on-state Current  $I_{TSM}$ , vs Number of Cycles, for Sinusoidal Currents,  $f=50Hz$

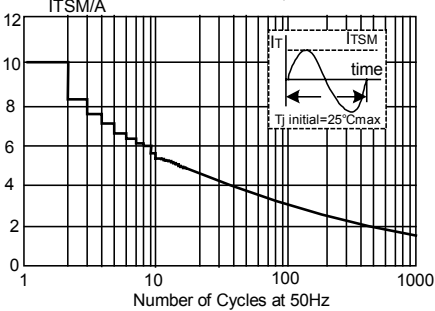


Figure 6. Normalised Gate Trigger Voltage  $V_{GT}(T_j)/V_{GT}(25^\circ C)$ , vs Junction Temperature  $T_j$

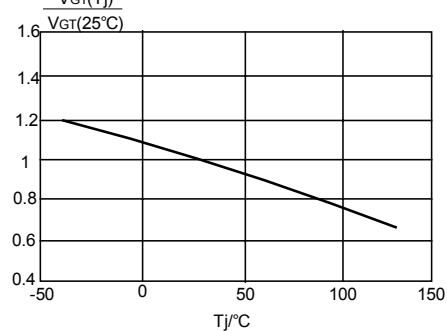


Figure 7. Normalised Gate Trigger current  $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$ , vs Junction Temperature  $T_j$

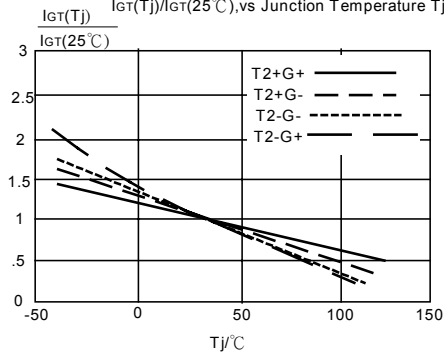


Figure 10. Typical and Maximum On-state Characteristic

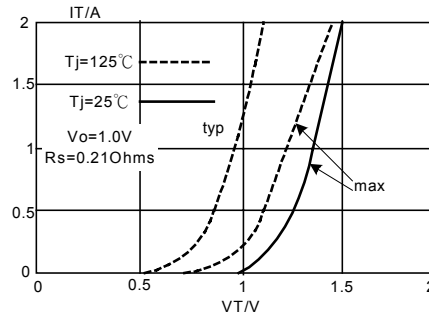


Figure 8. Normalised Latching Current  $I_L(T_j)/I_L(25^\circ\text{C})$ , vs Junction Temperature  $T_j$

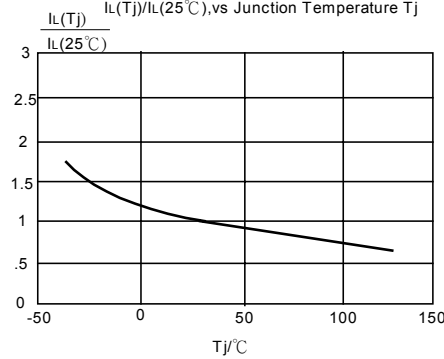


Figure 11. Transient Thermal Impedance  $Z_{th\ j\text{-lead}}$ , vs Pulse Width  $t_p$

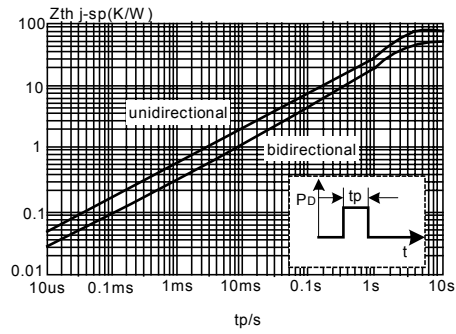


Figure 9. Normalised Holding Current  $I_H(T_j)/I_H(25^\circ\text{C})$ , vs Junction Temperature  $T_j$

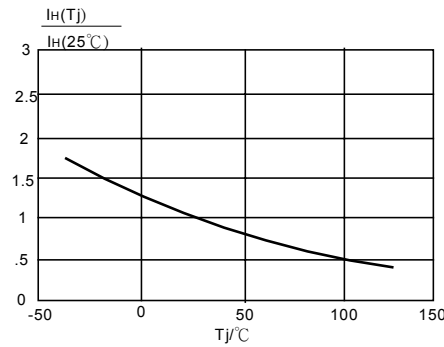
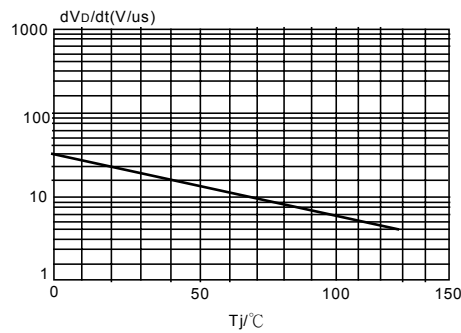


Figure 12. Typical Critical Rate of Rise of off-state Voltage,  $dV_D/dt$  vs Junction Temperature  $T_j$



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