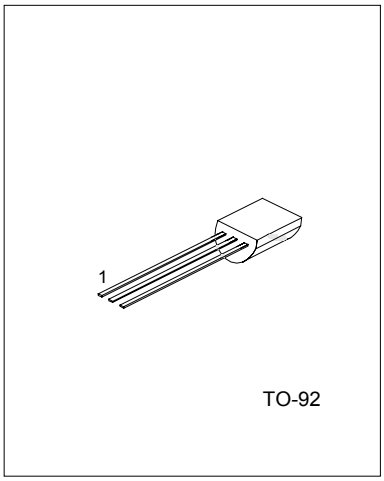
## TRIACS LOGIC LEVEL

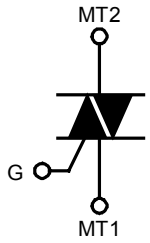



1:MT1 2:GATE 3:MT2

### DESCRIPTION

Passivated, sensitive gate triaces in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers. logic integrated circuits and other low power gate trigger circuits.

### SYMBOL




### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Repetitive Peak Off-State Voltage<br>BT131-500<br>BT131-600<br>BT131-800 | $V_{DRM}$ | <br>500*<br>600*<br>800* | V |
| RMS On-State Current<br>Full Sine Wave; Tlead≤51°C | $I_{T(RMS)}$ | 1 | A |
| Non-Repetitive Peak On-State Current<br>(Full Sine Wave; Tj=25°C prior to surge)<br>t=20ms<br>t=16.7ms | $I_{TSM}$ | <br><br>16<br>17.6 | A |
| Circuit Fusing (t=10ms) | $I^2t$ | 1.28 | $A^2s$ |
| Repetitive Rate of Rise of On-State Current after Triggering<br>ITM=1.5A, IG=0.2A, $dI_G/dt$=0.2A/μs<br>T2+G+<br>T2+G-<br>T2-G-<br>T2-G+ | $dI_T/dt$ | <br><br>50<br>50<br>50<br>10 | A/μs |
| Peak Gate Voltage | $V_{GM}$ | 5 | V |
| Peak Gate Current | $I_{GM}$ | 2 | A |
| Peak Gate Power | $P_{GM}$ | 5 | W |
| Average Gate Power (over any 20ms period) | $P_{G(AV)}$ | 0.5 | W |
| Operating Junction Temperature | Tj | 125 | °C |
| Storage temperature | Tstg | -40~150 | °C |

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/μs.

## THERMAL RESISTANCES

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Thermal Resistance Junction to Lead<br>Full Cycle<br>Half Cycle | Rth j-lead | | | <br>60<br>80 | K/W |
| Thermal Resistance junciton to Ambient<br>(PCB mounted ;lead length=4mm) | Rth j-lead | | 150 | | K/W |

## ELECTRICAL CHARACTERISTICS (Tj=25°C, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| Gate Trigger Current | $I_{GT}$ | $V_D$=12V, $I_T$=0.1A | | | | |
| | | T2+G+ | | 0.4 | 3 | |
| | | T2+G- | | 1.3 | 3 | mA |
| | | T2-G- | | 1.4 | 3 | |
| | | T2-G+ | | 3.8 | 7 | |
| Latching Current | $I_L$ | $V_D$=12V, $I_{GT}$=0.1A | | | | |
| | | T2+G+ | | 1.2 | 5 | |
| | | T2+G- | | 4.0 | 8 | mA |
| | | T2-G- | | 1.0 | 5 | |
| | | T2-G+ | | 2.5 | 8 | |
| On-State Voltage Latching Current | $V_T$ | $I_T$=2.0A | | 1.2 | 1.5 | V |
| Gate Trigger Voltage | $V_{GT}$ | $V_D$=12V, $I_T$=0.1A | | 0.7 | 1.5 | V |
| | | $V_D$=400V, $I_T$=0.1A, Tj=125°C | 0.2 | 0.3 | | |
| Off-state Leakage Current | $I_D$ | $V_D$=$V_{DRM(max)}$, Tj=125°C | | 0.1 | 0.5 | mA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Holding Current | $I_H$ | $V_D$=12V, $I_{GT}$=0.1A | | 1.3 | 5 | mA |
| Critical Rate of Rise ofoff-state Voltage | $dV_D/dt$ | $V_{DM}$=67% $V_{DRM(max)}$, Tj=125°C<br>Exponential waveform,$R_{GK}$=1kΩ | 5 | 15 | | V/μs |
| Gate Controlled Turn-on Time | $t_{gt}$ | $I_{TM}$=1.5A,$V_D$=$V_{DRM(max)}$, $I_G$=0.1A<br>$dI_G/dt$=5A/μs | | 2 | | μs |

## TYPICAL CHARACTERISTICS

Figure 1.Maximum on -state Dissipation.Ptot vs RMS On-state Current,IT(RMS),Whereα =conduction Angle.

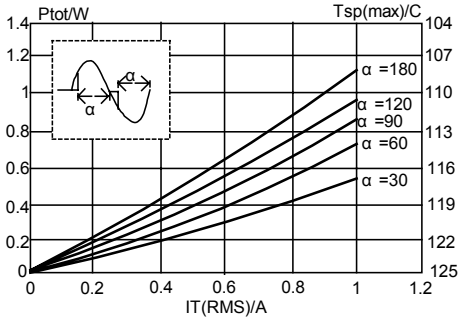



Figure 2. Maximum Permissible Non-repetitive Peak On-state Current ITSM,vs Pulse Width tp,for Sinusoidal Currents,tp≤ 20ms

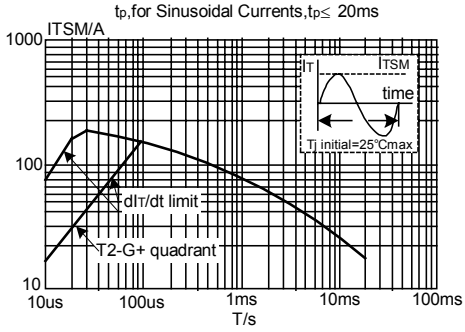



Figure 3 .Maximum Permissible Non-Repetitive peak on-state Current ITSM,vs Number of Cycles, for Sinusoidal Currents,f=50Hz

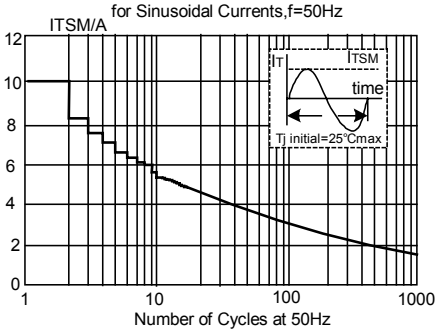



Figure 4.Maximum Permissible RMS Current IT(RMS) vs Lead Temperature Tlead

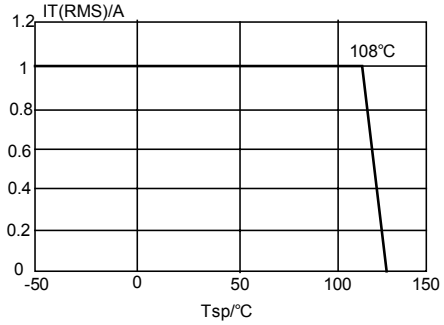



Figure 5.Maximum Permissible Repetitive RMS on-state Current IT(RMS),vs Surge Duration,for Sinusoidal Currents,f=50Hz;Tlead≤ 51℃

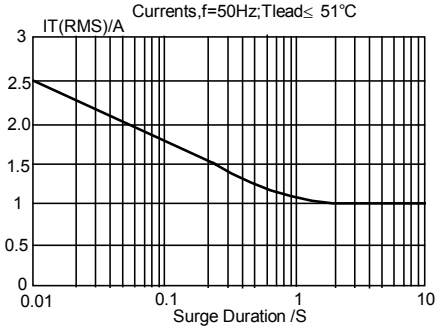



Figure 6.Normalised Gate Trigger Voltage VGT(Tj)/ VGT(25℃),vs Junction Temperature Tj

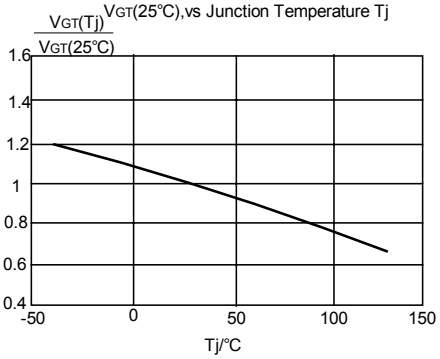


Figure 7.Normalised Gate Trigger current
IGT(Tj)/IGT(25℃),vs Junction Temperature Tj

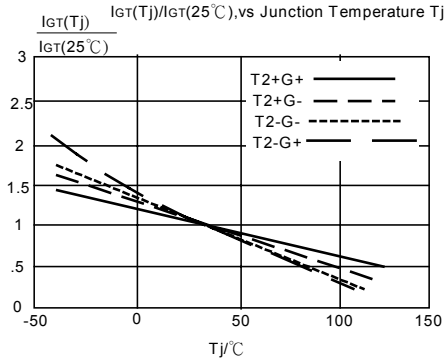



Figure 8.Normalised Latching Current
IL(Tj)/IL(25℃),vs Junction Temperature Tj

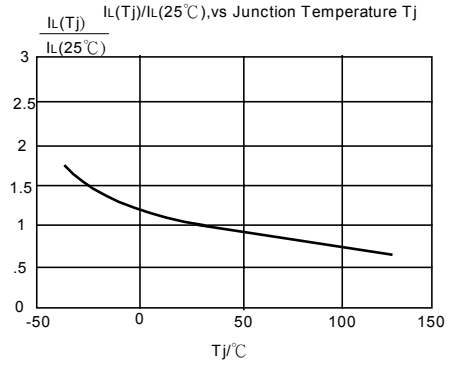



Figure 9.Normalised Holding Current
IH(Tj)/IH(25℃),vs Junction Temperature Tj

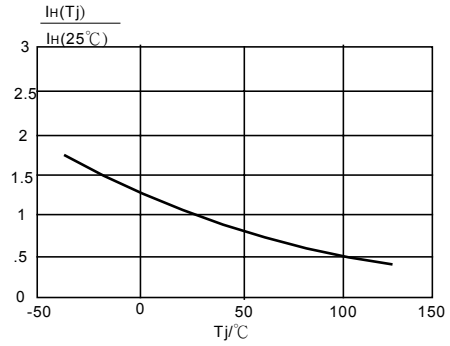



Figure 10.Typical and Maximum
On-state Characteristic

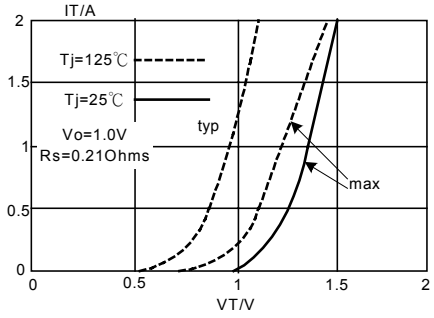



Figure 11.Transient Thermal Impedance
Zth j-lead,vs Pulse Width tp

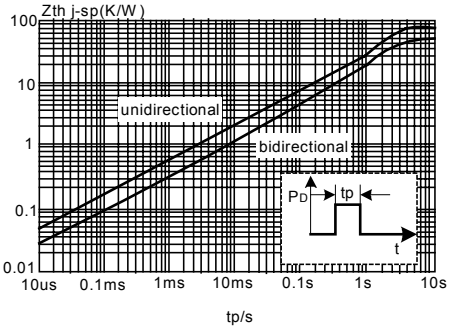



Figure 12.Typical Critical Rate of Rise of off-state Voltage,
dVD/dt vs Junction Temperature Tj