
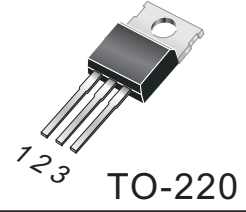


Description

Passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

<p>Symbol</p> 		<p>Simplified outline</p> 	
Pin	Description		
1	Main terminal 1 (T1)		
2	Main terminal 2 (T2)		
3	gate (G)		
TAB	Main terminal 2 (T2)		

Applications:

- ◆ Motor control
- ◆ Industrial and domestic lighting
- ◆ Heating
- ◆ Static switching

Features

- ◆ Blocking voltage to 600 V
- ◆ On-state RMS current to 4 A

SYMBOL	PARAMETER	Value	Unit
V_{DRM}	Repetitive peak off-state voltages	600	V
$I_{T(RMS)}$	RMS on-state current	4	A
I_{TSM}	Non-repetitive peak on-state current	25	A

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$R_{th(j-mb)}$	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
$R_{th(j-a)}$	Thermal resistance Junction to ambient	In free air	-	60	-	K/W

K/W

HAOPIN MICROELECTRONICS CO.,LTD.

Limiting values in accordance with the Maximum system(IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	Value	UNIT	
V_{DRM}	Repetitive peak off-state Voltages		-	600	V	
$I_{T(RMS)}$	RMS on-state current	Full sine wave; $T_{mb} \leq 107^\circ\text{C}$	-	4	A	
I_{TSM}	Non-repetitive surge peak on-state current	full sine wave;, $T_j=25^\circ\text{C}$ prior to surge	t=20ms	-	25	A
			t=16.7ms	-	27	A
I^2t	I^2t for fusing	T=10ms	-	3.1	A ² S	
di_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM}=6\text{A}; I_G=0.2\text{A};$ $DI_G/dt=0.2\text{A}/\mu\text{s}$	T2+G+	-	50	A/ μs
			T2+G-	-	50	A/ μs
			T2-G-	-	50	A/ μs
			T2-G+	-	10	A/ μs
I_{GM}	Peak gate current		-	2	A	
V_{GM}	Peak gate voltage		-	5	V	
P_{GM}	Peak gate power		-	5	W	
$P_{G(AV)}$	Average gate power	Over any 20 ms period	-	0.5	W	
T_{stg}	Storage temperature		-40	150	$^\circ\text{C}$	
T_j	Operating junction Temperature		-	125	$^\circ\text{C}$	

$T_j=25^\circ\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	
Static characteristics							
I_{GT}	Gate trigger current	$V_D=12\text{V}; I_T=0.1\text{A}$	T2+G+	-	2.0	5	mA
			T2+G-	-	2.5	5	mA
			T2-G-	-	2.5	5	mA
			T2-G+	-	5.0	10	mA
I_L	Latching current	$V_D=12\text{V}; I_{GT}=0.1\text{A}$	T2+G+	-	1.6	10	mA
			T2+G-	-	4.5	15	mA
			T2-G-	-	1.2	10	mA
			T2-G+	-	2.2	15	mA
I_H	Holding current	$V_D=12\text{V}; I_{GT}=0.1\text{A}$	-	1.2	10	mA	
V_T	On-state voltage	$I_T=5\text{A}$	-	1.4	1.70	V	
V_{GT}	Gate trigger voltage	$V_D=12\text{V}; I_T=0.1\text{A}$	-	0.7	1.5	V	
		$V_D=400\text{V}; I_T=0.1\text{A}; T_j=125^\circ\text{C}$	0.25	0.4	-	V	
I_D	Off-state leakage current	$V_D=V_{DRM(max)}; T_j=125^\circ\text{C}$	-	0.1	0.5	mA	

Dynamic Characteristics

DV_D/dt	Critical rate of rise of Off-state voltage	$V_{DM}=67\% V_{DRM(max)}; T_j=125^\circ\text{C};$ Exponential wave form; $R_{GK}=1\text{K}\Omega$	-	5	-	V/ μs
t_{gt}	Gate controlled turn-on time	$I_{TM}=6\text{A}; V_D=V_{DRM(max)}; I_G=0.1\text{A};$ $DI_G/dt=5\text{A}/\mu\text{s}$	-	2	-	μs

Description

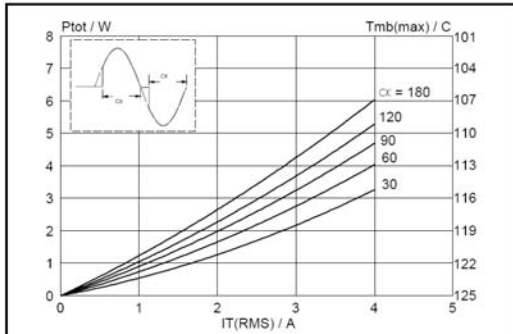


Fig.1. Maximum on-state dissipation, P_{tot} , versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

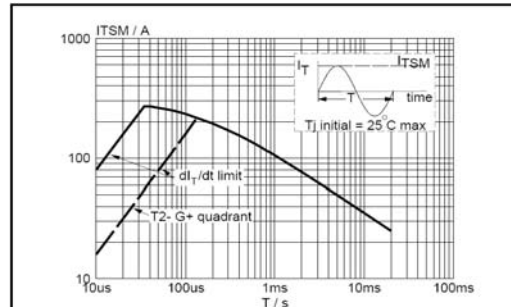


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 20ms$.

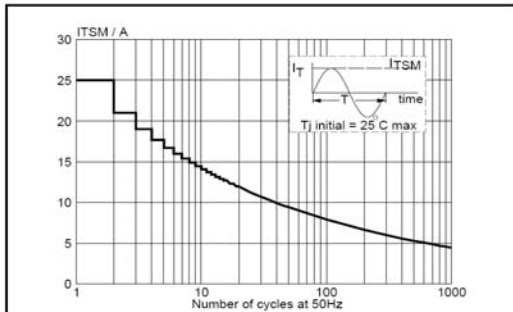


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50 Hz$.

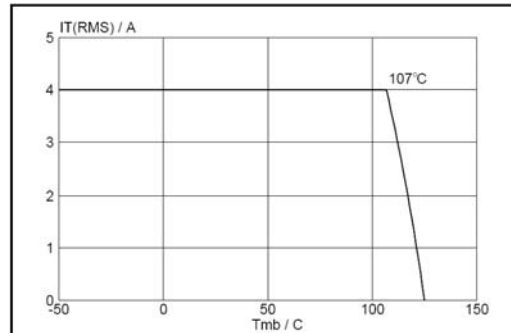


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb} .

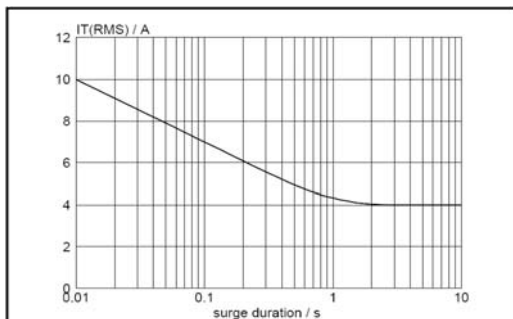


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50 Hz$; $T_{mb} \leq 107 C$.

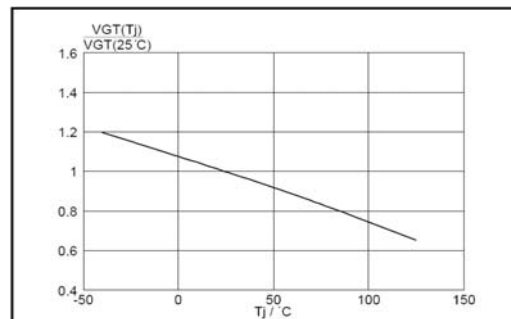
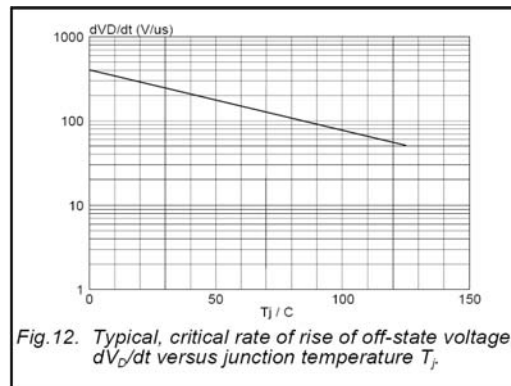
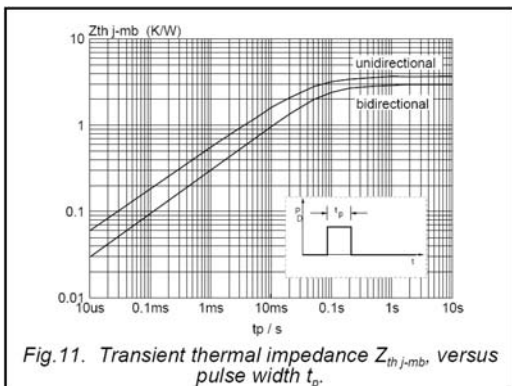
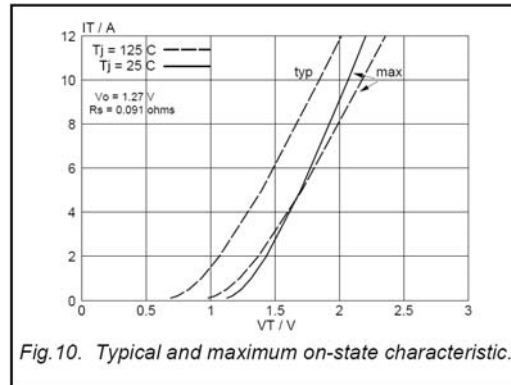
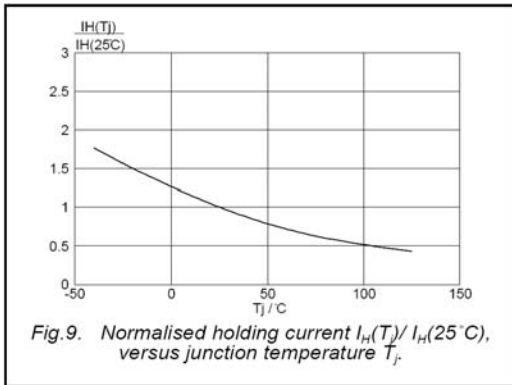
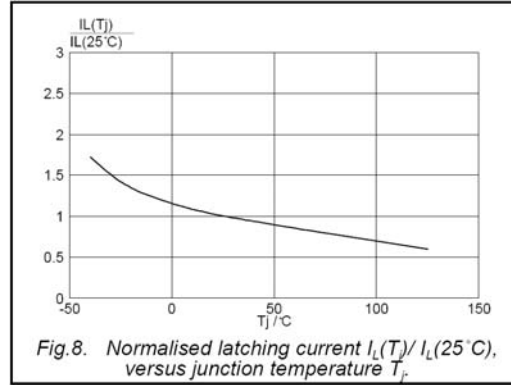
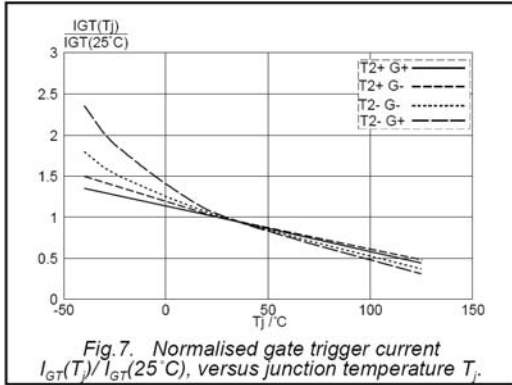


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25 C)$, versus junction temperature T_j .

Description



MECHANICAL DATA

