BT136S-800F

4Q Triac

30 September 2013 **Product data sheet**

1. General description

Planar passivated four quadrant triac in a SOT428 (DPAK) surface-mountable plastic package intended for use in general purpose bidirectional and phase control applications.

2. Features and benefits

- High blocking voltage capability
- Less sensitive gate for improved noise immunity
- Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in all four quadrants

3. Applications

- General purpose motor control
- General purpose switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		-	-	25	A
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq$ 107 °C; Fig. 1; Fig. 2; Fig. 3		-	-	4	A
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		-	5	25	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		-	8	25	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		-	11	25	mA
		V_D = 12 V; I_T = 0.1 A; T2- G+; T_j = 25 °C; Fig. 7		-	30	70	mA

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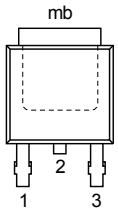
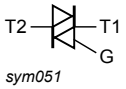
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 DPAK (SOT428)	
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT136S-800F	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ °C; Fig. 1; Fig. 2; Fig. 3		-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5		-	25	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	27	A
I^2t	I2t for fusing	$t_p = 10$ ms; SIN		-	3.1	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs; T2+ G+		-	50	A/µs
		$I_T = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs; T2+ G-		-	50	A/µs
		$I_T = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs; T2- G-		-	50	A/µs
		$I_T = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs; T2- G+		-	10	A/µs
I_{GM}	peak gate current			-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C

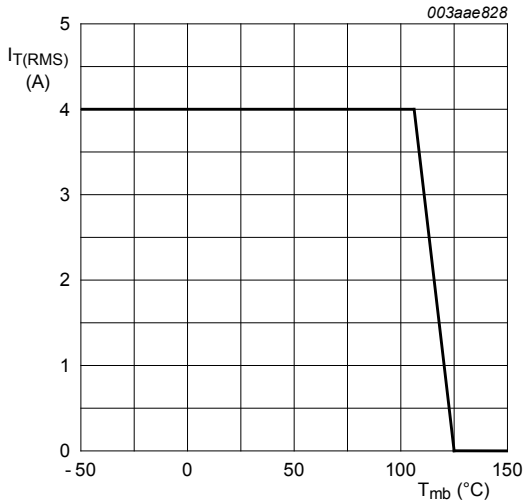
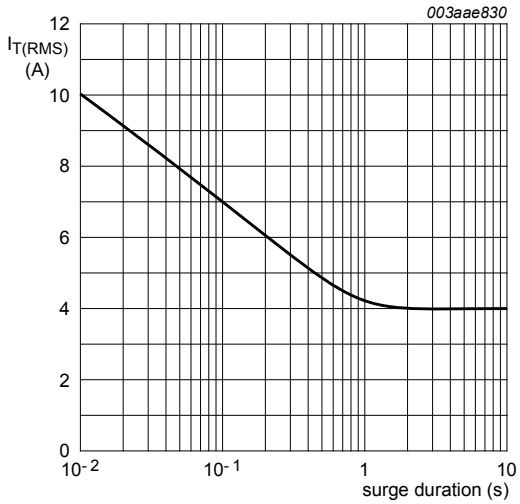


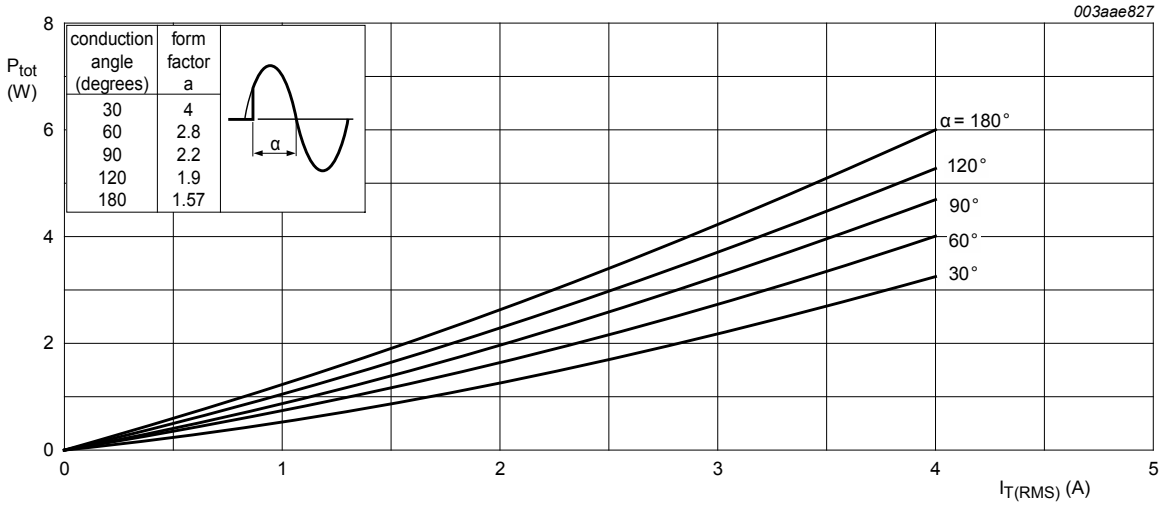
Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz

$T_{mb} \leq 107$ °C

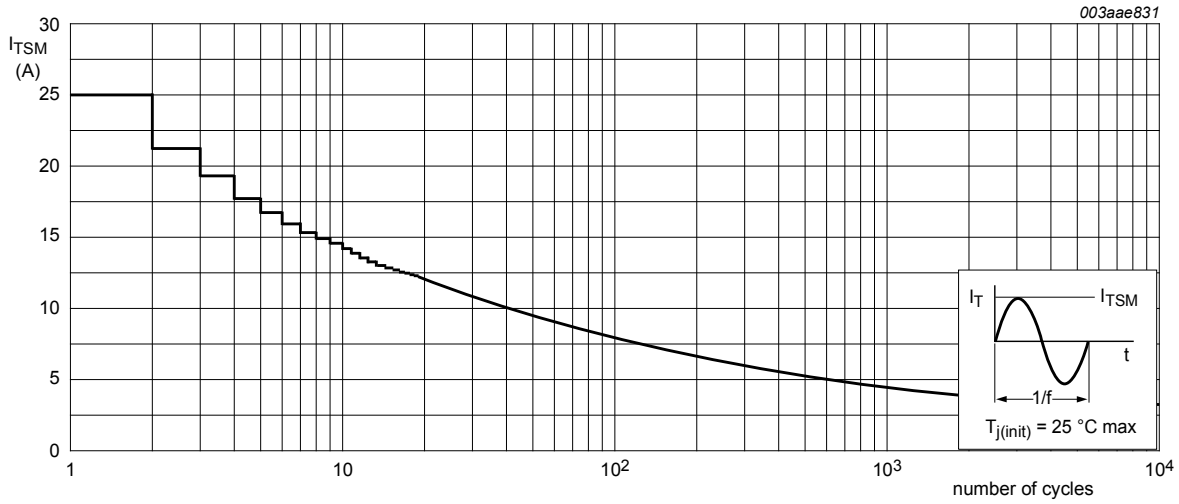
Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle

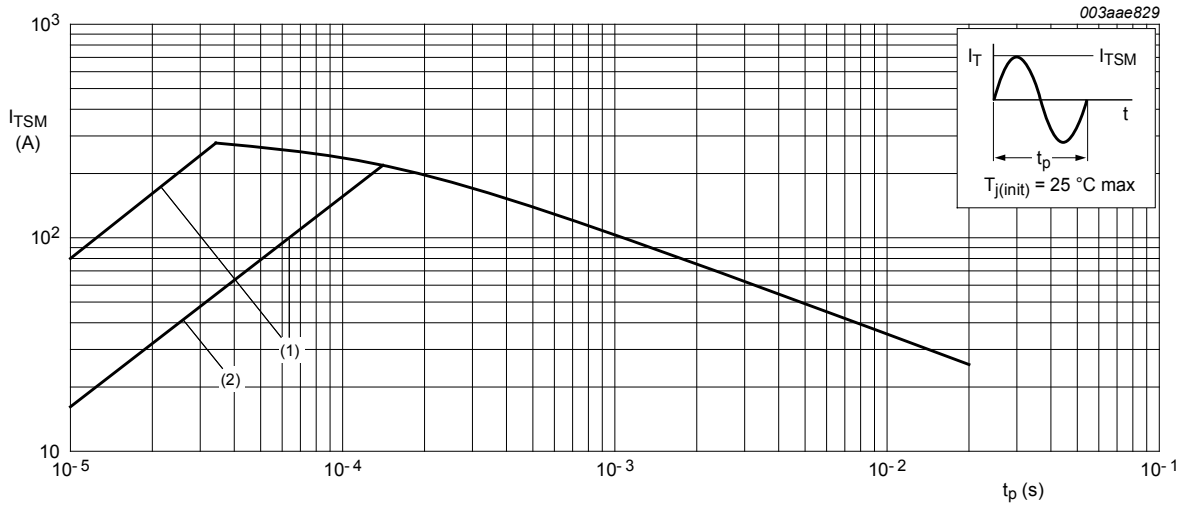
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

(2) T2- G+ quadrant limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	half cycle; Fig. 6		-	-	3.7	K/W
		full cycle; Fig. 6		-	-	3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; printed circuit board (FR4) mounted; standard footprint, single-sided copper, tin-plated		-	75	-	K/W

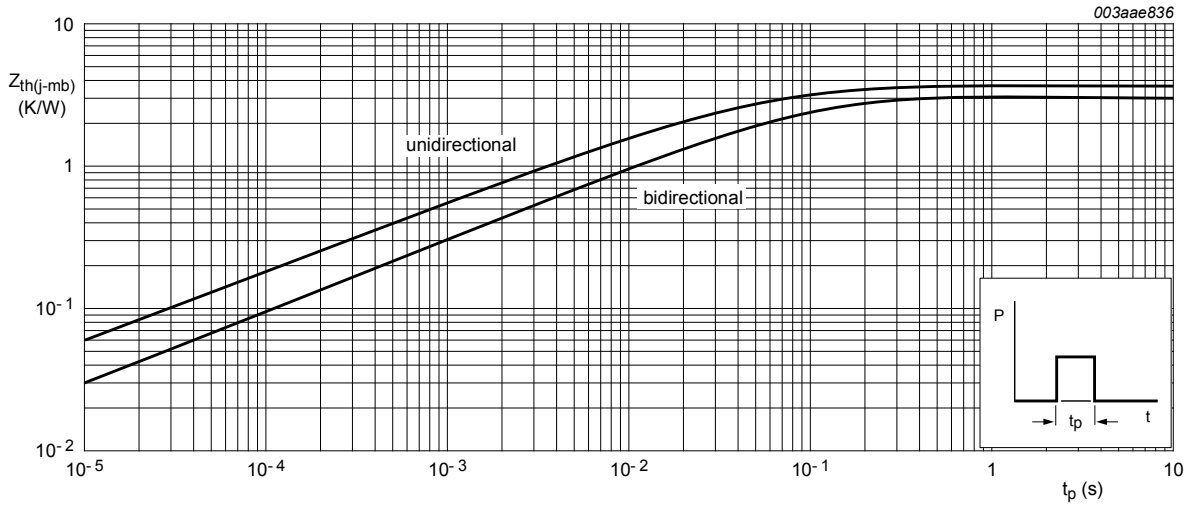
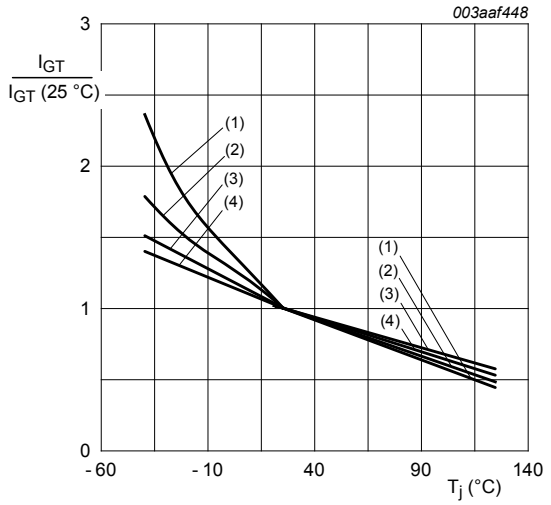


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		-	5	25	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		-	8	25	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		-	11	25	mA
		V_D = 12 V; I_T = 0.1 A; T2- G+; T_j = 25 °C; Fig. 7		-	30	70	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 8		-	7	20	mA
		V_D = 12 V; I_G = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 8		-	16	30	mA
		V_D = 12 V; I_G = 0.1 A; T2- G-; T_j = 25 °C; Fig. 8		-	5	20	mA
		V_D = 12 V; I_G = 0.1 A; T2- G+; T_j = 25 °C; Fig. 8		-	7	30	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	5	15	mA
V_T	on-state voltage	I_T = 5 A; T_j = 25 °C; Fig. 10		-	1.4	1.7	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.7	1	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C; Fig. 11		0.25	0.4	-	V
I_D	off-state current	V_D = 800 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		50	250	-	V/µs
dV_{com}/dt	rate of change of commutating voltage	V_D = 400 V; T_j = 95 °C; dI_{com}/dt = 1.8 A/ms; I_T = 4 A; gate open circuit		-	50	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 6 A; V_D = 800 V; I_G = 0.1 mA; dI_G/dt = 5 A/µs		-	2	-	µs



(1) T2- G+
(2) T2- G-
(3) T2+ G-
(4) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

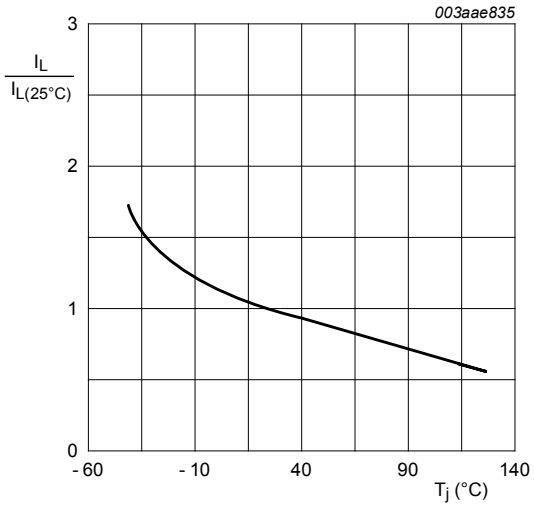


Fig. 8. Normalized latching current as a function of junction temperature

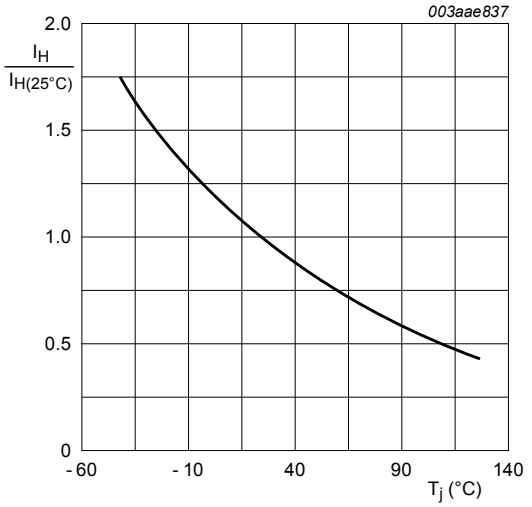
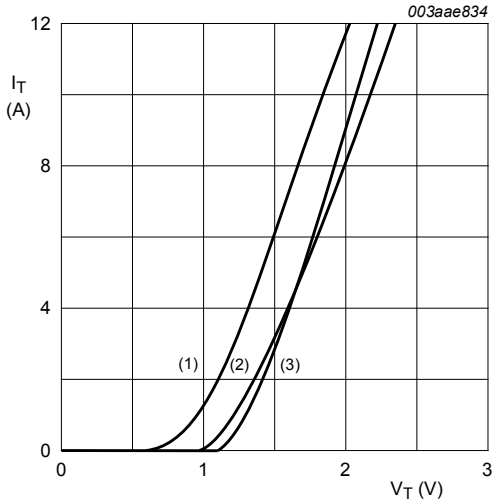


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.27 V
R_s = 0.091 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

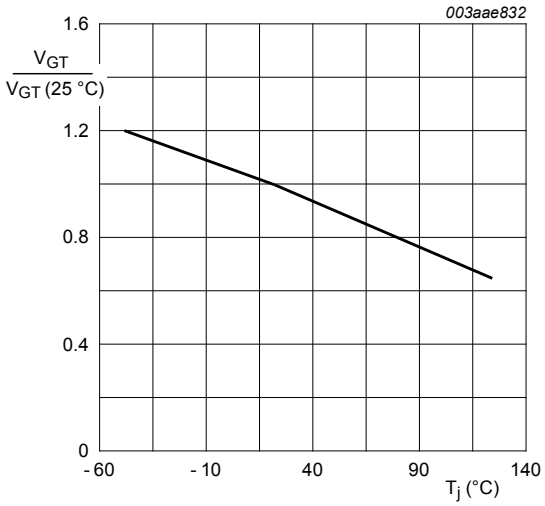
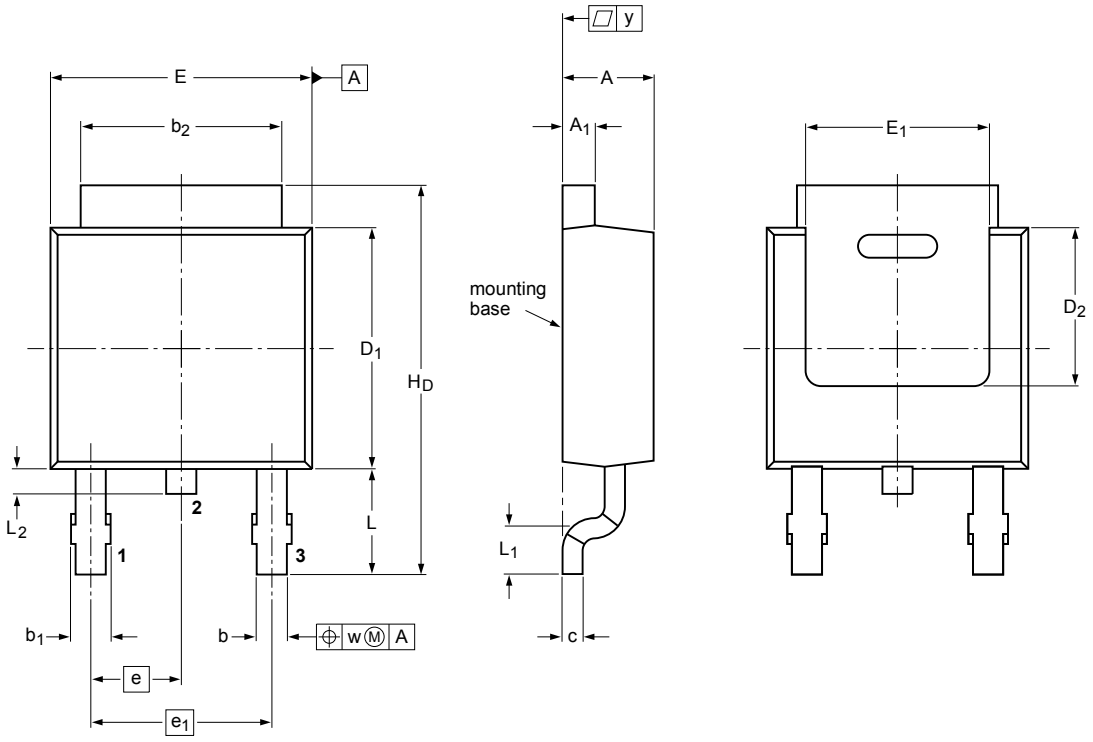


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig. 12. Package outline DPAK (SOT428)

11. Soldering

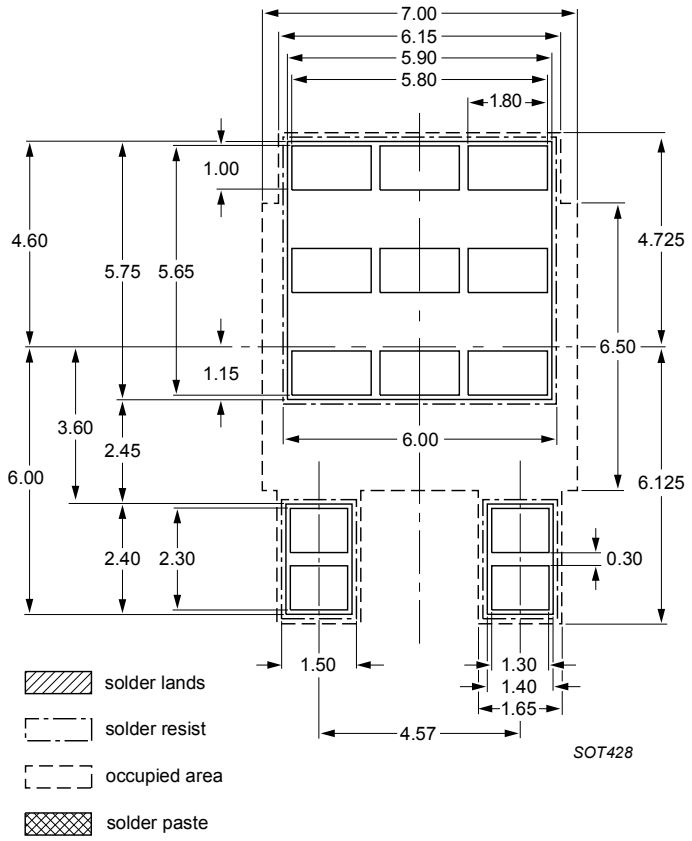


Fig. 13. Reflow soldering footprint for DPAK (SOT428)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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